QICK AMO Extension Updates

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Architecture of Generator

- Fifth order polynomial function for frequency modulation:

$$f[t] = c_0 + c_1 t + c_2 t^2 + c_3 t^3 + c_4 t^4 + c_5 t^5$$

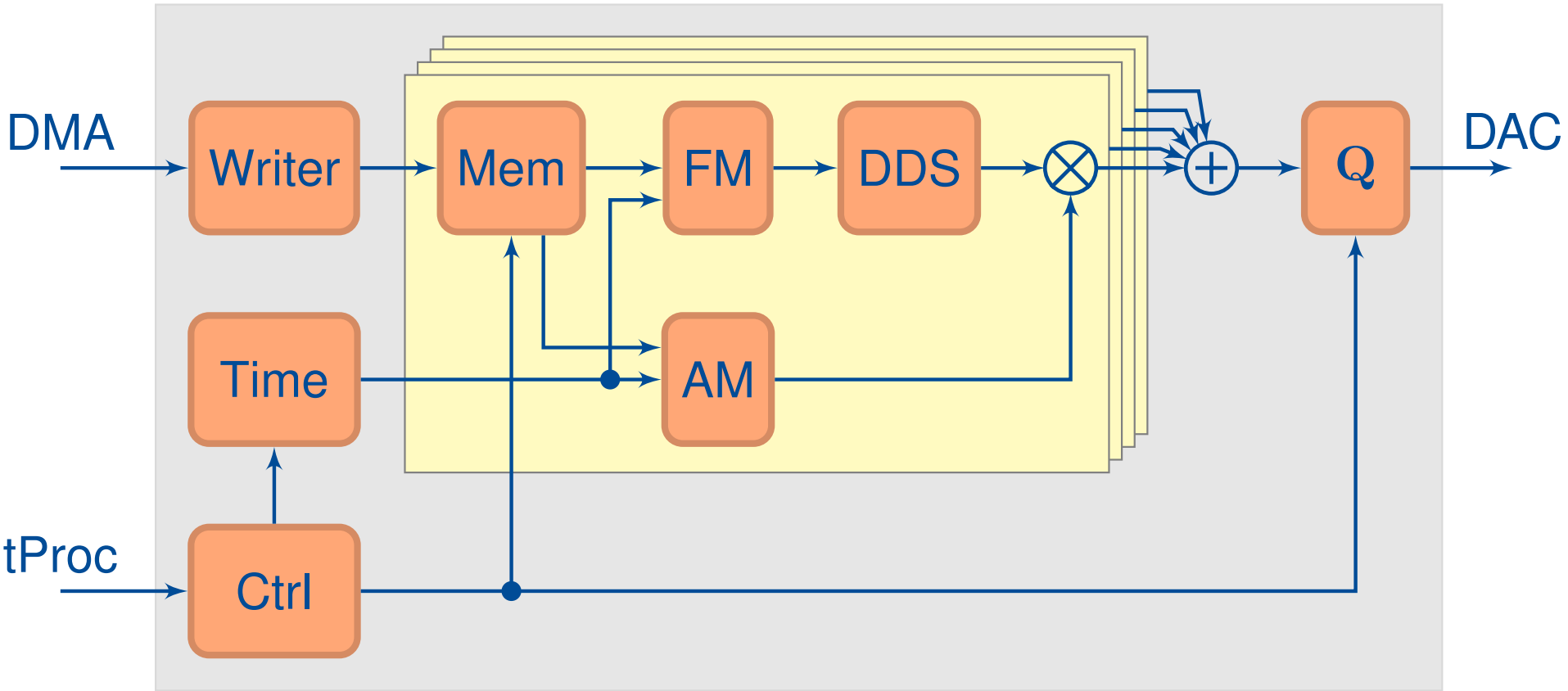
- Third order polynomial function for amplitude modulation:

$$a[t] = a_0 + a_1 t + a_2 t^2 + a_3 t^3$$

- Gain for modulation scaling.
- tProc control for sweep start and control.
- Independent parameter memory per DDS instance.
- 32 independent DDS instances.
- Last DDS AM output routed to DAC.

AMO Generator V4 Block Diagram

- 32 independent DDSs: FM, AM and Memory.
- Parameter memory: configurable size (256 actual).
- tProc control: address, wait, quantization and ctrl.
- ctrl field: phase reset, saturation logic, DDS 31 disable.



Generator Control

- Parameter memory holds sweep coefficients.
- Each memory location stores a set.
- The total number of sets can be controlled by Firmware.

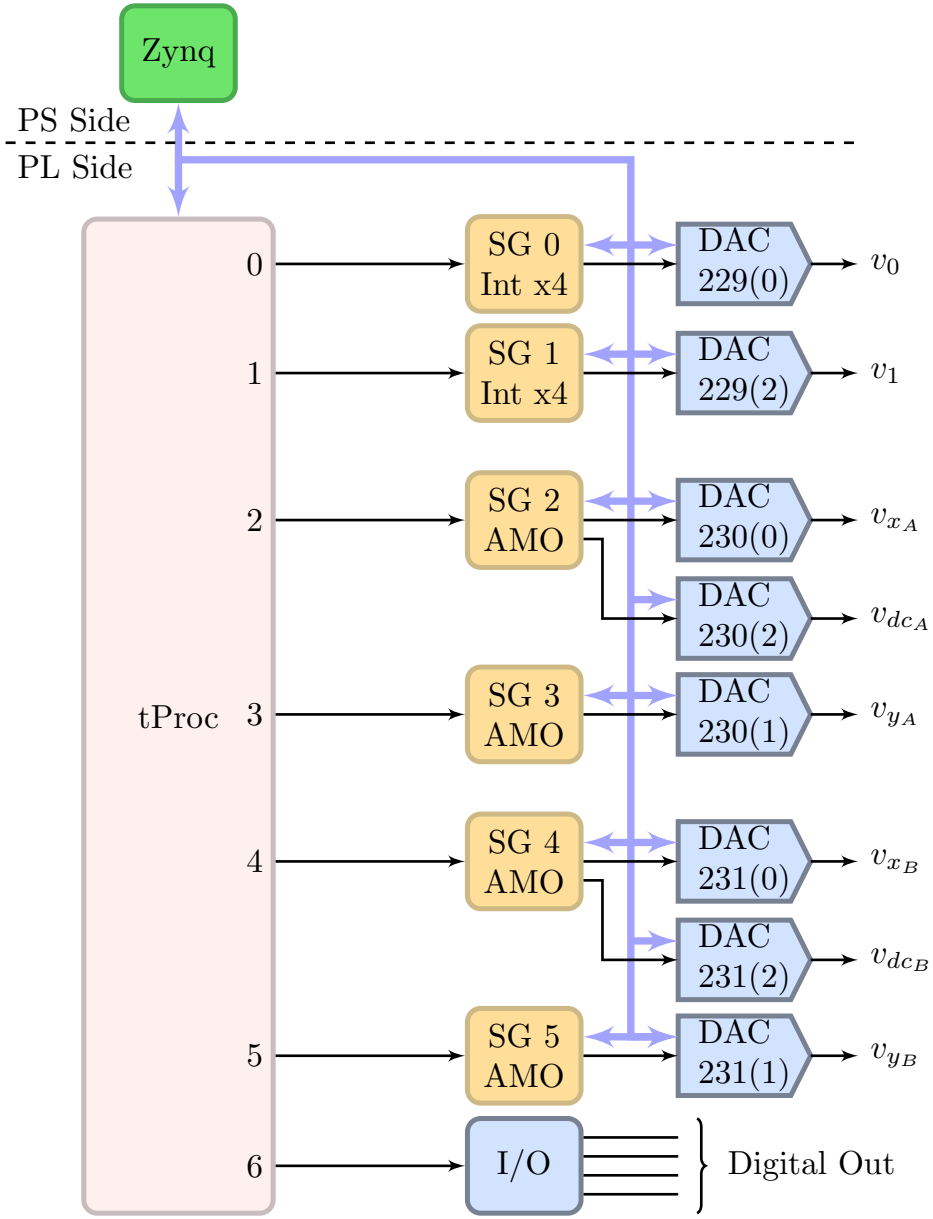
	8	18	16	16	16	16	16	18	18	18	18	18	18	18
0	CTRL	POFF	AM_G	AM_C3	AM_C2	AM_C1	AM_C0	FM_G	FM_C5	FM_C4	FM_C3	FM_C2	FM_C1	FM_C0
1	CTRL	POFF	AM_G	AM_C3	AM_C2	AM_C1	AM_C0	FM_G	FM_C5	FM_C4	FM_C3	FM_C2	FM_C1	FM_C0
2	CTRL	POFF	AM_G	AM_C3	AM_C2	AM_C1	AM_C0	FM_G	FM_C5	FM_C4	FM_C3	FM_C2	FM_C1	FM_C0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

- The tProc pushed waveforms in real time.
- Parameters: set number, duration and quantization.

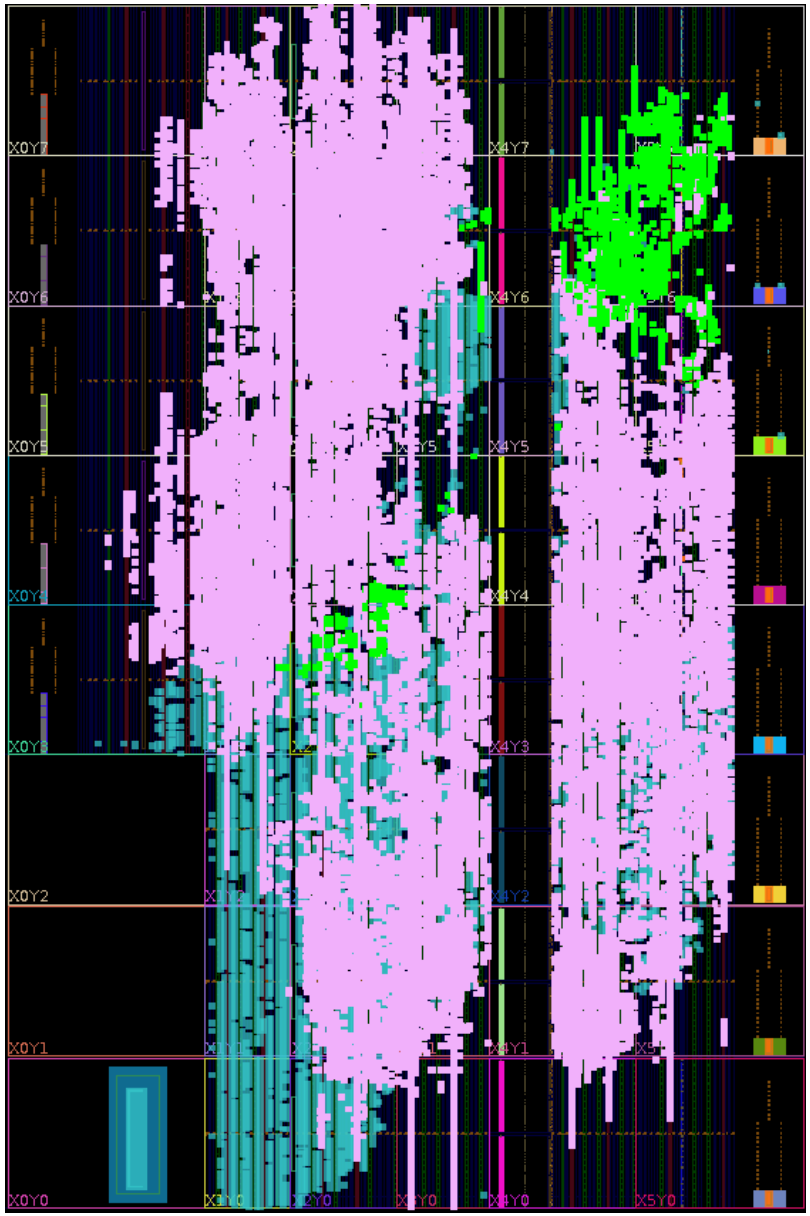
8	8	32	32
qsel	ctrl	wait	addr

`ctrl[0]:phase reset, ctrl[1]:saturation, ctrl[2]:dds 31 enable`

Test Firmware

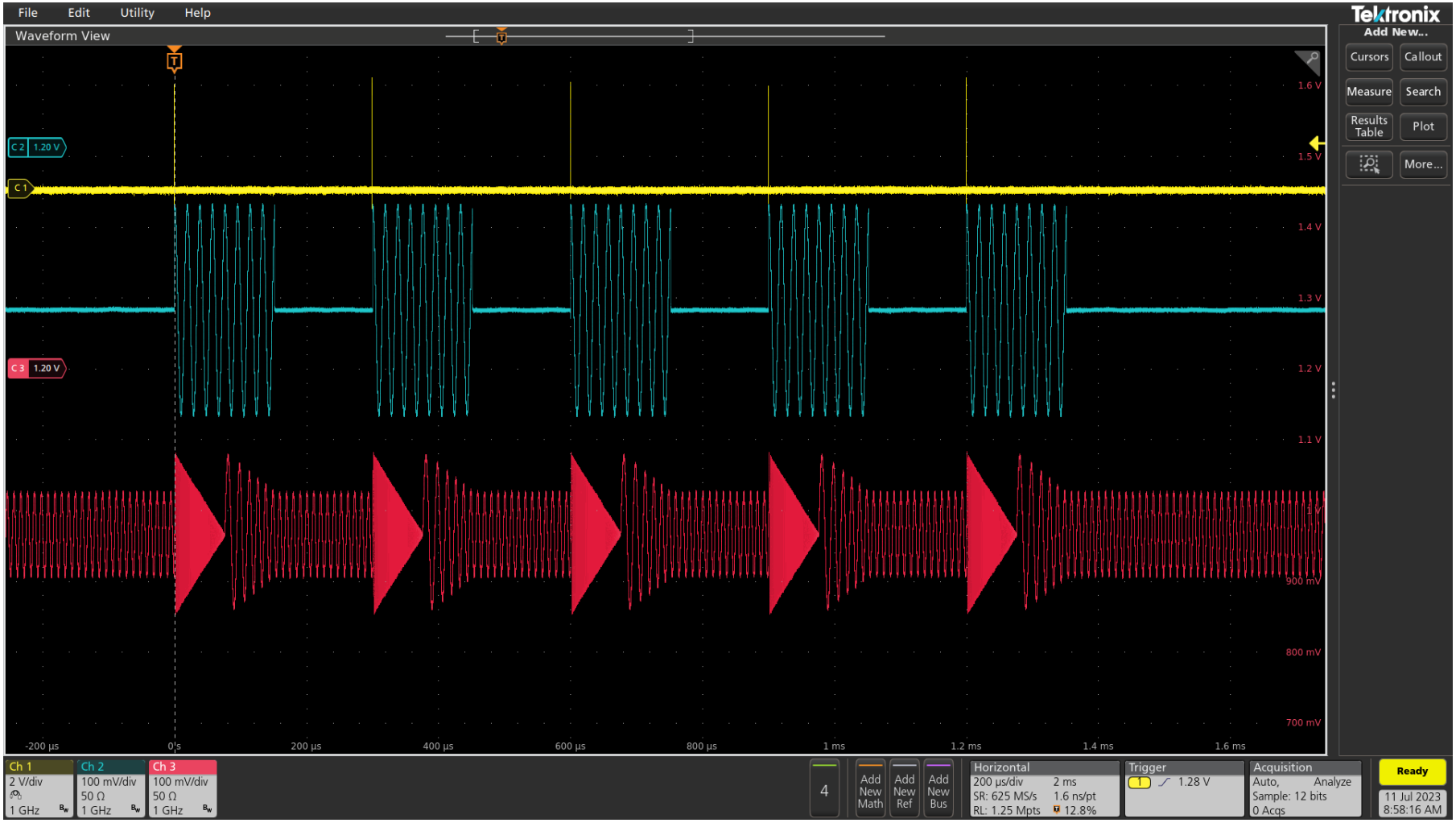


FPGA Resource Usage



- axis_clock_converter_2 (d_1_axis_clock_converter_2_0)
- axis_clock_converter_3 (d_1_axis_clock_converter_3_0)
- axis_set_reg_0 (d_1_axis_set_reg_0_0)
- axis_sg_int4_v1_0 (d_1_axis_sg_int4_v1_0_0)
- axis_sg_int4_v1_1 (d_1_axis_sg_int4_v1_1_0)
- axis_signal_gen_amo_0 (d_1_axis_signal_gen_amo_0_0)
- axis_signal_gen_amo_1 (d_1_axis_signal_gen_amo_1_0)
- axis_signal_gen_amo_2 (d_1_axis_signal_gen_amo_2_0)
- axis_signal_gen_amo_3 (d_1_axis_signal_gen_amo_3_0)
- axis_switch_gen (d_1_axis_switch_gen_0)
- axis_switch_gen_amo (d_1_axis_switch_gen_amo_0)
- axis_tproc64x32_x8_0 (d_1_axis_tproc64x32_x8_0_0)
- clk_tproc (d_1_clk_tproc_0)

Scope Capture: modulation



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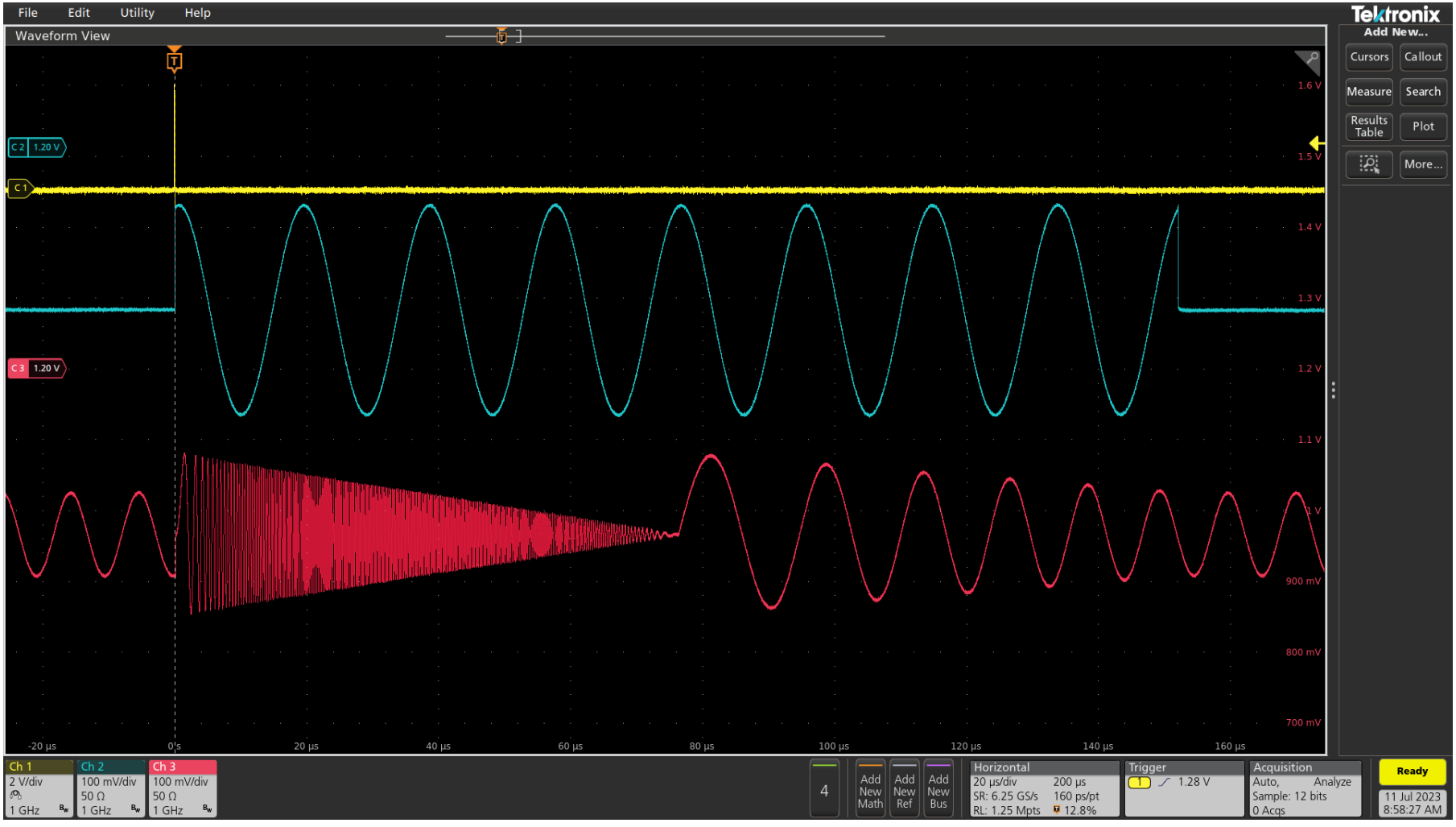
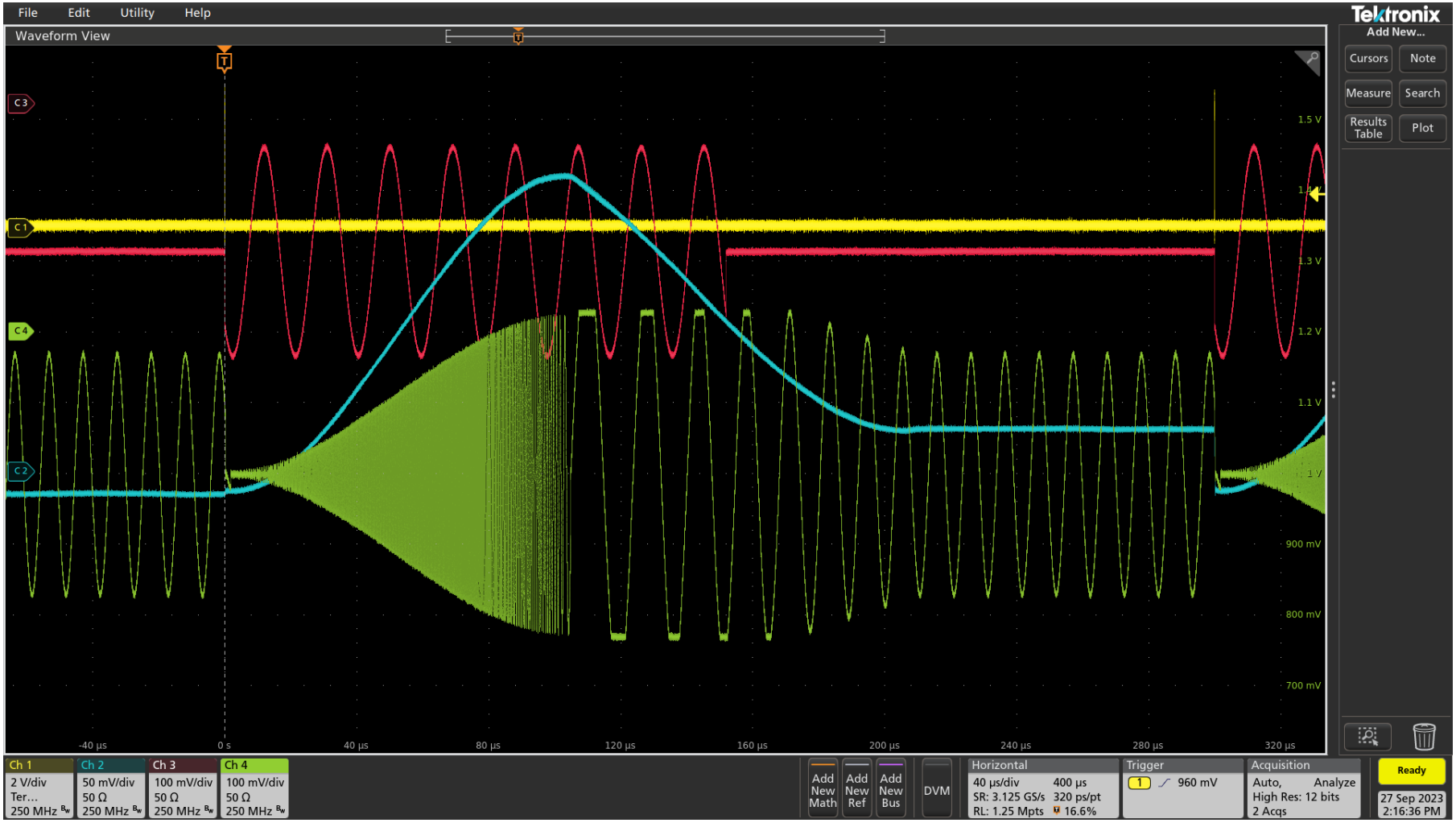
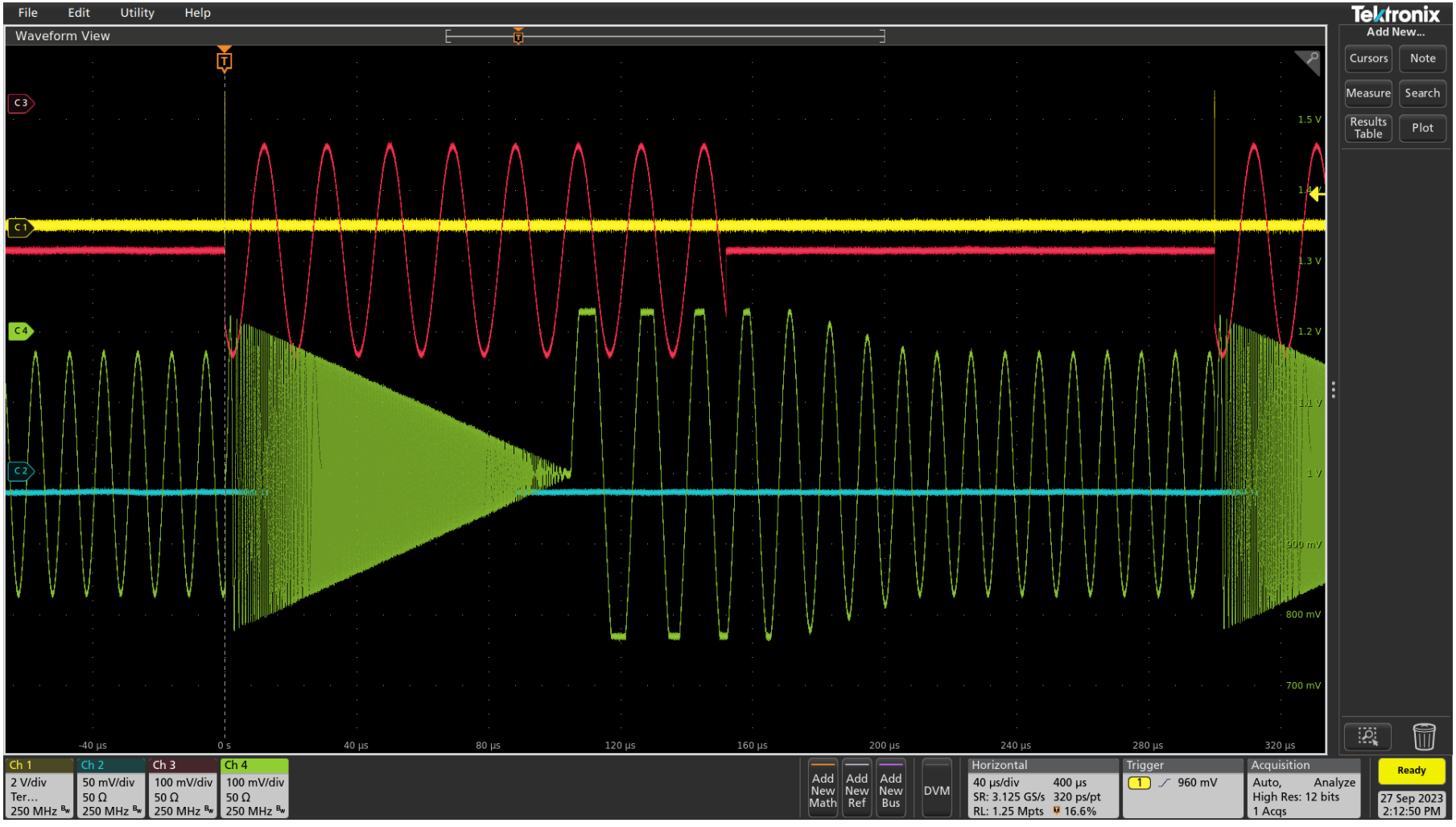
Scope Capture: modulation



Scope Capture: auxiliary output



Scope Capture: saturation logic



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