Aim

To realize logic gates with the help of universal NAND gates, and to construct a full adder

Apparatus

Breadboard, NAND gates (IC 7400), NOR Gates (IC7402), LEDs, connecting wires

Theory

NAND gate is a combination of two logic gates: AND followed by NOT. Its output is therefore complement of the output of an AND gate. This gate can have minimum two inputs, and has one output. The NAND (and NOR) gate is referred to as a 'universal gate' because all logic functions: AND, OR, NOT, X-OR, X-NOR, etc. can be realized by using NAND (or NOR gates) alone.

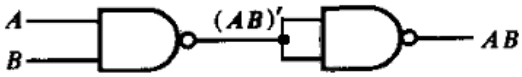
NAND gate as NOT gate

A NOT produces complement of the input, and can have only one input. By tying the inputs of a NAND gate together, it works as a NOT gate: Y = (A.A)' = (A)'

NOT (inverter)

NAND gate as AND gate

A NAND produces complement of AND gate. Connecting a NAND in series with its NOT version produces AND gate. Y = ((A.B)')' = (A.B)



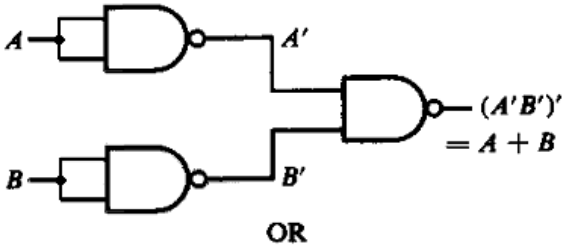
AND

NAND gate as OR gate

From DeMorgan's theorems: (A.B)' = A' + B'

=> (A'.B')' = A'' + B'' = A + B

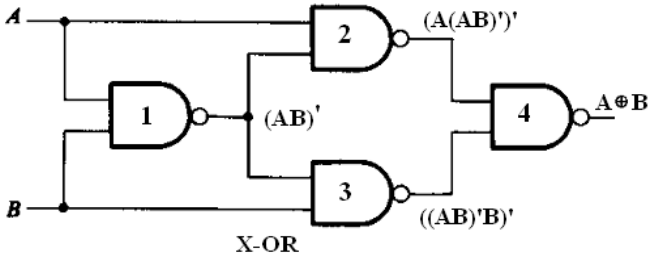
Therefore, by giving inverted inputs to a NAND gate, obtain OR operation at output.



OR

NAND gates as XOR gate

The output of a two-input XOR gate is shown by: Y = A'B + AB'. This can be achieved with the logic diagram shown as follows.



X-OR

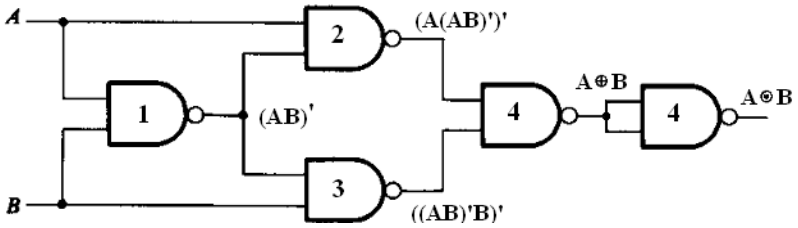
Gate No.	Inputs	Output
1	A, B	(AB)′
2	A, (AB)′	(A (AB)′)′
3	(AB)′, B	(B (AB)′)′
4	(A (AB)′)′, (B (AB)′)′	A′B + AB′

Now the output from Gate 4 is the overall output of the configuration.

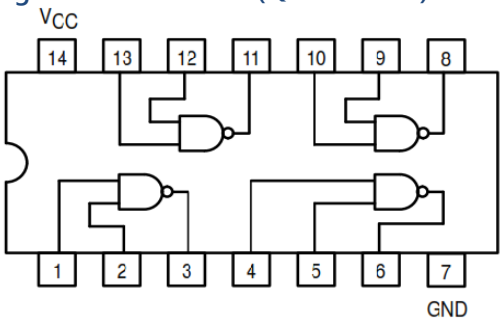
$$
\begin{aligned}
Y &= ((A\,(AB)')'\,(B\,(AB)')')' \\
&= (A(AB)')'' + (B(AB)')'' \\
&= (A(AB)') + (B(AB)') \\
&= (A(A' + B')) + (B(A' + B')) \\
&= (AA' + AB') + (BA' + BB') \\
&= (\,0 + AB' + BA' + 0\,) \\
&= AB' + BA'
\end{aligned}
$$

NAND gates as X-NOR gate

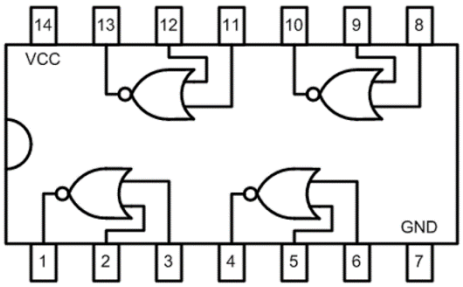
XNOR gate is an XOR gate followed by a NOT gate. Giving the output of X-OR gate to a NOT gate would therefore result in an XNOR gate: Y = AB+ A′B′



Pin Configuration of IC 7400 (Quad-NAND) and IC 7402 (Quad-NOR) are shown as follows:



IC 7400

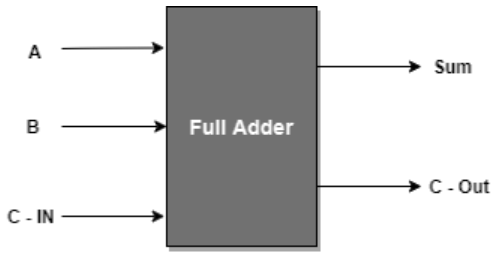


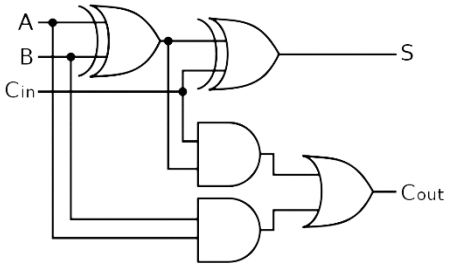
IC 7402

(Use V_{CC} = 5V).

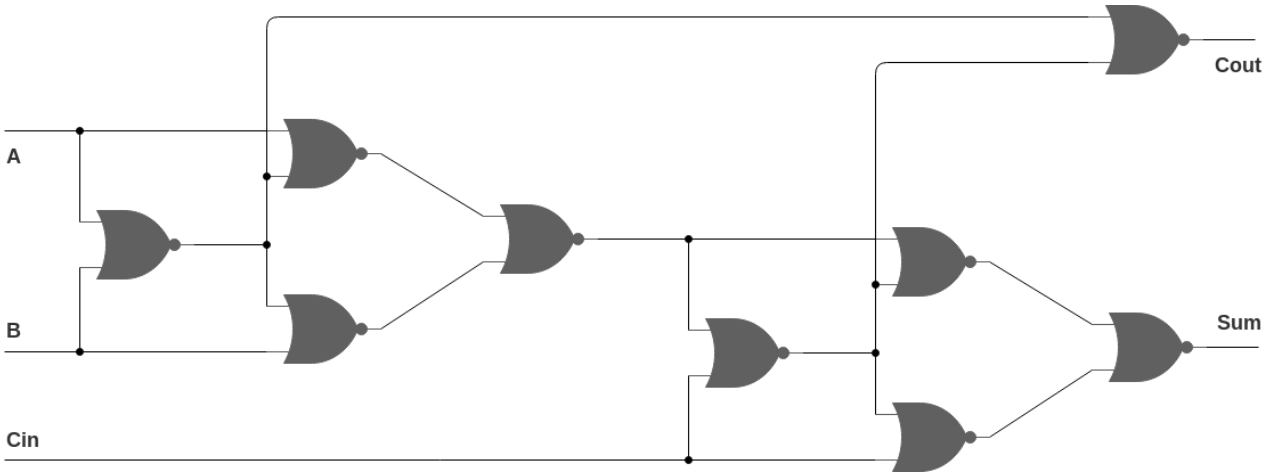
Full Adder

The full adder accepts two inputs bits and an input carry, and generates a sum output and an output carry. The first two inputs are A and B and the third input is an input carry, designated as C_{in}.





Full adder Circuit



Full-adder using NOR Gates

INPUTS			OUTPUTS	
A	B	C_{in}	SUM	CARRY $_{OUT}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table for a Full Adder

Experiment

These circuits are to be verified with LEDs or output voltage level measured using DMM. Logic Level 0 is denoted by low voltage (0V) and Logic Level 1 is denoted by high voltage (V_{CC}), here 5V.