1. Description

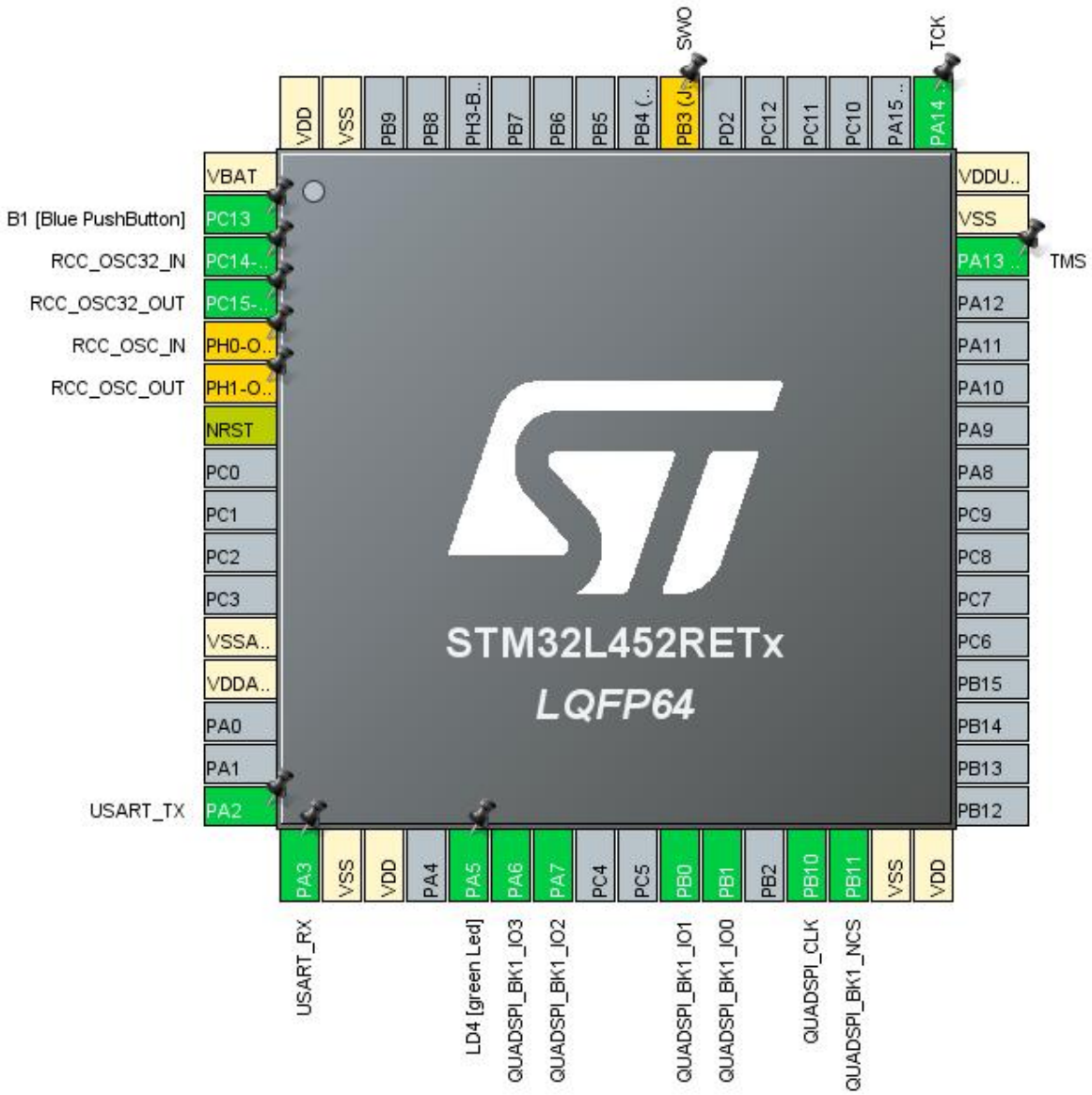
1.1. Project

Project Name	STM32L452_QSPI_SRAM
Board Name	NUCLEO-L452RE
Generated with:	STM32CubeMX 5.6.1
Date	01/15/2021

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x2
MCU name	STM32L452RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



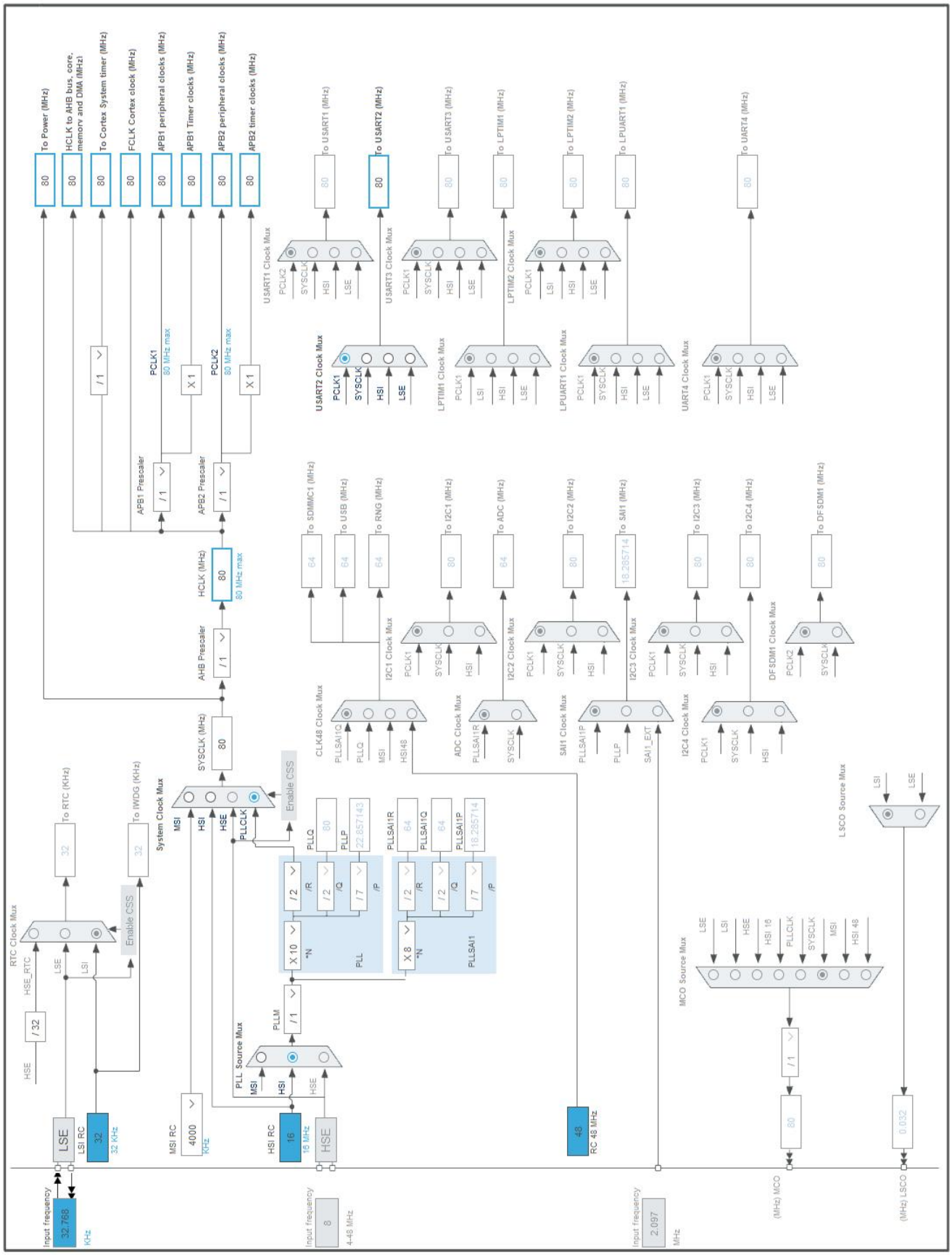
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN (PH0) *	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT (PH1) *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 **	I/O	GPIO_Output	LD4 [green Led]
22	PA6	I/O	QUADSPI_BK1_IO3	
23	PA7	I/O	QUADSPI_BK1_IO2	
26	PB0	I/O	QUADSPI_BK1_IO1	
27	PB1	I/O	QUADSPI_BK1_IO0	
29	PB10	I/O	QUADSPI_CLK	
30	PB11	I/O	QUADSPI_BK1_NCS	
31	VSS	Power		
32	VDD	Power		
46	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDDUSB	Power		
49	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 (JTDO/TRACESWO) *	I/O	SYS_JTDO-SWO	SWO
63	VSS	Power		
64	VDD	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32L452_QSPI_SRAM
Project Folder	D:\30_ARM_WS\workspace\STM32L452_QSPI_SRAM
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_L4 V1.15.1

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x2
MCU	STM32L452RETx
Datasheet	029968_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

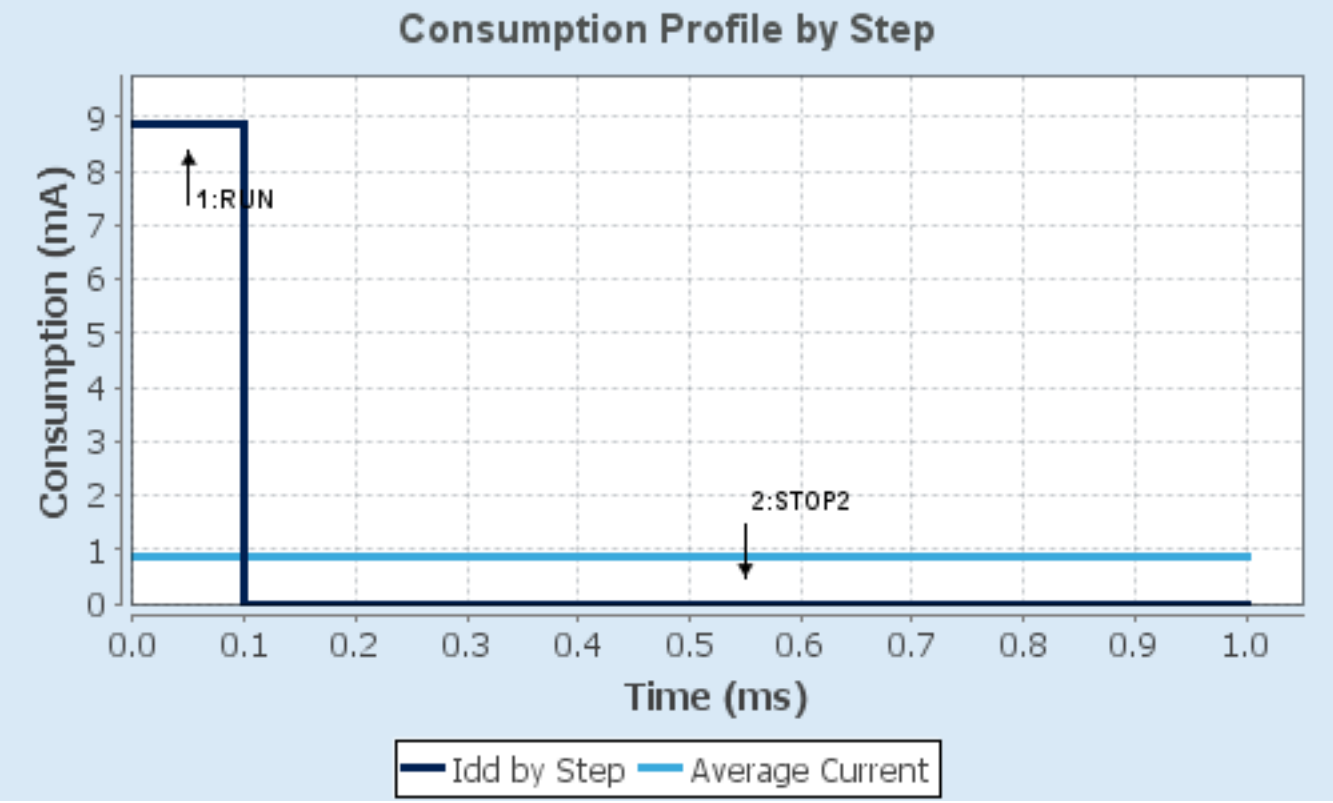
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	8.85 mA	2.05 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.78	105
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	886.84 µA
Battery Life	5 months, 6 days, 23 hours	Average DMIPS	100.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
9
8
7
6
5
4
3
2
1
0
1:RUN
2:STOP2
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. GPIO

7.2. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.2.1. Parameter Settings:

General Parameters:

Clock Prescaler	**1 ***
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	**19 ***
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.3. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. USART2

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
QUADSPI	PA6	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA7	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB0	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB1	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB11	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USART_RX
Single Mapped Signals	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PB3 (JTDO/TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	SWO

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD4 [green Led]

8.2. DMA configuration

DMA request	Stream	Direction	Priority
QUADSPI	DMA1_Channel5	Peripheral To Memory	**Very High ***

QUADSPI: DMA1_Channel5 DMA request Settings:

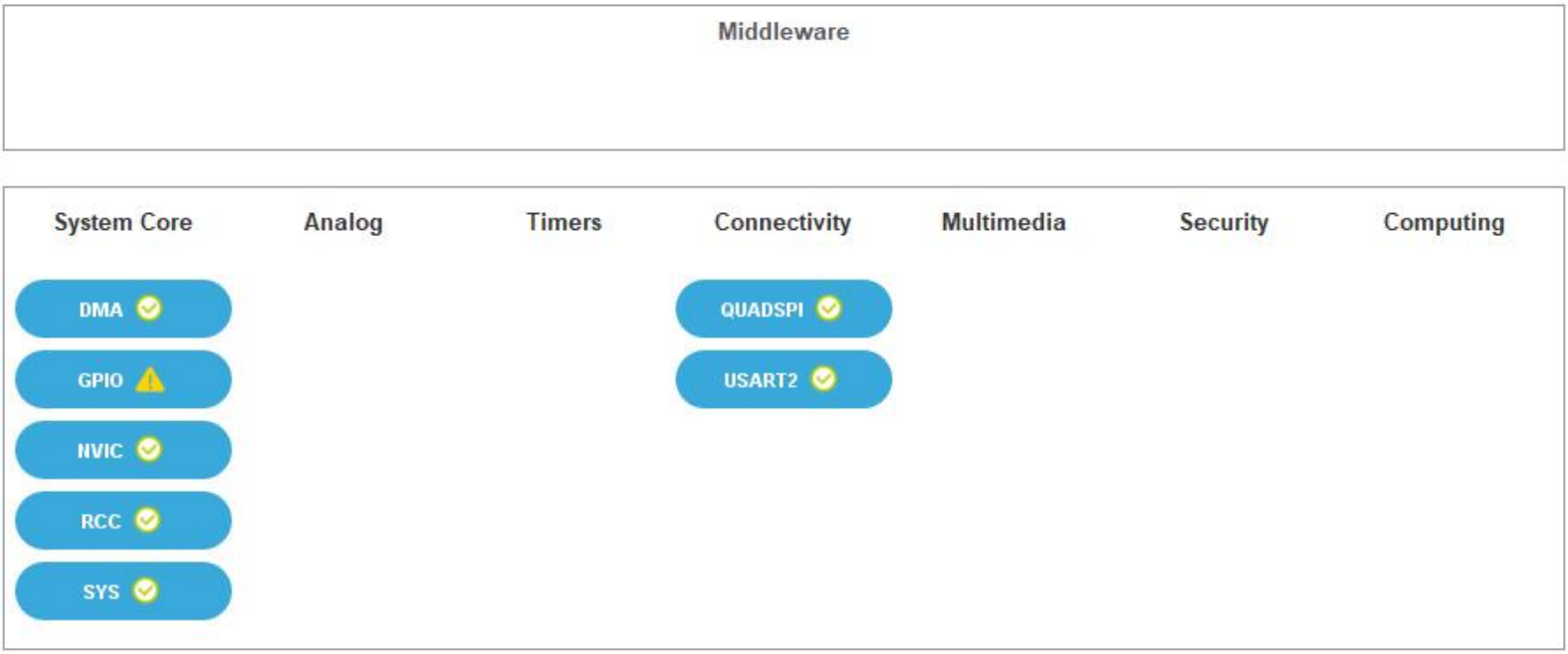
Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel5 global interrupt	true	0	0
QUADSPI global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		

*** User modified value**

9. Predefined Views - Category view : Current



10. Software Pack Report