1. Description

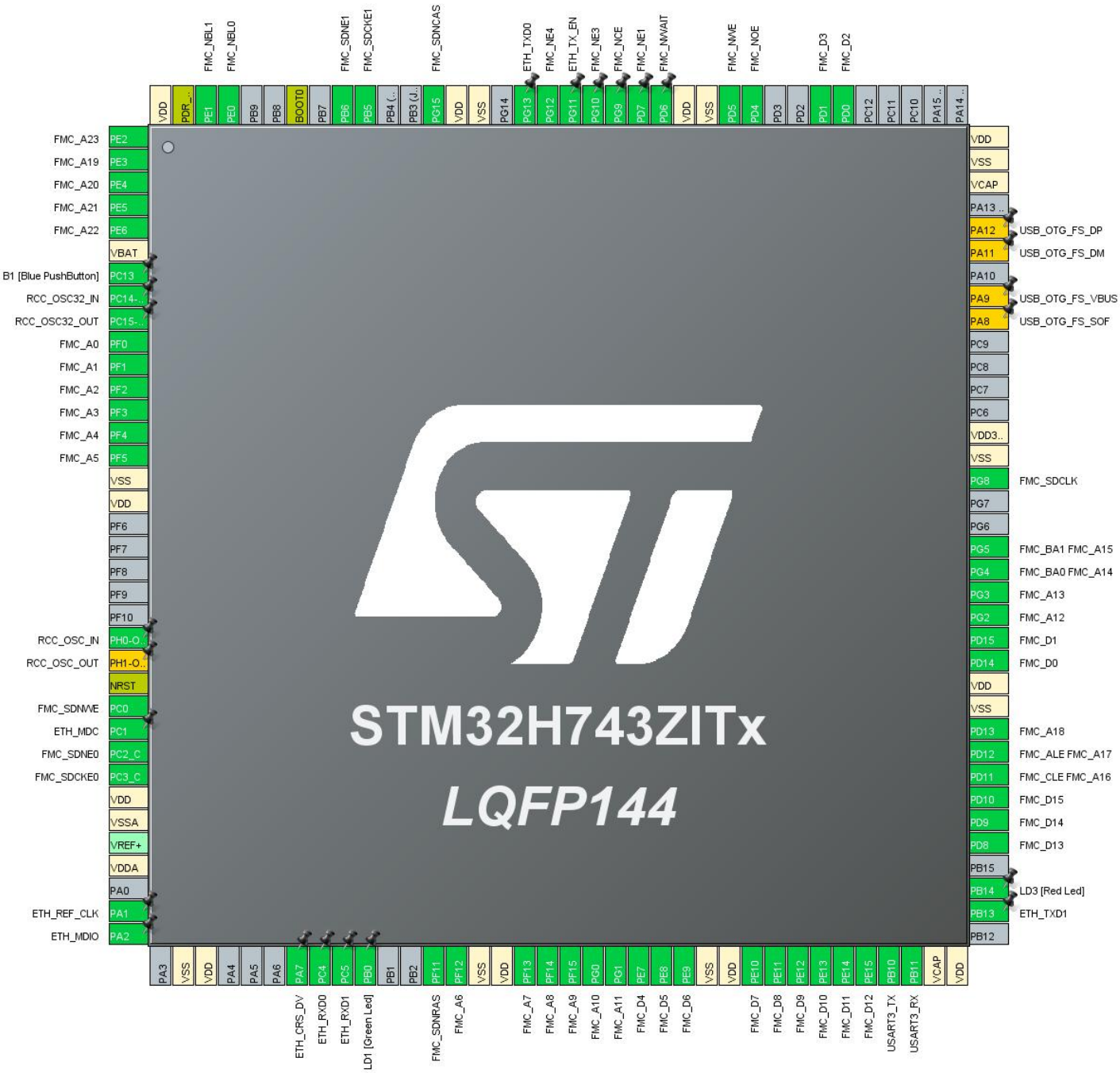
1.1. Project

Project Name	STM32H743_MEMORY_SDRAM
Board Name	NUCLEO-H743ZI2
Generated with:	STM32CubeMX 5.6.1
Date	09/20/2020

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	FMC_A23	
2	PE3	I/O	FMC_A19	
3	PE4	I/O	FMC_A20	
4	PE5	I/O	FMC_A21	
5	PE6	I/O	FMC_A22	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	B1 [Blue PushButton]
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1) **	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	FMC_SDNWE	
27	PC1	I/O	ETH_MDC	
28	PC2_C	I/O	FMC_SDNE0	
29	PC3_C	I/O	FMC_SDCKE0	
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
38	VSS	Power		
39	VDD	Power		
43	PA7	I/O	ETH_CRS_DV	
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	

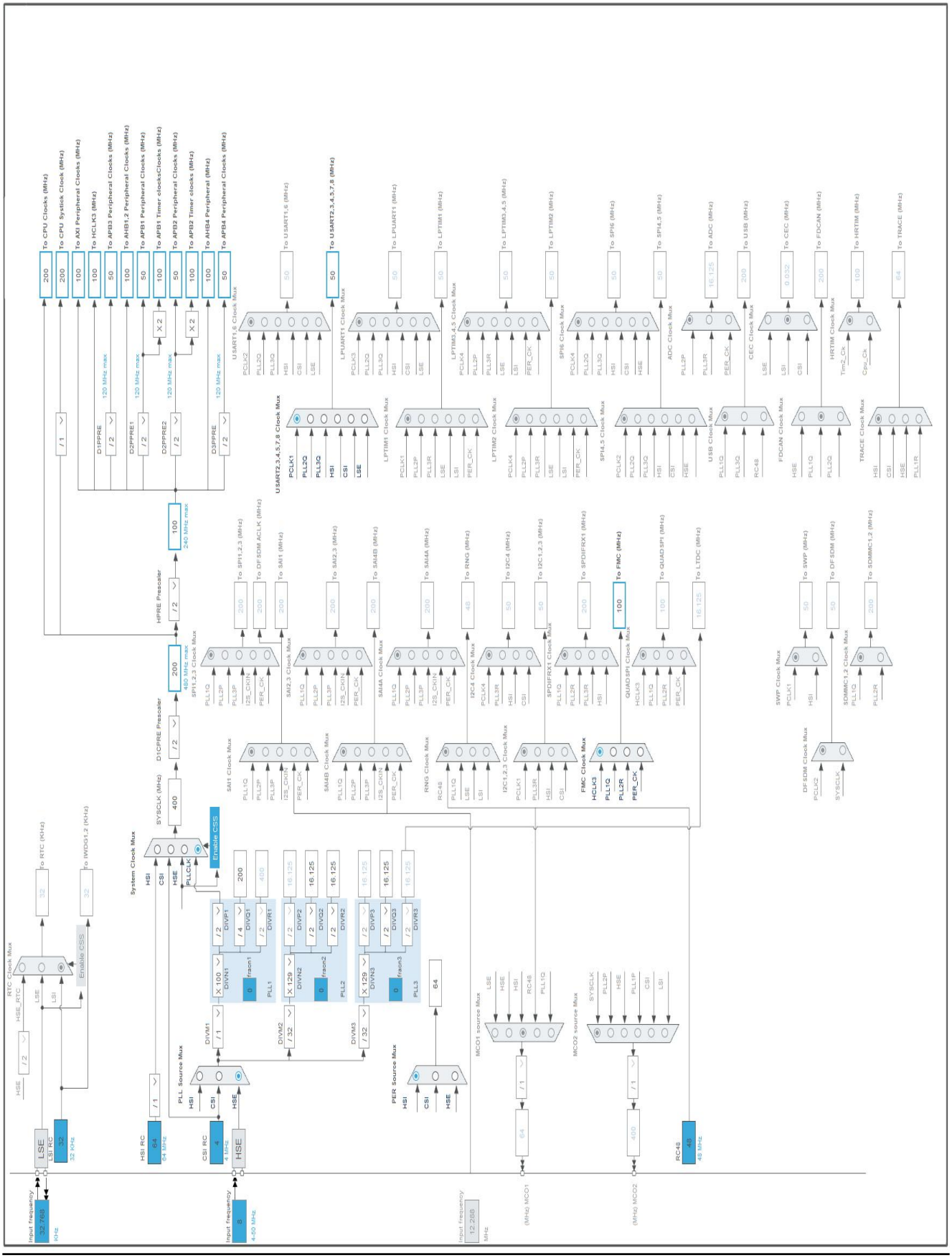
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
46	PB0 *	I/O	GPIO_Output	LD1 [Green Led]
49	PF11	I/O	FMC_SDNRAS	
50	PF12	I/O	FMC_A6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FMC_A7	
54	PF14	I/O	FMC_A8	
55	PF15	I/O	FMC_A9	
56	PG0	I/O	FMC_A10	
57	PG1	I/O	FMC_A11	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10	I/O	USART3_TX	
70	PB11	I/O	USART3_RX	
71	VCAP	Power		
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	
75	PB14 *	I/O	GPIO_Output	LD3 [Red Led]
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
80	PD11	I/O	FMC_CLE, FMC_A16	
81	PD12	I/O	FMC_ALE, FMC_A17	
82	PD13	I/O	FMC_A18	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
87	PG2	I/O	FMC_A12	
88	PG3	I/O	FMC_A13	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
89	PG4	I/O	FMC_BA0, FMC_A14	
90	PG5	I/O	FMC_BA1, FMC_A15	
93	PG8	I/O	FMC_SDCLK	
94	VSS	Power		
95	VDD33_USB	Power		
100	PA8 **	I/O	USB_OTG_FS_SOF	
101	PA9 **	I/O	USB_OTG_FS_VBUS	
103	PA11 **	I/O	USB_OTG_FS_DM	
104	PA12 **	I/O	USB_OTG_FS_DP	
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
118	PD4	I/O	FMC_NOE	
119	PD5	I/O	FMC_NWE	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	FMC_NWAIT	
123	PD7	I/O	FMC_NE1	
124	PG9	I/O	FMC_NCE	
125	PG10	I/O	FMC_NE3	
126	PG11	I/O	ETH_TX_EN	
127	PG12	I/O	FMC_NE4	
128	PG13	I/O	ETH_TXD0	
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	FMC_SDNCAS	
135	PB5	I/O	FMC_SDCKE1	
136	PB6	I/O	FMC_SDNE1	
138	BOOT0	Boot		
141	PE0	I/O	FMC_NBL0	
142	PE1	I/O	FMC_NBL1	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32H743_MEMORY_SDRAM
Project Folder	D:\30_ARM_WS\workspace\STM32H743_MEMORY_SDRAM
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_H7 V1.7.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743ZITx
Datasheet	DS12110_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

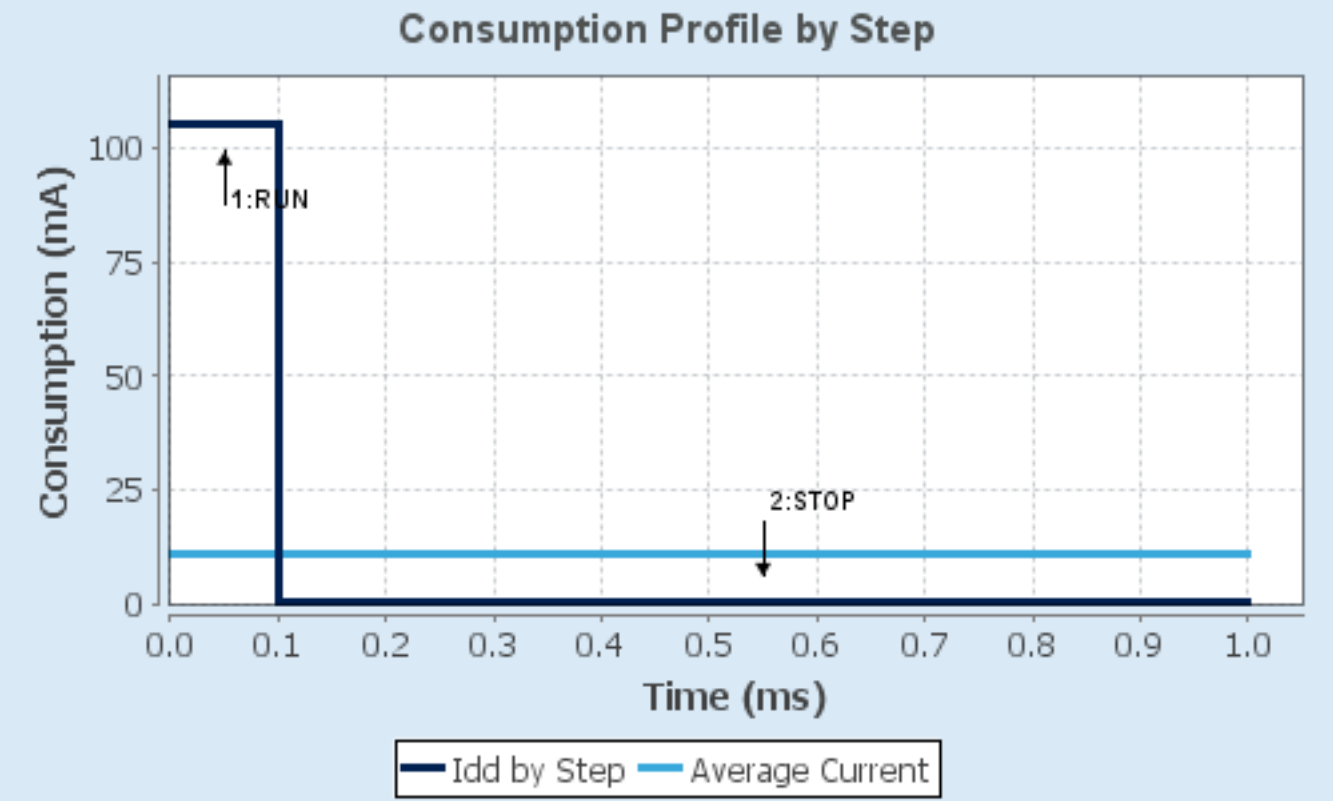
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS1: Scale1-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DSTANDBY	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	FLASH_A	NA
CPU Frequency	400 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON Cache-ON	Flash-LP
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	105 mA	170 µA
Duration	0.1 ms	0.9 ms
DMIPS	856.0	0.0
Ta Max	111.14	124.98
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	10.65 mA
Battery Life	2 days, 10 hours	Average DMIPS	856.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.2. ETH

Mode: RMII

7.2.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30040060 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30040000 ***
Rx Buffers Address	**0x30040200 ***
Rx Buffers Length	1524

7.3. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: SRAM

Address: 19 bits

Data: 16 bits

Byte enable: set

NOR Flash/PSRAM/SRAM/ROM/LCD 2

Chip Select: NE3
Memory type: SRAM
Address: 19 bits
Data: 16 bits
Byte enable: set
NOR Flash/PSRAM/SRAM/ROM/LCD 3
Chip Select: NE4
Memory type: NOR Flash
Address: 24 bits
Data: 16 bits
Wait: Asynchronous
NAND Flash 1
Chip Select: set
Data/Address: 8 bits
Ready or busy: NWAIT
SDRAM 1
Clock and chip enable: SDCKE0+SDNE0
Internal bank number: 4 banks
Address: 13 bits
Data: 16 bits
Byte enable: set
SDRAM 2
Clock and chip enable: SDCKE1+SDNE1
Internal bank number: 4 banks
Address: 13 bits
Data: 16 bits
Byte enable: set

7.3.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	SRAM
Bank	Bank 1 NOR/PSRAM 1
Write operation	**Enabled ***
Write FIFO	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	

	2 *
Data setup time in HCLK clock cycles	**1 ***
Bus turn around time in HCLK clock cycles	**3 ***

7.3.2. Bank Mapping:

Mapping parameters:

FMC bank mapping	Default mapping

7.3.3. NOR/PSRAM 2:

NOR/PSRAM control:

Memory type	SRAM
Bank	Bank 1 NOR/PSRAM 3
Write operation	**Enabled ***
Write FIFO	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	**2 ***
Data setup time in HCLK clock cycles	**1 ***
Bus turn around time in HCLK clock cycles	**3 ***

7.3.4. NOR/PSRAM 3:

NOR/PSRAM control:

Memory type	NOR Flash
Bank	Bank 1 NOR/PSRAM 4
Write operation	**Enabled ***
Write FIFO	Enabled
Extended mode	**Enabled ***
Wait signal polarity	Low polarity

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	**7 ***
Data setup time in HCLK clock cycles	**2 ***
Bus turn around time in HCLK clock cycles	**3 ***
Access mode	B

NOR/PSRAM timing for write accesses:

Extended address setup time	

	0 *
Extended data setup time	**3 ***
Extended bus turn around time	**3 ***
Extended access mode	B

7.3.5. NAND 1:

NAND control:

Bank	NAND bank 3
ECC computation	**Enabled ***
ECC page size	**1024 bytes ***
CLE low to RE low delay in HCLK cycles	**1 ***
ALE low to RE low delay in HCLK cycles	**1 ***

NAND common space timing in HCLK cycles:

Common space setup time	**1 ***
Common space wait time	**2 ***
Common space hold time	**2 ***
Common space Hi-Z time	**2 ***

NAND attribute space timing in HCLK cycles:

Attribute space setup time	**1 ***
Attribute space wait time	**2 ***
Attribute space hold time	**2 ***
Attribute space Hi-Z time	**2 ***

NAND characteristic information:

Page size	**2048 ***
Spare area size	**32 ***
Block size	**64 ***
Block number	**2048 ***
Plane number	**4 ***
Plane size	**512 ***
Extra command enable	Disabled

7.3.6. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	

	9 bits *
Number of row address bits	13 bits
CAS latency	**2 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	**Enabled ***
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**6 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**6 ***
Write recovery time	**3 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

7.3.7. SDRAM 2:

SDRAM control:

Bank	SDRAM bank 2
Number of column address bits	**9 bits ***
Number of row address bits	13 bits
CAS latency	**2 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	**Enabled ***
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**6 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**6 ***
Write recovery time	**3 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

7.4. GPIO

7.5. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

SupplySource	PWR_LDO_SUPPLY
RCC Parameters:	
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32
System Parameters:	
VDD voltage (V)	3.3
Flash Latency(WS)	1 WS (2 CPU cycle)
Power Parameters:	
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
PLL range Parameters:	
PLL1 clock Input range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range

7.6. SYS

Timebase Source: SysTick

7.7. USART3

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:	
Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FMC	PE2	FMC_A23	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE3	FMC_A19	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE4	FMC_A20	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE5	FMC_A21	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE6	FMC_A22	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC2_C	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3_C	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD11	FMC_CLE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD12	FMC_ALE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD13	FMC_A18	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG3	FMC_A13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD6	FMC_NWAIT	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG9	FMC_NCE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG10	FMC_NE3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG12	FMC_NE4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB5	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single	PH1-	RCC_OSC_OUT	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
Mapped Signals	OSC_OUT (PH1)					
	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	USB_OTG_FS_VBUS	n/a	n/a	n/a	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green Led]
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red Led]

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

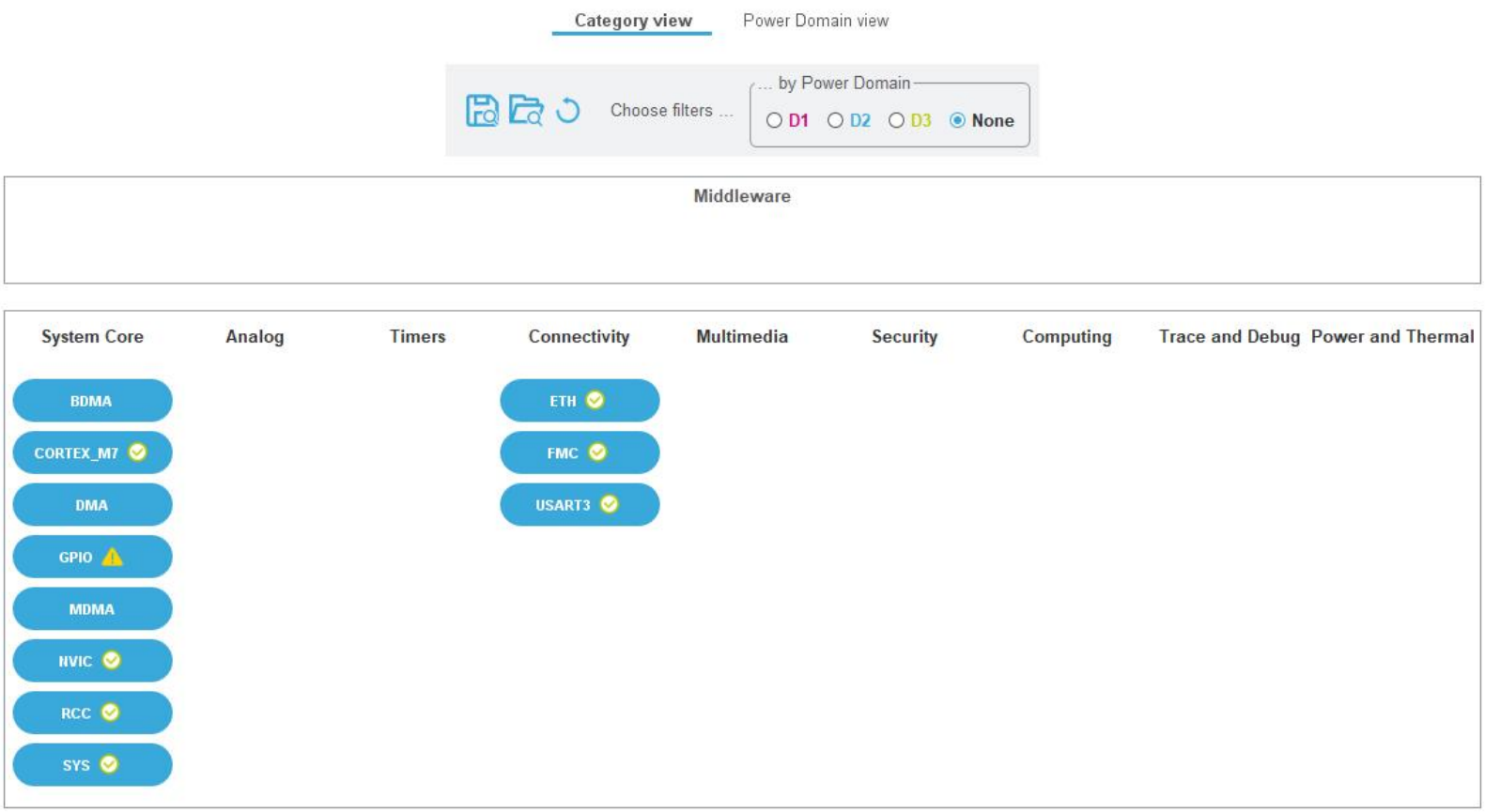
nothing configured in DMA service

8.5. NVIC configuration

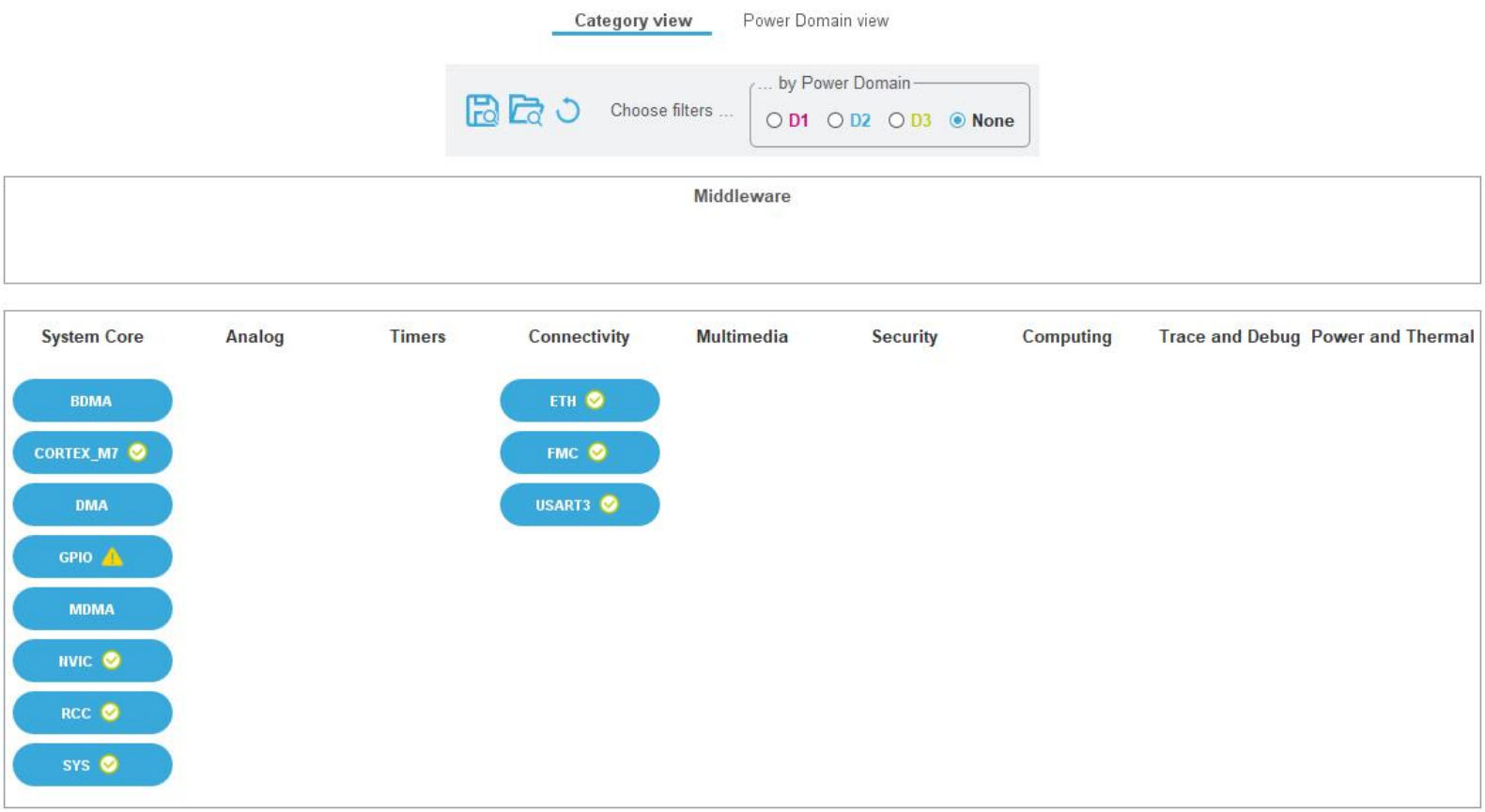
Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART3 global interrupt	unused		
FMC global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

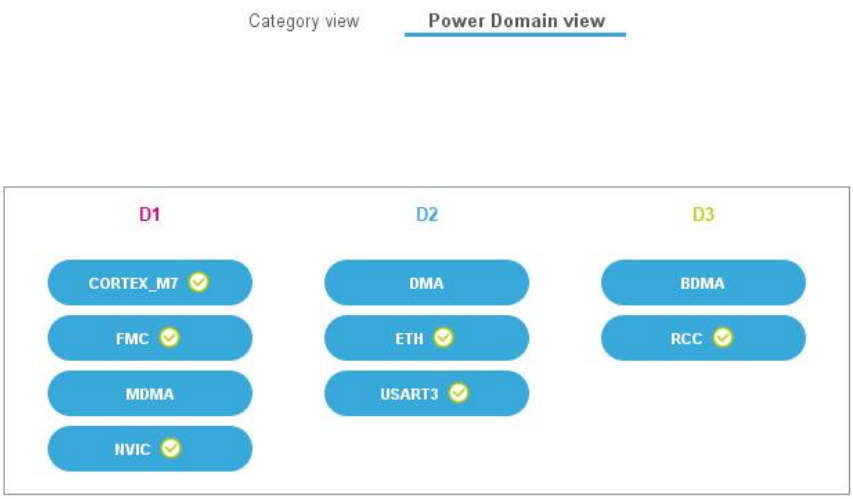
9. Predefined Views - Category view : Current



10. Predefined Views - Category view : Without filters



11. Predefined Views - Power Domain view



12. Software Pack Report