



1. Description

1.1. Project

Project Name	STM32F411_PDM_SPI
Board Name	NUCLEO-F411RE
Generated with:	STM32CubeMX 6.2.1
Date	03/23/2022

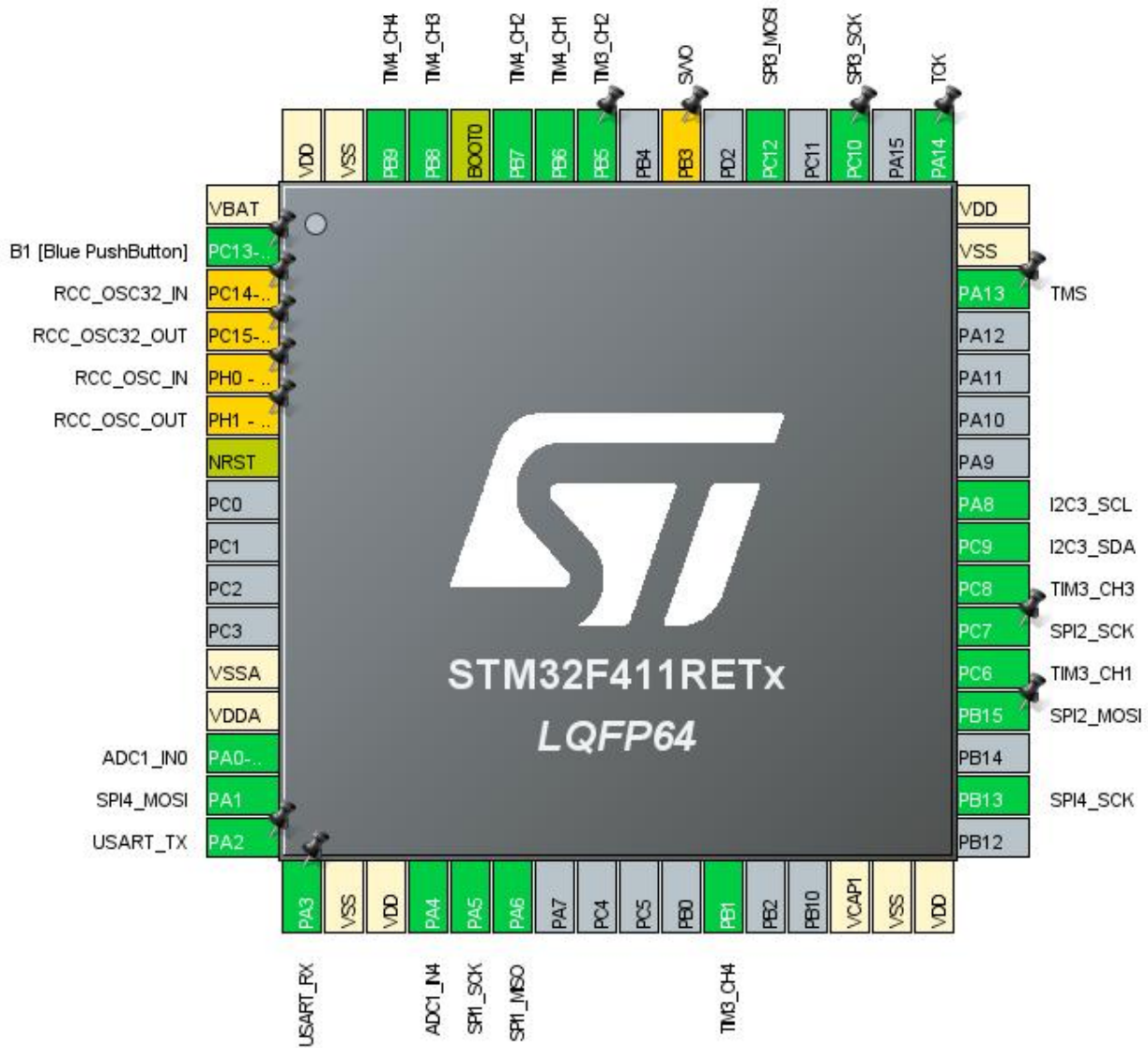
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration



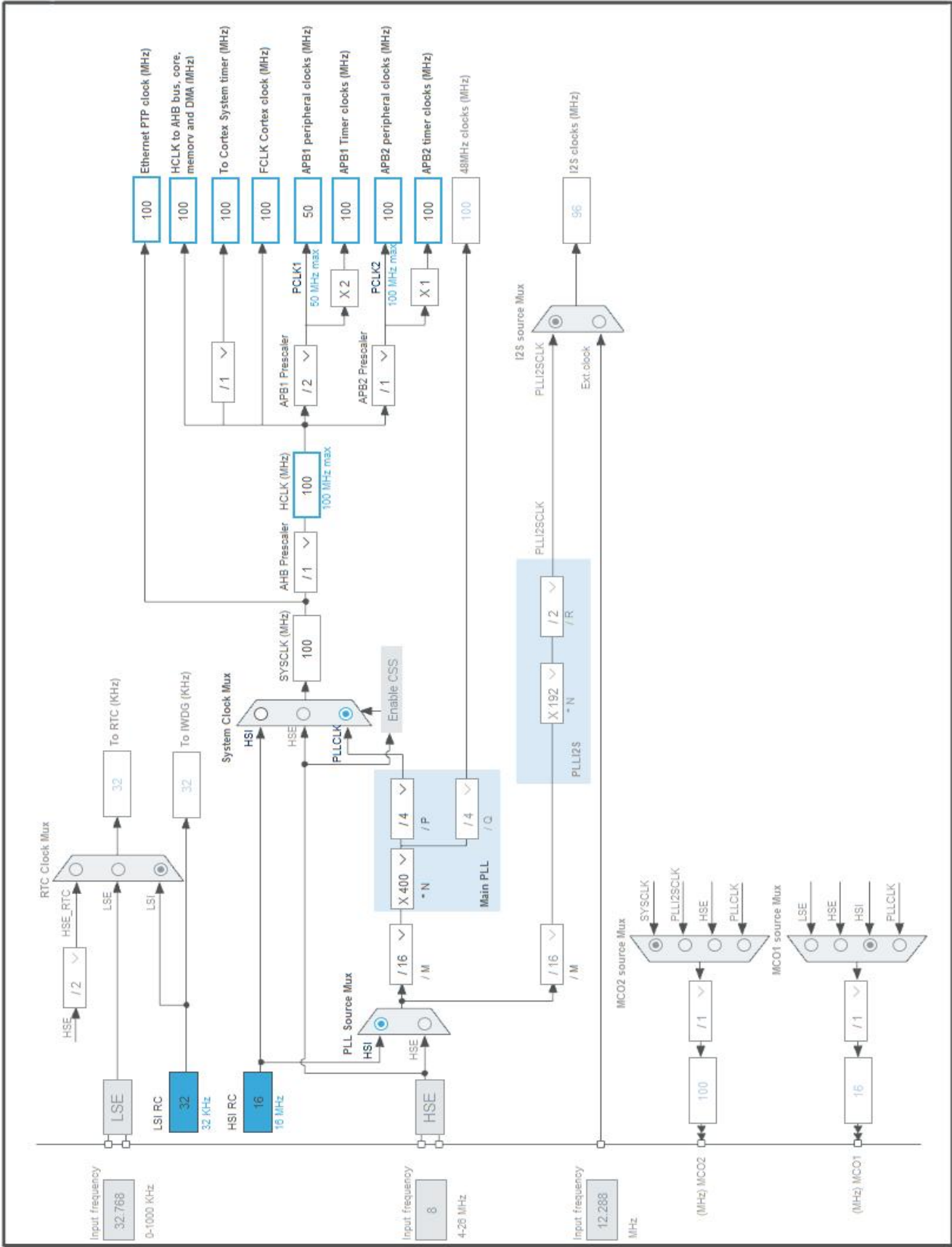
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN *	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT *	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN *	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	
15	PA1	I/O	SPI4_MOSI	
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	
21	PA5	I/O	SPI1_SCK	
22	PA6	I/O	SPI1_MISO	
27	PB1	I/O	TIM3_CH4	
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
34	PB13	I/O	SPI4_SCK	
36	PB15	I/O	SPI2_MOSI	
37	PC6	I/O	TIM3_CH1	
38	PC7	I/O	SPI2_SCK	
39	PC8	I/O	TIM3_CH3	
40	PC9	I/O	I2C3_SDA	
41	PA8	I/O	I2C3_SCL	
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
51	PC10	I/O	SPI3_SCK	
53	PC12	I/O	SPI3_MOSI	
55	PB3 *	I/O	SYS_JTDO-SWO	SWO

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
57	PB5	I/O	TIM3_CH2	
58	PB6	I/O	TIM4_CH1	
59	PB7	I/O	TIM4_CH2	
60	BOOT0	Boot		
61	PB8	I/O	TIM4_CH3	
62	PB9	I/O	TIM4_CH4	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32F411_PDM_SPI
Project Folder	C:\Users\MOND\Desktop\Firm
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.1
Application Structure	Basic
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_SPI1_Init	SPI1
5	MX_USART2_UART_Init	USART2
6	MX_SPI2_Init	SPI2
7	MX_SPI3_Init	SPI3
8	MX_SPI4_Init	SPI4
9	MX_TIM3_Init	TIM3
10	MX_TIM4_Init	TIM4
11	MX_ADC1_Init	ADC1

Rank	Function Name	Peripheral Instance Name
12	MX_I2C3_Init	I2C3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411RETx
Datasheet	DS10314_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	1.7

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

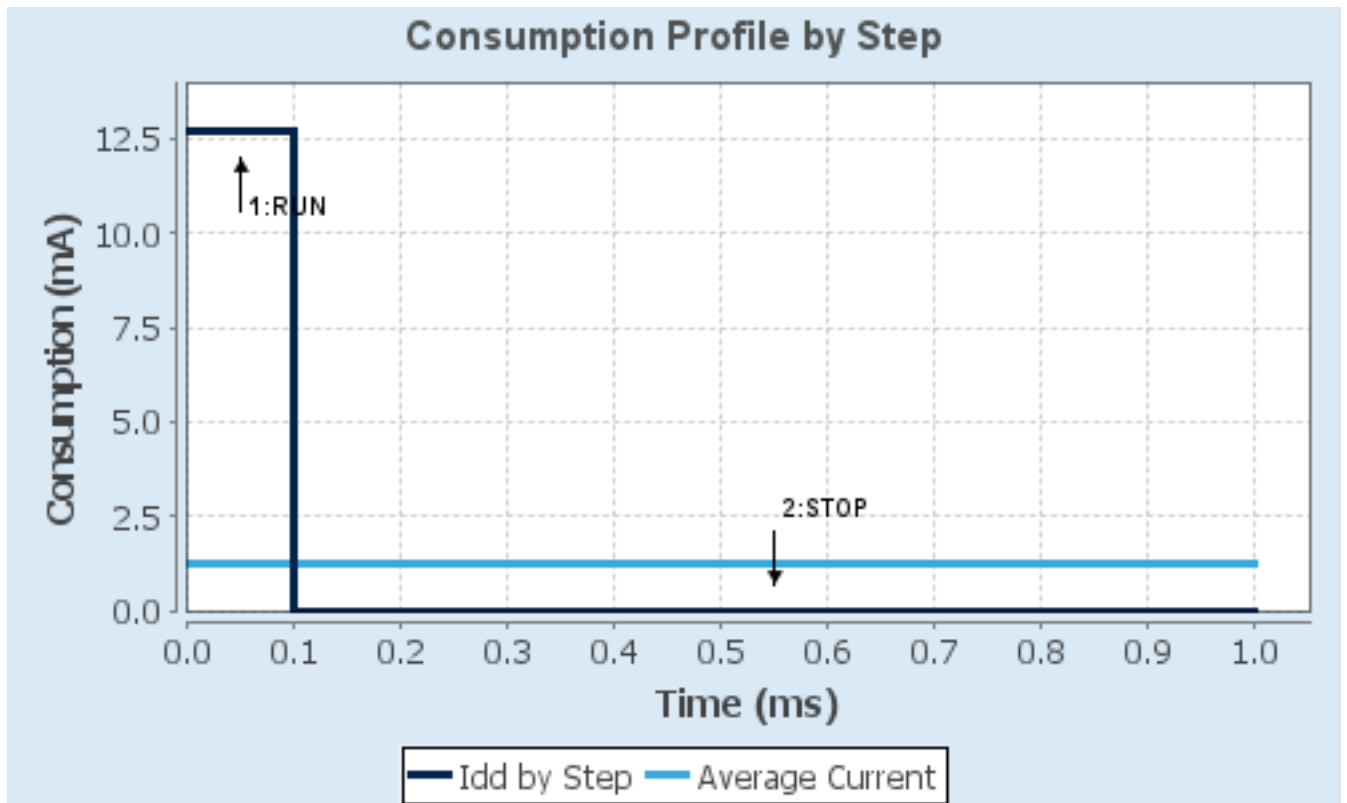
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 μ A
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	103.99	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19 days, 6 hours	Average DMIPS	125.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN0

mode: IN4

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode
ADC_Settings:	
Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0
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WatchDog:

Enable Analog WatchDog Mode	false
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7.2. I2C3

I2C: I2C

7.2.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
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Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0x60 *
General Call address detection	Disabled

7.3. RCC

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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7.4. SPI1

Mode: Receive Only Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	LSB First *

Clock Parameters:

Prescaler (for Baud Rate)	128 *
Baud Rate	781.25 KBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
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NSS Signal Type

Software

7.5. SPI2

Mode: Receive Only Slave

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format

Motorola

Data Size

8 Bits

First Bit

LSB First *

Clock Parameters:

Clock Polarity (CPOL)

Low

Clock Phase (CPHA)

1 Edge

Advanced Parameters:

CRC Calculation

Disabled

NSS Signal Type

Software

7.6. SPI3

Mode: Receive Only Slave

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format

Motorola

Data Size

8 Bits

First Bit

LSB First *

Clock Parameters:

Clock Polarity (CPOL)

Low

Clock Phase (CPHA)

1 Edge

Advanced Parameters:

CRC Calculation

Disabled

NSS Signal Type

Software

7.7. SPI4

Mode: Receive Only Slave

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	LSB First *

Clock Parameters:

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.8. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.9. TIM3

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	2 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1024 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.10. TIM4

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	2 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1024 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
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Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.11. USART2

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	Very High *	
	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	Very High *	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI2	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC7	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI4	PA1	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB13	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM3	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down		USART_TX

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					Very High *	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART_RX
Single Mapped Signals	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13-ANTI_TAMP	GPIO_EXTI13	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_RX	DMA2_Stream0	Peripheral To Memory	Very High *
SPI2_RX	DMA1_Stream3	Peripheral To Memory	High *
SPI3_RX	DMA1_Stream0	Peripheral To Memory	High *
SPI4_RX	DMA2_Stream3	Peripheral To Memory	High *
I2C3_RX	DMA1_Stream1	Peripheral To Memory	Low
I2C3_TX	DMA1_Stream4	Memory To Peripheral	Low
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low

SPI1_RX: DMA2_Stream0 DMA request Settings:

Mode: **Circular ***
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

SPI2_RX: DMA1_Stream3 DMA request Settings:

Mode: **Circular ***
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

SPI3_RX: DMA1_Stream0 DMA request Settings:

Mode: **Circular ***
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

SPI4_RX: DMA2_Stream3 DMA request Settings:

Mode: **Circular ***
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

I2C3_RX: DMA1_Stream1 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

I2C3_TX: DMA1_Stream4 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream1 global interrupt	true	0	0
DMA1 stream3 global interrupt	true	0	0
DMA1 stream4 global interrupt	true	0	0
DMA1 stream5 global interrupt	true	0	0
DMA1 stream6 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
SPI2 global interrupt	true	0	0
USART2 global interrupt	true	0	0
SPI3 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream3 global interrupt	true	0	0
I2C3 event interrupt	true	0	0
I2C3 error interrupt	true	0	0
SPI4 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
DMA1 stream3 global interrupt	false	true	true
DMA1 stream4 global interrupt	false	true	true
DMA1 stream5 global interrupt	false	true	true
DMA1 stream6 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
SPI1 global interrupt	false	true	true
SPI2 global interrupt	false	true	true
USART2 global interrupt	false	true	true
SPI3 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream3 global interrupt	false	true	true
I2C3 event interrupt	false	true	true
I2C3 error interrupt	false	true	true
SPI4 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware					
System Core	Analog	Timers	Connectivity	Multimedia	Computing
DMA ✓	ADC1 ✓	TIM3 ✓	I2C3 ✓		
GPIO ⚠		TIM4 ✓	SPI1 ✓		
NVIC ✓			SPI2 ✓		
RCC ✓			SPI3 ✓		
SYS ✓			SPI4 ✓		
			USART2 ✓		

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00115249.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00119316.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00137034.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00156364.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note http://www.st.com/resource/en/application_note/DM00144612.pdf
Application note http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note http://www.st.com/resource/en/application_note/DM00325582.pdf
Application note http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note http://www.st.com/resource/en/application_note/DM00354244.pdf
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Application note http://www.st.com/resource/en/application_note/DM00725181.pdf