1. Description

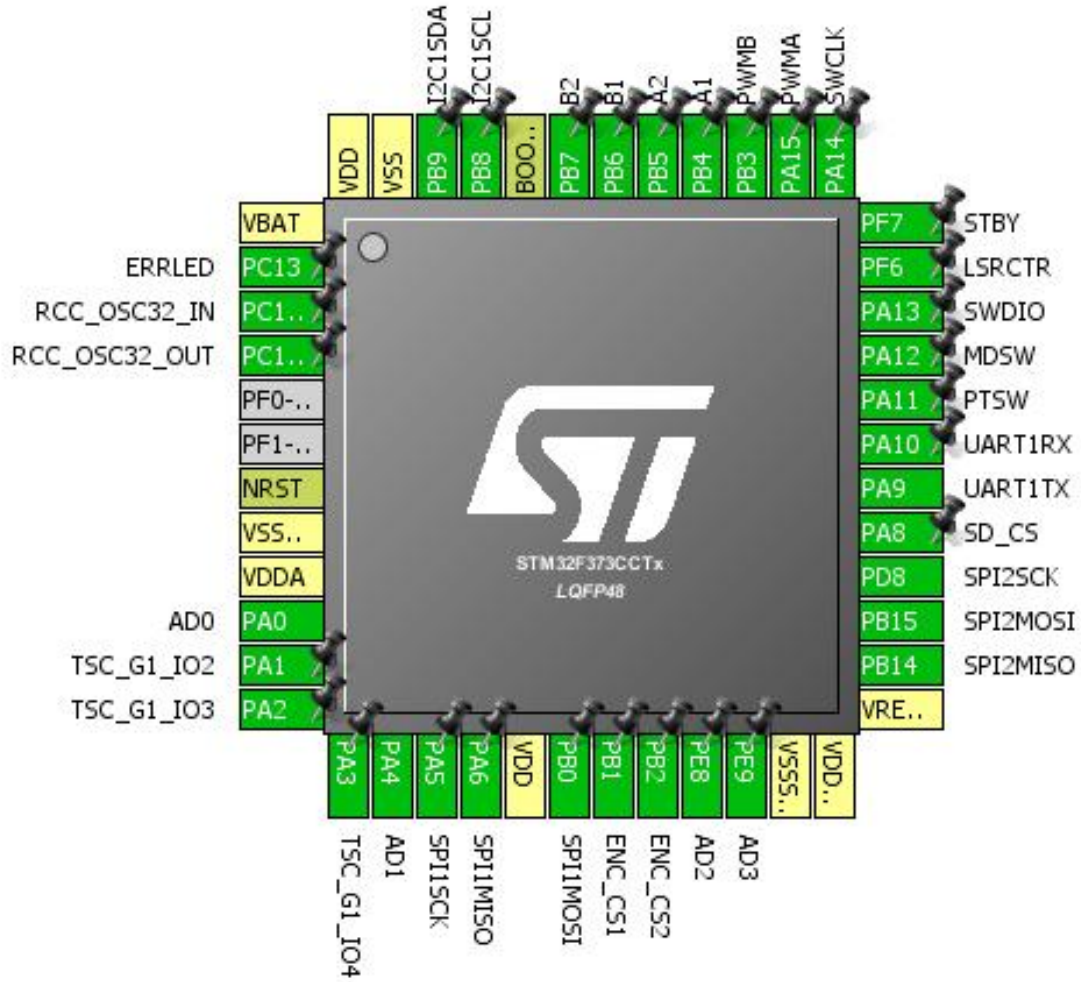
1.1. Project

Project Name	STM32F373CCT_PB5_1
Board Name	STM32F373CCT_PB5_1
Generated with:	STM32CubeMX 4.17.0
Date	03/14/2017

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F373
MCU name	STM32F373CCTx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration



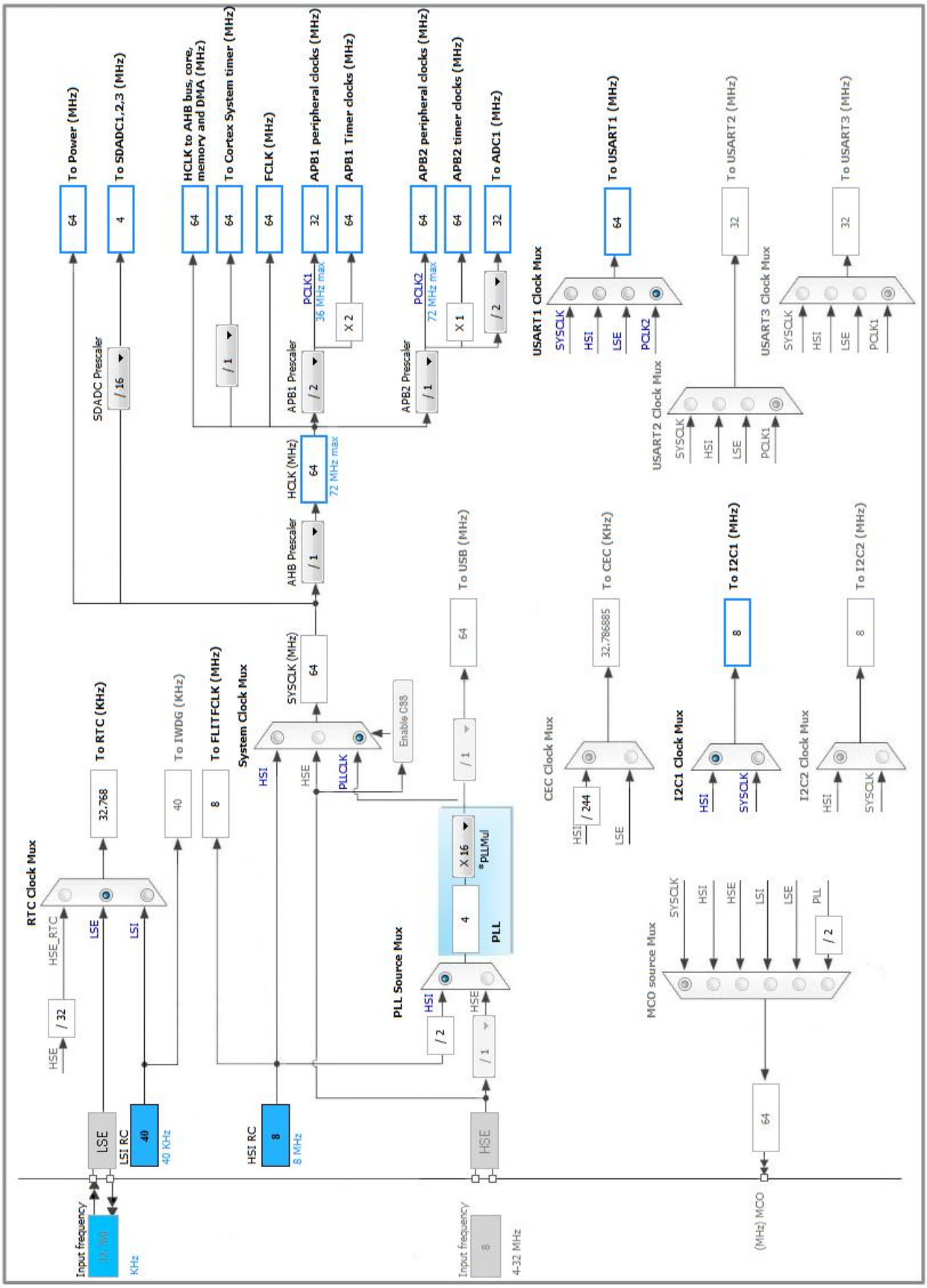
3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Output	ERRLED
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA	Power		
10	PA0	I/O	ADC1_IN0	AD0
11	PA1	I/O	TSC_G1_IO2	
12	PA2	I/O	TSC_G1_IO3	
13	PA3	I/O	TSC_G1_IO4	
14	PA4	I/O	ADC1_IN4	AD1
15	PA5	I/O	SPI1_SCK	SPI1SCK
16	PA6	I/O	SPI1_MISO	SPI1MISO
17	VDD	Power		
18	PB0	I/O	SPI1_MOSI	SPI1MOSI
19	PB1 *	I/O	GPIO_Output	ENC_CS1
20	PB2 *	I/O	GPIO_Output	ENC_CS2
21	PE8	I/O	SDADC2_AIN8P	AD2
22	PE9	I/O	SDADC2_AIN7P	AD3
23	VSSSD/VREFSD-	Power		
24	VDDSD	Power		
25	VREFSD+	Power		
26	PB14	I/O	SPI2_MISO	SPI2MISO
27	PB15	I/O	SPI2_MOSI	SPI2MOSI
28	PD8	I/O	SPI2_SCK	SPI2SCK
29	PA8 *	I/O	GPIO_Output	SD_CS
30	PA9	I/O	USART1_TX	UART1TX
31	PA10	I/O	USART1_RX	UART1RX
32	PA11 *	I/O	GPIO_Input	PTSW
33	PA12 *	I/O	GPIO_Input	MDSW
34	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
35	PF6 *	I/O	GPIO_Output	LSRCTR
36	PF7 *	I/O	GPIO_Output	STBY
37	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
38	PA15	I/O	TIM2_CH1	PWMA

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	PB3	I/O	TIM2_CH2	PWMB
40	PB4 *	I/O	GPIO_Output	A1
41	PB5 *	I/O	GPIO_Output	A2
42	PB6 *	I/O	GPIO_Output	B1
43	PB7 *	I/O	GPIO_Output	B2
44	BOOT0	Boot		
45	PB8	I/O	I2C1_SCL	I2C1SCL
46	PB9	I/O	I2C1_SDA	I2C1SDA
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

mode: IN4

5.1.1. Parameter Settings:

ADC_Settings:	
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Number Of Conversion	**2 ***
External Trigger Conversion Edge	**Trigger detection on the rising edge ***
External Trigger Conversion Source	Timer 19 Trigger Out event
Rank	1
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**2 ***
Channel	**Channel 4 ***
Sampling Time	1.5 Cycles
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

5.2. I2C1

I2C: I2C

5.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x2000090E

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.3. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.4. RTC

mode: Activate Clock Source

5.4.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

5.5. SDADC2

IN7: IN7-Single-Ended

IN8: IN8-Single-Ended

mode: Conversion Configuration 0

mode: Conversion Configuration 1

5.5.1. Parameter Settings:

General Settings:

Low Power Mode	None
Fast Conversion Mode	Disable
Slow Clock Mode	Disable
Reference Voltage	Forced externally using VREF pin

Conversion Configuration 0:

Input Mode	Differential mode
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

Conversion Configuration 1:

Input Mode	Differential mode
Gain	equal to 1
Common Mode	SDADC VSSA
Offset	0

SDADC Regular Conversions Settings:

Enable Regular Conversion	Disable

SDADC Injected Conversions Settings:

Enable Injected Conversion	Disable

5.6. SPI1

Mode: Full-Duplex Master

5.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola

Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**2.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.7. SPI2

Mode: Full-Duplex Master

5.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**16.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.8. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.9. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.10. TIM3

Clock Source : Internal Clock

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.11. TIM4

Clock Source : Internal Clock

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.12. TIM19

Clock Source : Internal Clock

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.13. TSC

Sampling: G1_IO2

mode: G1_IO3

mode: G1_IO4

5.13.1. Parameter Settings:

TSC Settings:

Charge Transfer High Pulse Length	2 Cycles
Charge Transfer Low Pulse Length	2 Cycles
Spread Spectrum	Disable
Pulse Generator Prescaler	Synchronous clock mode divided by 64
Maximum Count Value	**16383 charge transfer cycles ***
IO Default Mode	Output push-pull low
Acquisition Mode	Normal acquisition mode

5.14. USART1

Mode: Asynchronous

5.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN0	Analog mode	No pull up pull down	n/a	AD0
	PA4	ADC1_IN4	Analog mode	No pull up pull down	n/a	AD1
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull up	**High ***	I2C1SCL
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull up	**High ***	I2C1SDA
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
SDADC2	PE8	SDADC2_AIN8P	Analog mode	No pull up pull down	n/a	AD2
	PE9	SDADC2_AIN7P	Analog mode	No pull up pull down	n/a	AD3
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull up pull down	**High ***	SPI1SCK
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull up pull down	**High ***	SPI1MISO
	PB0	SPI1_MOSI	Alternate Function Push Pull	No pull up pull down	**High ***	SPI1MOSI
SPI2	PB14	SPI2_MISO	Alternate Function Push Pull	No pull up pull down	**High ***	SPI2MISO
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull up pull down	**High ***	SPI2MOSI
	PD8	SPI2_SCK	Alternate Function Push Pull	No pull up pull down	**High ***	SPI2SCK
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	No pull up pull down	Low	PWMA
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull up pull down	Low	PWMB
TSC	PA1	TSC_G1_IO2	Alternate Function Open Drain	No pull up pull down	Low	
	PA2	TSC_G1_IO3	Alternate Function Push Pull	No pull up pull down	Low	
	PA3	TSC_G1_IO4	Alternate Function Push Pull	No pull up pull down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull up	**High ***	UART1TX
	PA10	USART1_RX	Alternate Function Push Pull	Pull up	**High ***	UART1RX
GPIO	PC13	GPIO_Output	Output Push Pull	**Pull down ***	Low	ERRLED
	PB1	GPIO_Output	Output Push Pull	**Pull up ***	**High ***	ENC_CS1
	PB2	GPIO_Output	Output Push Pull			ENC_CS2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
				Pull up *	**High ***	
	PA8	GPIO_Output	Output Push Pull	**Pull up ***	**High ***	SD_CS
	PA11	GPIO_Input	Input mode	**Pull up ***	**n/a**	PTSW
	PA12	GPIO_Input	Input mode	**Pull up ***	**n/a**	MDSW
	PF6	GPIO_Output	Output Push Pull	**Pull down ***	**High ***	LSRCTR
	PF7	GPIO_Output	Output Push Pull	**Pull down ***	**High ***	STBY
	PB4	GPIO_Output	Output Push Pull	**Pull down ***	**High ***	A1
	PB5	GPIO_Output	Output Push Pull	**Pull down ***	**High ***	A2
	PB6	GPIO_Output	Output Push Pull	**Pull down ***	**High ***	B1
	PB7	GPIO_Output	Output Push Pull	**Pull down ***	**High ***	B2

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	**High ***

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
ADC1 interrupt	true	0	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	true	0	0
SDADC2 global interrupt	true	0	0
TIM19 global interrupt	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line2 interrupt and touch sense controller interrupt	unused		
TIM2 global interrupt	unused		
I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F373
MCU	STM32F373CCTx
Datasheet	022691_Rev6

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	STM32F373CCT_PB5_1
Project Folder	C:\Users\stern\workspace\STM32F373CCT_PB5_1
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F3 V1.6.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No