CHAPTER 3

INTEL 8086 ARCHITECTURE AND ADDRESSING MODES

MAJOR FEATURES OF 8086 PROCESSOR

- 8086 Microprocessor is an enhanced version of 8085 Microprocessor that was designed by Intel in 1976.
- It is a *16-bit Microprocessor* having *20 address lines and16 data lines* that provides up to 1MB storage.
- It consists of powerful instruction set, which *provides operations like multiplication and division easily*.
- It supports two modes of operation, i.e. *Maximum mode and Minimum mode*.
- *Maximum mode is suitable for system having multiple processors* and Minimum mode is suitable for system having a single processor.

FEATURES OF 8086

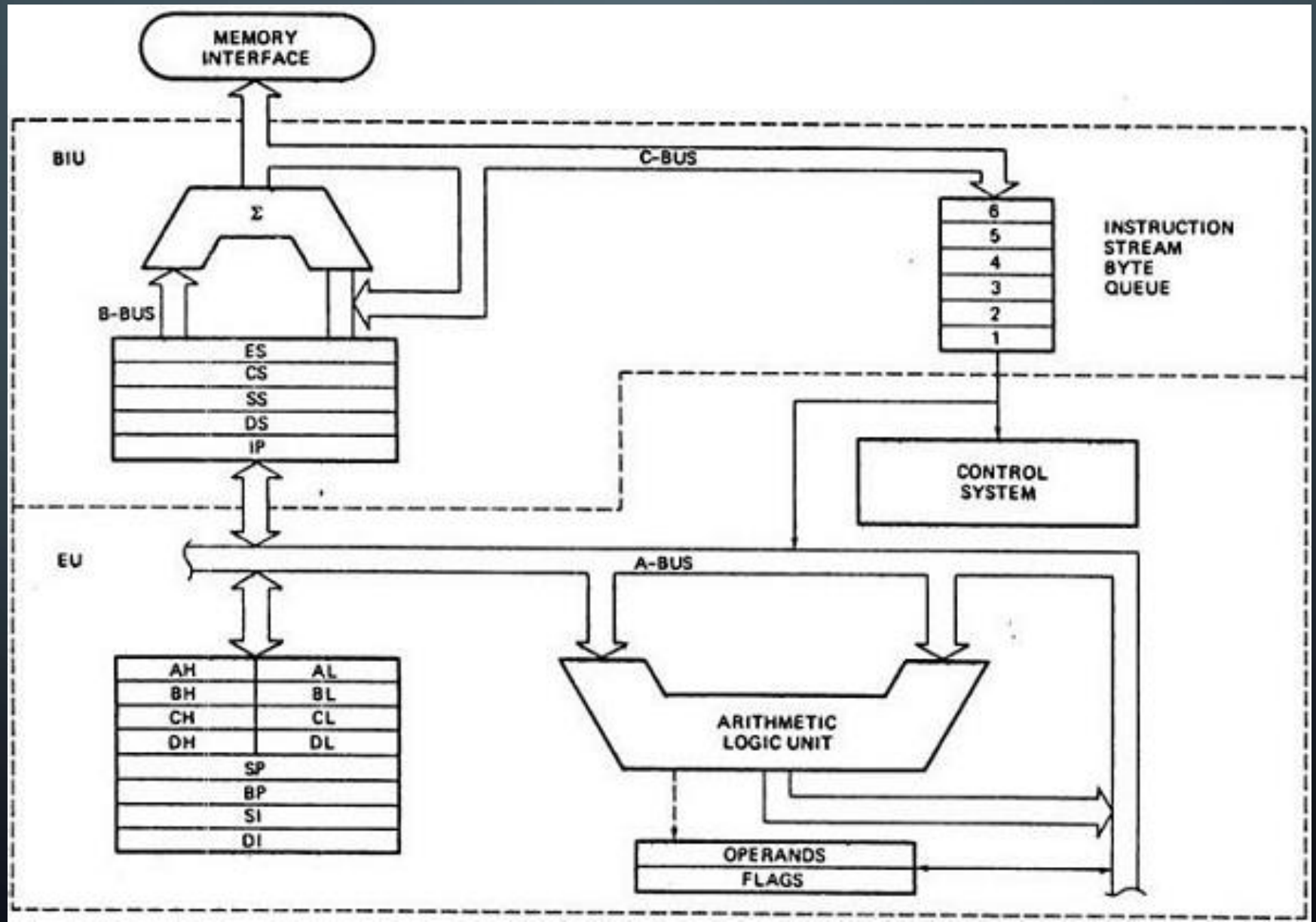
The most prominent features of a 8086 microprocessor are as follows –

- It has an *instruction queue, which is capable of storing six instruction bytes* from the memory resulting in faster processing.
- It was the *first 16-bit processor having 16-bit ALU, 16-bit registers, internal data bus, and 16-bit external data bus* resulting in faster processing.
- It is available in 3 versions based on the frequency of operation –
  - 8086 → 5MHz
  - 8086-2 → 8MHz
  - 8086-1 → 10 MHz

- It uses two stages of pipelining, i.e. *Fetch Stage and Execute Stage*, which improves performance.
- Fetch stage can *pre-fetch up to 6 bytes of instructions* and *stores them in the queue.*
- Execute stage executes these instructions.
- It has *256 vectored interrupts*.
- It consists of *29,000 transistors.*

8085 Microprocessor	8086 Microprocessor
It is an 8-bit microprocessor.	It is a 16-bit microprocessor.
It has a 16-bit address line.	It has a 20-bit address line.
It has a 8-bit data bus.	It has a 16-bit data bus.
The memory capacity is 64 KB.	The memory capacity is 1 MB.
The Clock speed of this microprocessor is 3 MHz.	The Clock speed of this microprocessor varies between 5, 8 and 10 MHz for different versions.
It has five flags.	It has nine flags.
8085 microprocessor does not support memory segmentation.	8086 microprocessor supports memory segmentation.
It does not support pipelining.	It supports pipelining.
It is accumulator based processor.	It is general purpose register based processor.
It has no minimum or maximum mode.	It has minimum and maximum modes.
In 8085, only one processor is used.	In 8086, more than one processor is used. An additional external processor can also be employed.
It contains less number of transistors compare to 8086 microprocessor. It contains about 6500 transistor.	It contains more number of transistors compare to 8085 microprocessor. It contains about 29000 transistors.
The cost of 8085 is low.	The cost of 8086 is high.

ARCHITECTURE OF 8086



- 8086 Microprocessor is divided into two functional units:

➢ *EU (Execution Unit):*

- Execution unit *gives instructions to BIU* stating *from where to fetch the data and then decode and execute* those instructions.
- Its function is to *control operations on data* using the instruction decoder & ALU.
- EU *has no direct connection with system buses* as shown in the previous figure, it *performs operations over data through BIU*.
- EU consists of the following components:
  1. *ALU*
  2. *Flag registers.*

1. ALU:

- It *handles all arithmetic and logical operations*, like +, −, ×, /, OR, AND, NOT operations.

2. Flag Register:

- It is a *16-bit register that behaves like a flip-flop*, i.e. it *changes its status according to the result* stored in the accumulator.
- It has *9 flags* and they are *divided into 2 groups*

  2.1 Conditional Flags

  2.2 Control Flags.

2.1. CONDITIONAL FLAGS

- It *represents the result of the last arithmetic or logical instruction executed*. Following is the list of conditional flags –

1. **Carry flag**
   - This flag *indicates an overflow condition* for arithmetic operations.
2. **Auxiliary flag**
   - When an operation is performed at ALU, if it results in a *carry/barrow from lower nibble (i.e. D0 – D3) to upper nibble (i.e. D4 – D7), then this flag is set*, i.e. *carry given by D3 bit to D4 is AF flag*.
3. **Parity flag** –
   - This flag is used to *indicate the parity of the result*, i.e. when the lower order 8-bits of the result contains *even number of 1's, then the Parity Flag is set*.
   - For *odd number of 1's, the Parity Flag is reset*.

4. **Zero flag**
   - This flag is *set to 1 when the result of arithmetic or logical operation is zero* else it is set to 0.
5. **Sign flag**
   - This flag *holds the sign of the result*.
   - When the *result of the operation is negative, then the sign flag is set to 1 else set to 0.*
6. **Overflow flag**
   - This flag *represents the result when the system capacity is exceeded*.