**Timing Analysis of JTAG Communication (MSP430F5438A and MSP-FET430UIF)**

According to the datasheet for the MSP430F5438A, the maximum TCK frequency is 10MHz as shown by the following table.

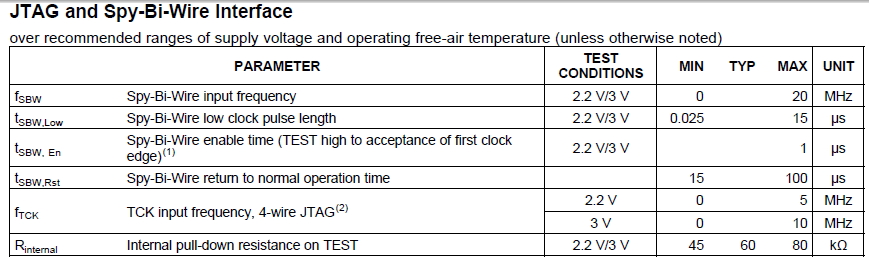


Figure 1: MSP430F5438A Datasheet JTAG Timing Requirements

When using the logic analyzer to sample the JTAG signals, we must sample at least at twice the highest frequency of the signals. Therefore I set the sample rate at 50MHz. Figure 2 displays a screen capture of the JTAG signals: TCK, TMS, TDI, TDO. Note that the highest TCK frequency is 3.847MHz which is less than the maximum TCK frequency specified by the datasheet.

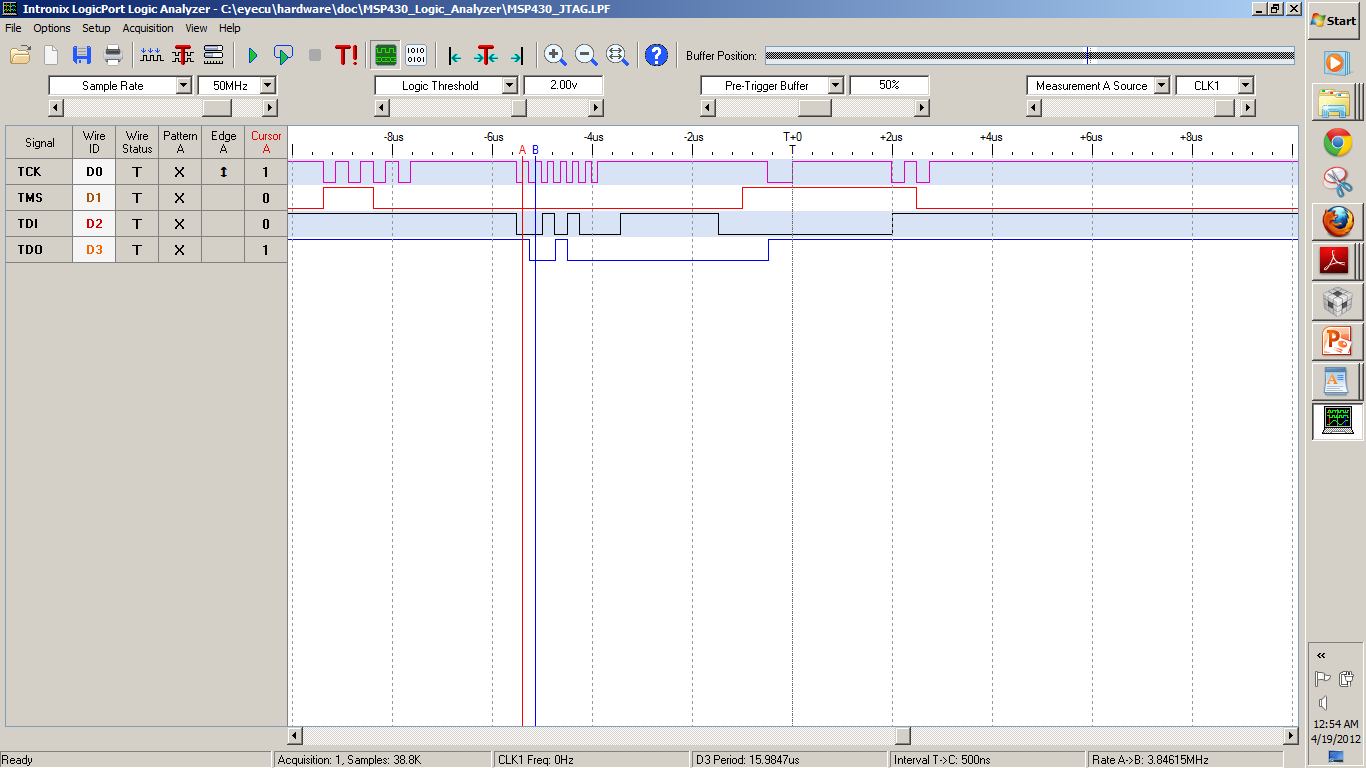


Figure 2: Logic Analyzer Capture of JTAG Communication

**MSP430F5438A Programming and Verification**

Adapting some sample code provided by Texas Instruments, I was able to verify that the MSP430F5438A was successfully programmed.

According to the datasheet for the MSP430F5438A, there is an internal low frequency oscillator onboard. The frequency of this oscillator is 32kHz as shown in the following excerpt from the datasheet.

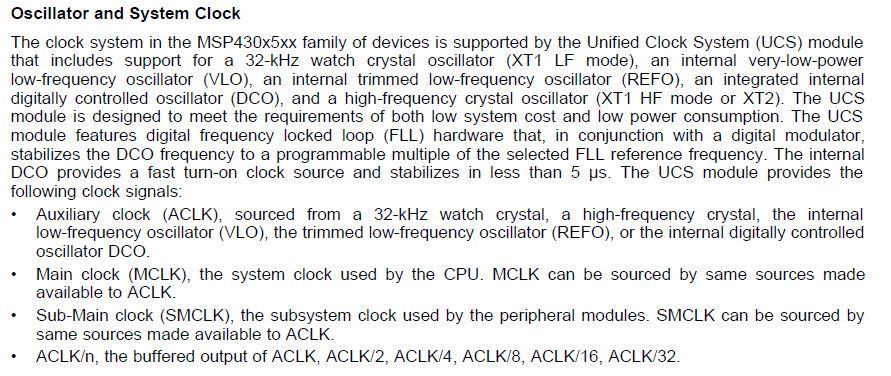


Figure 3: MSP430F5438A Internal Oscillator

To verify the proper programming of the MSP, I set the internal clock to output to pin P11.0 and probed the waveform generated at this pin. The following is the code I used to program the MSP

**#include** "msp430x54xA.h"

**void** **main**(**void**)

{

WDTCTL = WDTPW + WDTHOLD; // Stop WDT

P11DIR = BIT0; // P11.0 to output direction

P11SEL = BIT0; // P11.0 to output ACLK

UCSCTL4 |= SELS\_5; // Select ACLK source

**while**(1); // Loop in place

}

Figure 4 displays the waveform captured by the oscilloscope. As we expect, the signal has a frequency of roughly 32.768kHz and a voltage of ~3.3V.

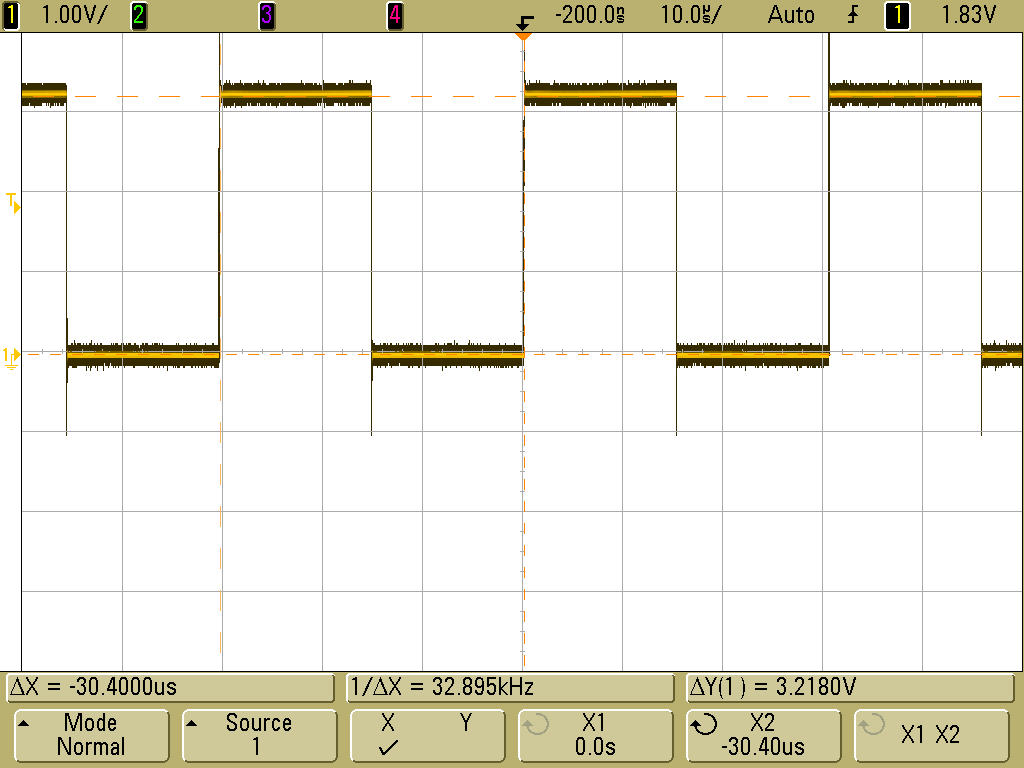


Figure 4: Oscilloscope Capture of ACLK

Furthermore, the debugger in Code Composer Studio version 5 is operational as shown by Figure 5.

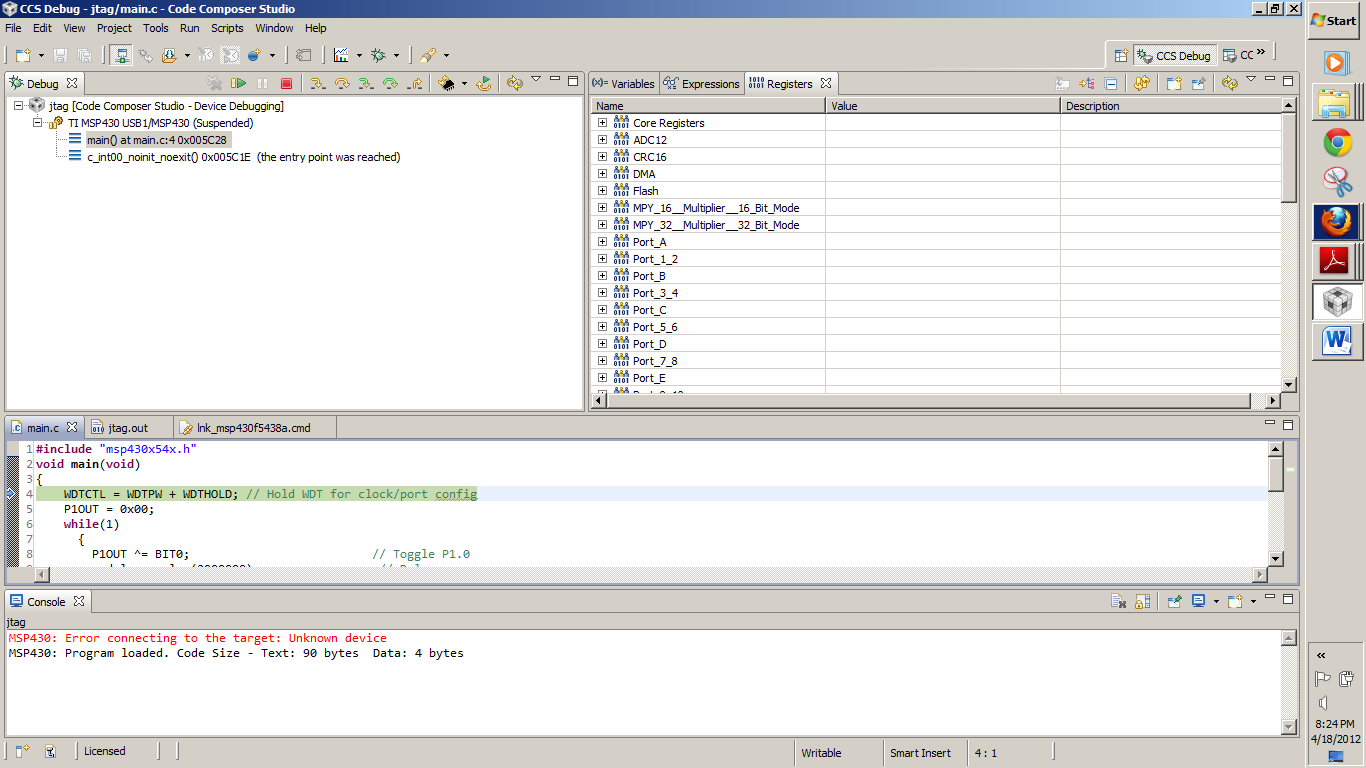


Figure 5: CCSv5 Debugger Operational