Shri Vile Parle Kelavani Mandal's
DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING
(Autonomous College Affiliated to the University of Mumbai)
NAAC Accredited with "A" Grade (CGPA : 3.18)

End Semester Examination (February 2022)
Academic Year: 2021-2022

Max. Marks: 50	**Duration: 2 Hr.**
Class: **TE**	Semester: V
Course: **Processor Organization and Architecture**	Course Code: **DJ19CEC502**
Program: **Third Year Computer Engineering**	

Instructions:
(1) Solve ANY FIVE questions.
(2) Read the questions carefully.
(3) Assume suitable data wherever required, but justify it.
(4) All questions carry equal marks.
(5) Answer to each new question is to be started on a fresh page.
(6) Figure to the right indicate full marks.
(7) Draw the neat labelled diagrams wherever necessary.

Question No.		Max. Marks
Q1 (a)	Explain Von Neumann architecture with the help of diagram.	5
Q1 (b)	Evaluate (8 divided by 4) using Restoring algorithm	5
Q2 (a)	What is Cache Coherency? Describe any one method to ensure Cache coherency.	10
	OR	
Q2(b)	Explain and evaluate for the given reference page string 7,0,1,2,0,3,0,4,2,3,0,3,1,2,0 find out the page fault and page hit for FIFO replacement algorithm. Page frame size=3	10
Q3 (a)	Explain in detail about the different addressing modes in Microprocessor 8086.	10
	OR	
Q3 (b)	Discuss various instruction format for 8086 with suitable example.	10
Q4 (a)	Explain software interrupts in 8086 with suitable example	5
Q4 (b)	Describe instruction set with example :PUSH and POP	5
Q5 (a)	Explain the concept of Virtual Memory.	5
Q5 (b)	Describe Interrupts in 8051 microcontroller with suitable example	5
Q6 (a)	Explain 5 stage pipelining with suitable example	10
	OR	
Q6 (b)	Write short note on Pentium Superscalar Architecture	10

All the Best!