Chapter3:
Multiplexer, Latch, Buffer

Asst.Prof.Dr.Supakit Nootyaskool

Objective

- Explain the concept of multiplexer and de-multiplexer circuit in the data communication system อย่างใน Telecom
- Understand the different between the latch circuit and buffer circuit.
- Explain the truth table of Set-Reset flipflop also know the circuit.

Topic

- Multiplexer circuit
- Demultiplexer circuit
- Latch circuit
- Buffer circuit
- Set-Reset Flipflop

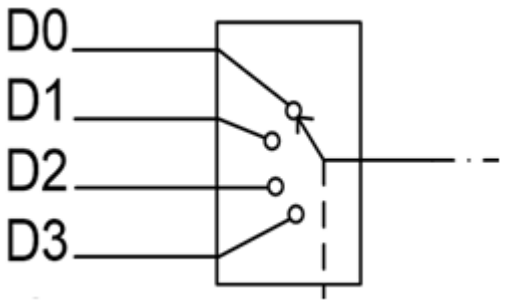
MULTIPLEXER CIRCUIT

Student will able to explain the multiplexer circuit.

Student realizes the important of the multiplexer circuit in the communication system.

Selector switch

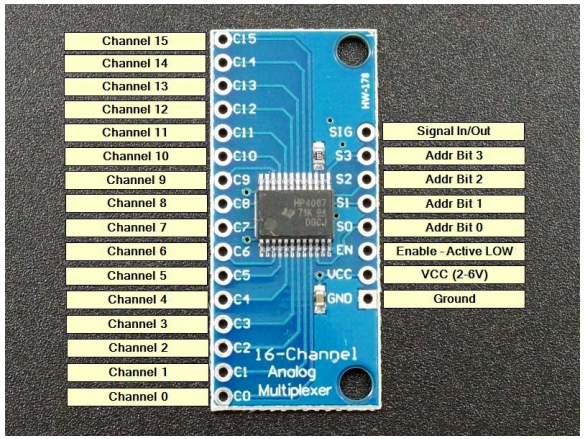
เป็นลูกบิด ในเครื่องซักผ้า, Microwave

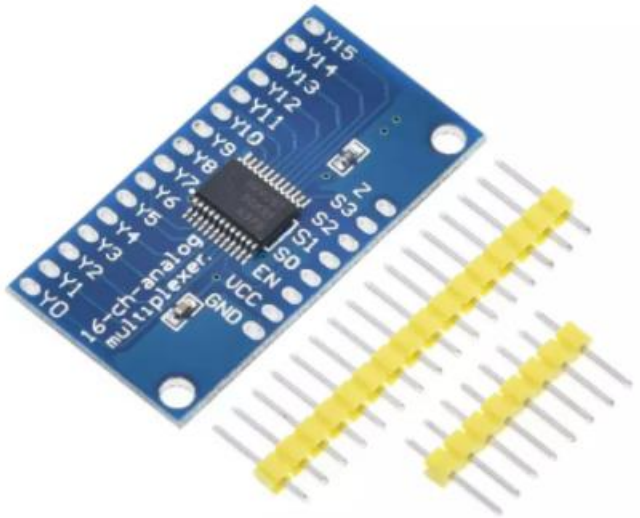


A selector switch is a mechanical switch used to select between different signal channels. Selector switches are commonly found in electrical machines, radios, and even in vehicles.

เช่น เลือกสัญญาณ Internet ที่แบ่งใช้หลายช่องสัญญาณ

Switch -> Multiplexer (MUX)





LazGlobal CD74HC4067 16-Channel Analog Digital Multiplexer Breakout Board Module For Arduino

★★★★★ 1 คะแน

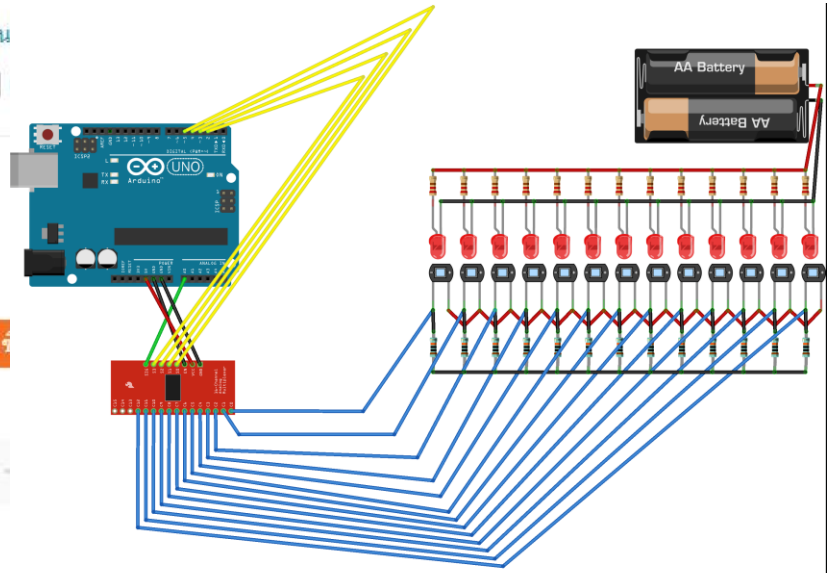
แบรนด์: No Brand |

฿36.00

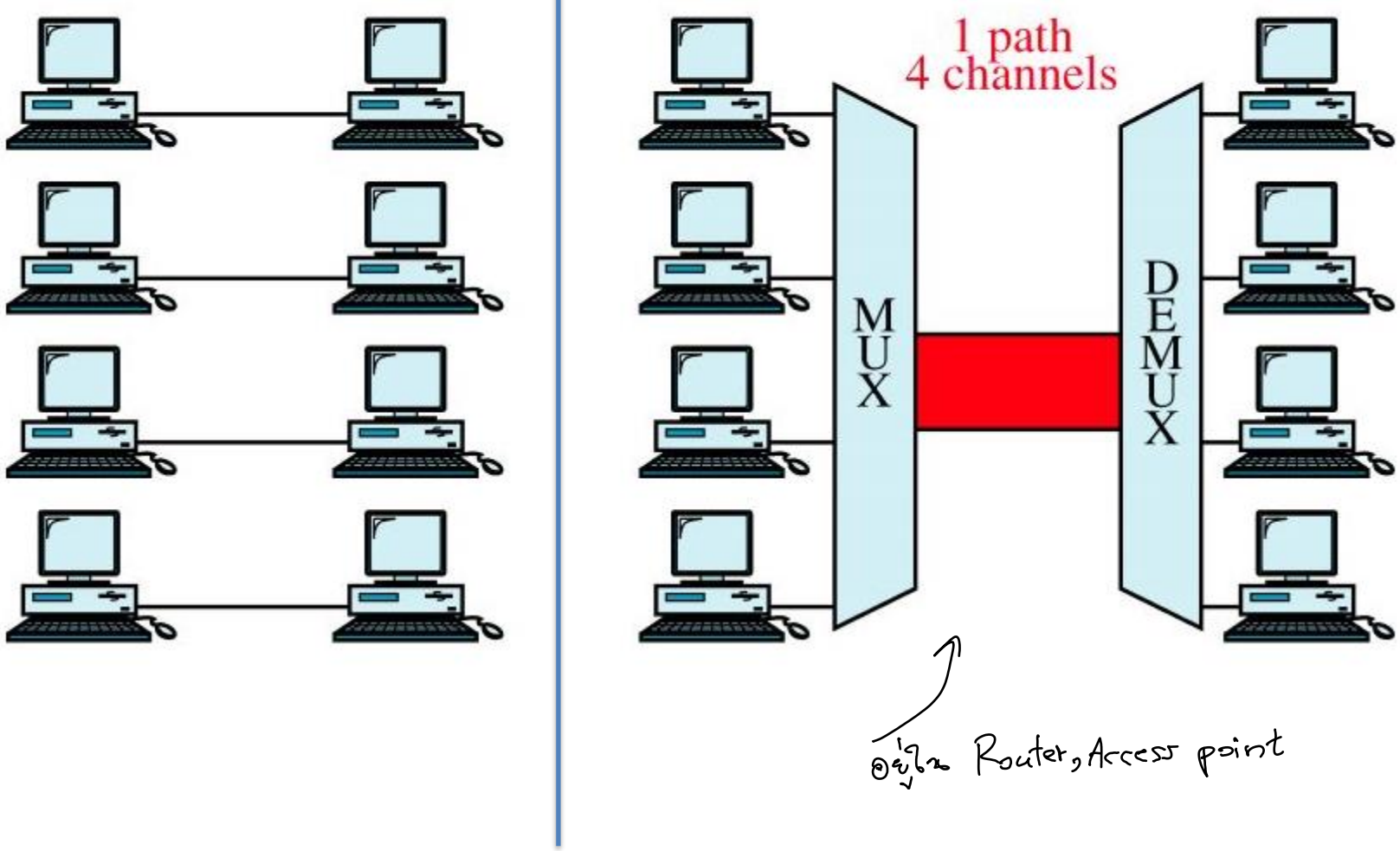
฿50.00 -28%

โปรโมชั่น

จำนวน

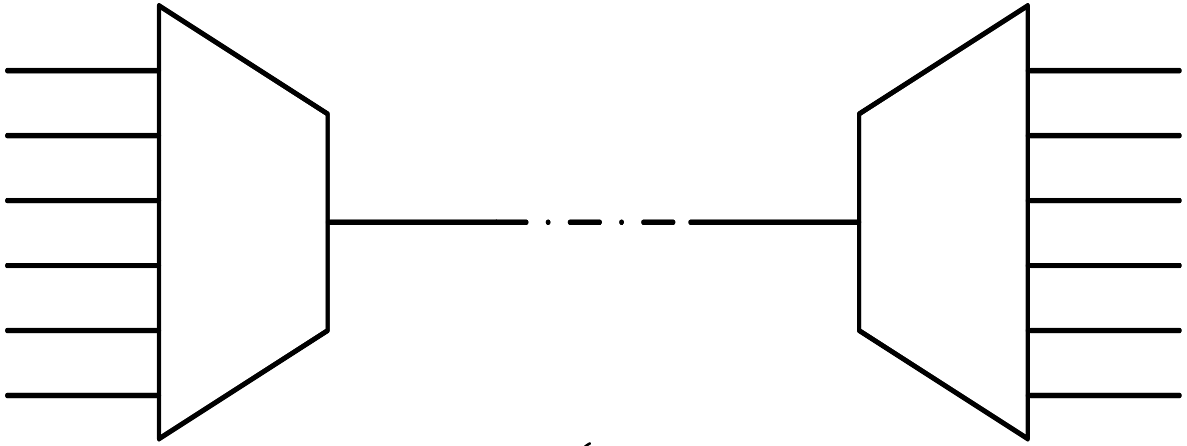


Compare between No MUX and MUX



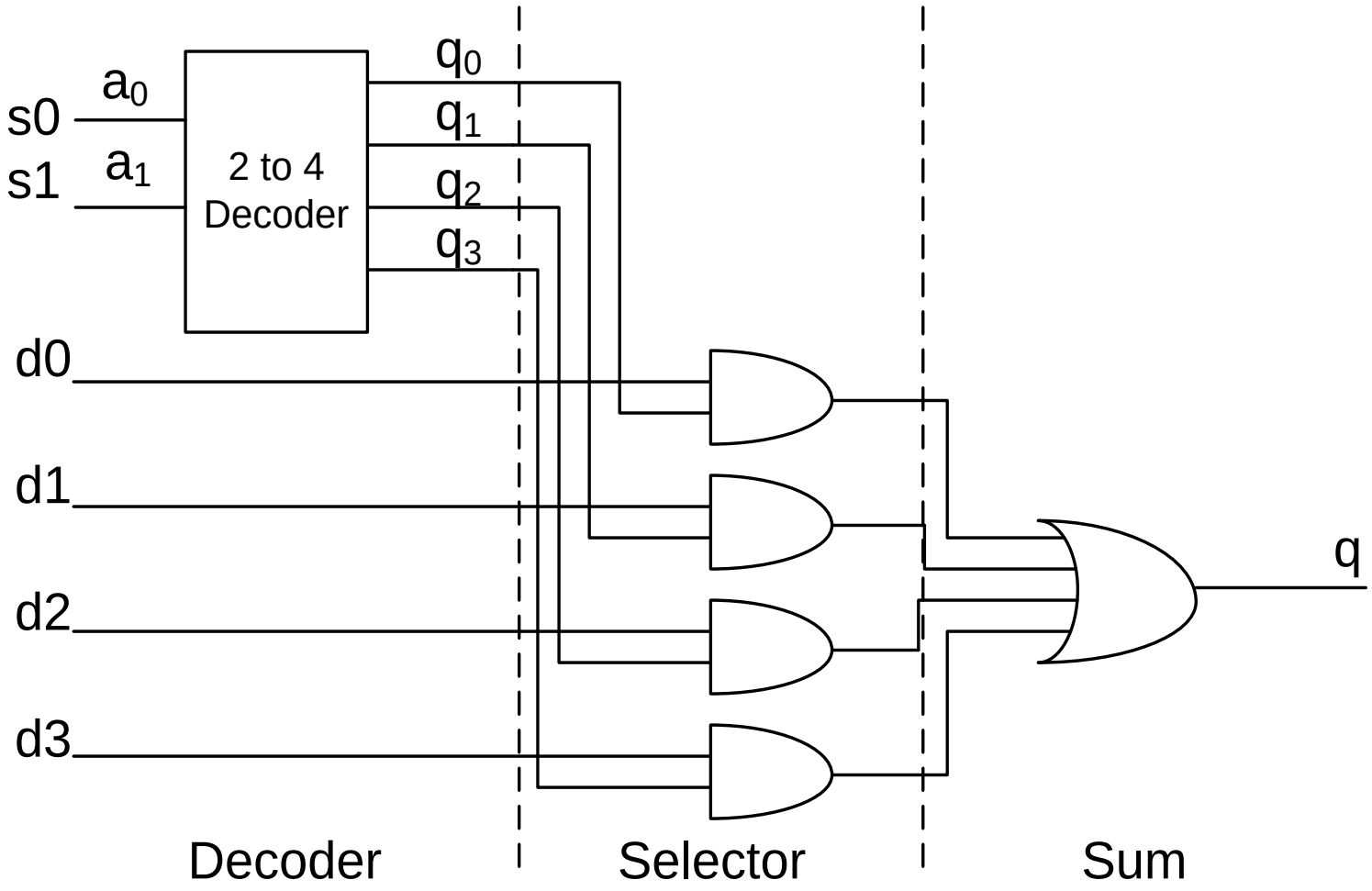
What is circuit inside MUX and DEMUX

สาย sekct อาจจะมี/ไม่มี
(ใช้การ synchronize เวลาแทน
ว่ากี่วินาที → channel ไหนส่ง)

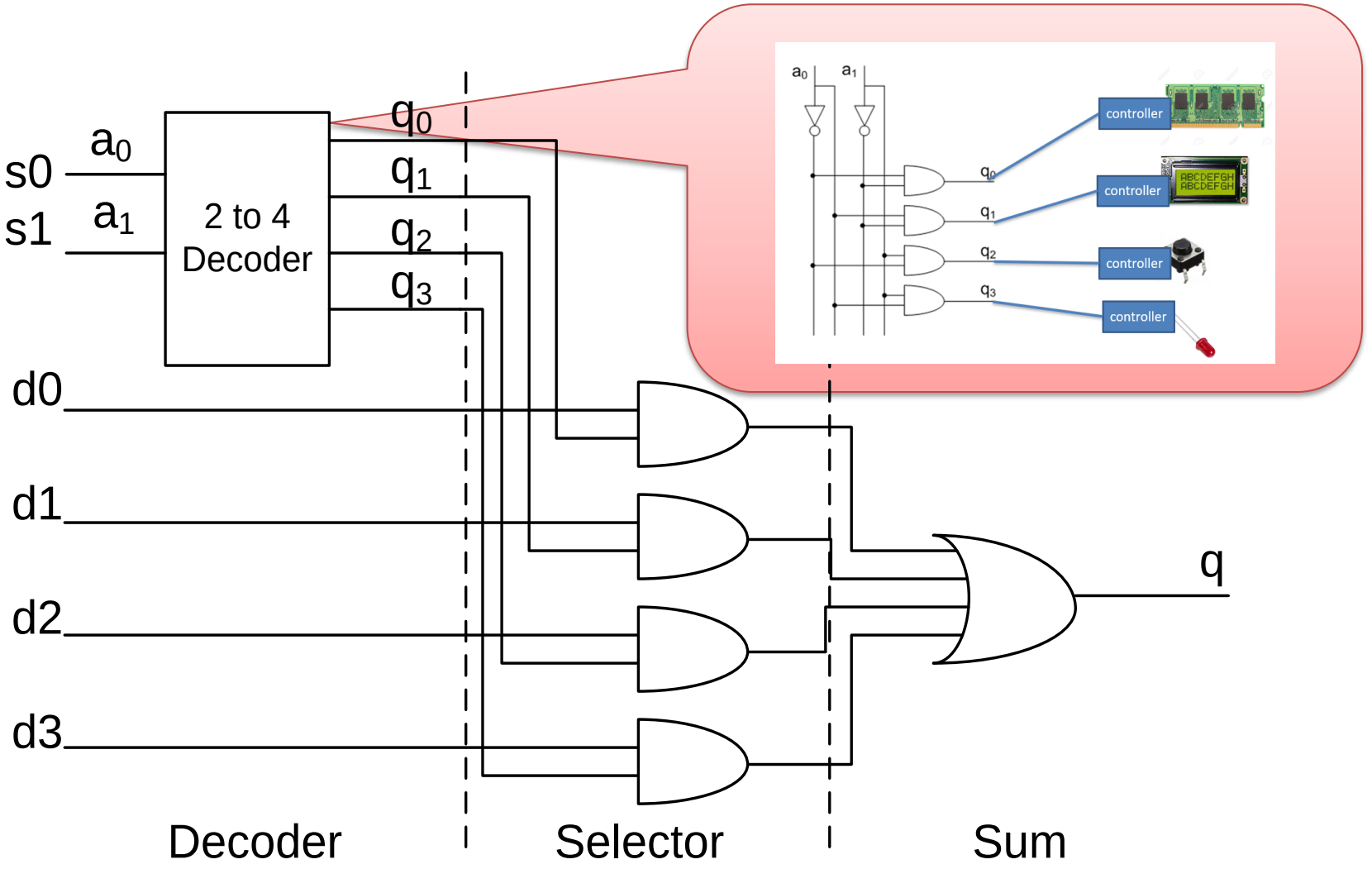


สัญลักษณ์ทาง electronics
MUX /DEMUX

Multiplexer circuit



Multiplexer circuit

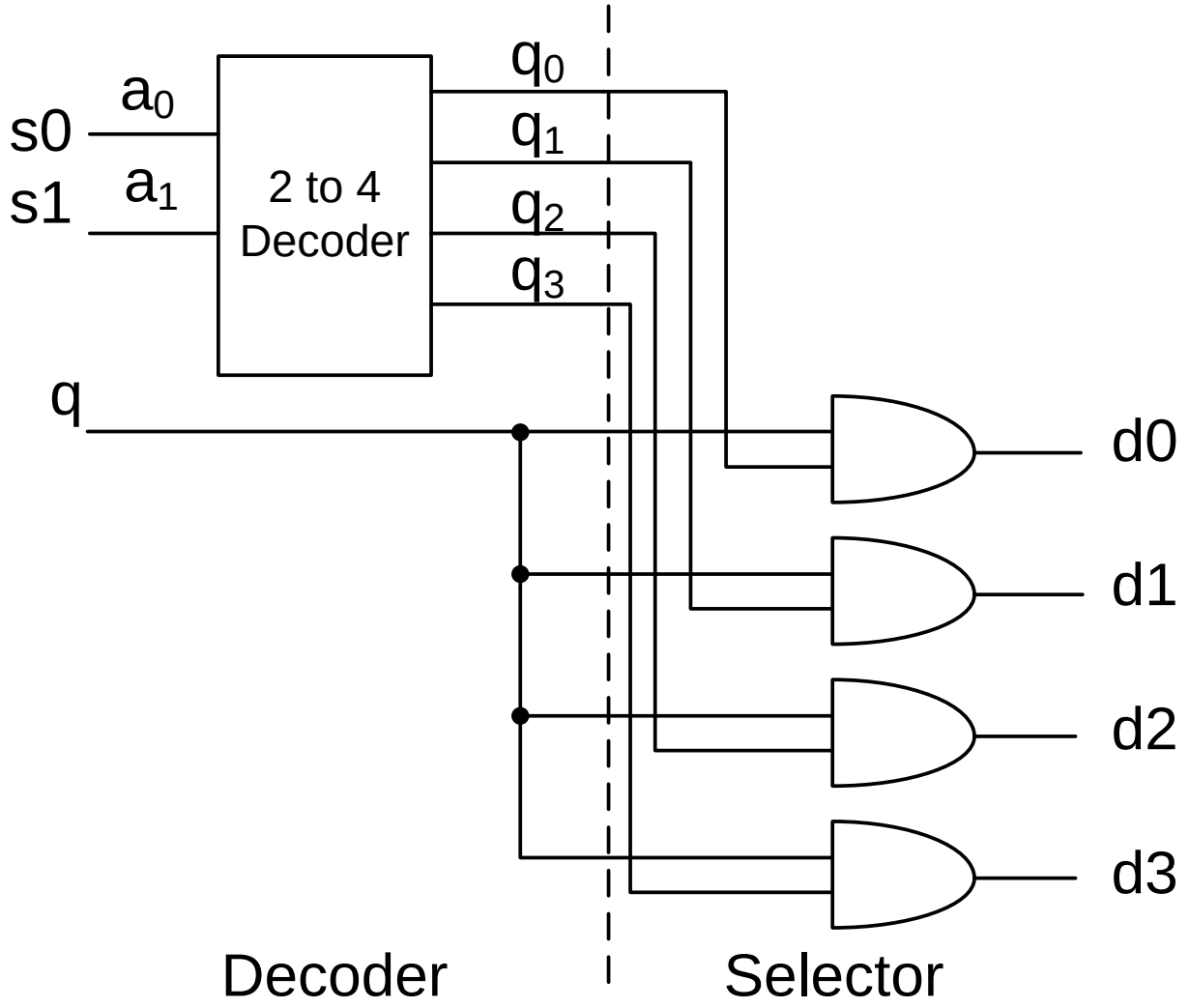


DEMULTIPLEXER CIRCUIT

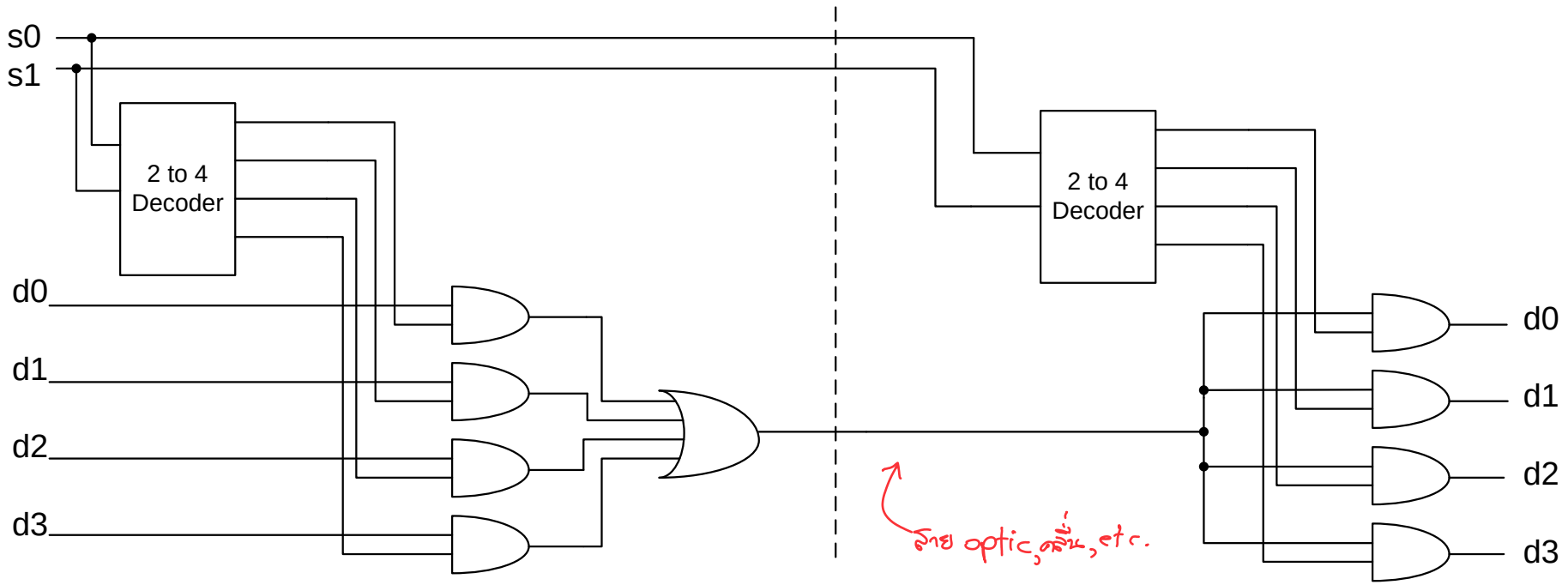
Student will able to understand the data switching in the multiplexer through the demultiplexer circuit .

De-multiplexer circuit

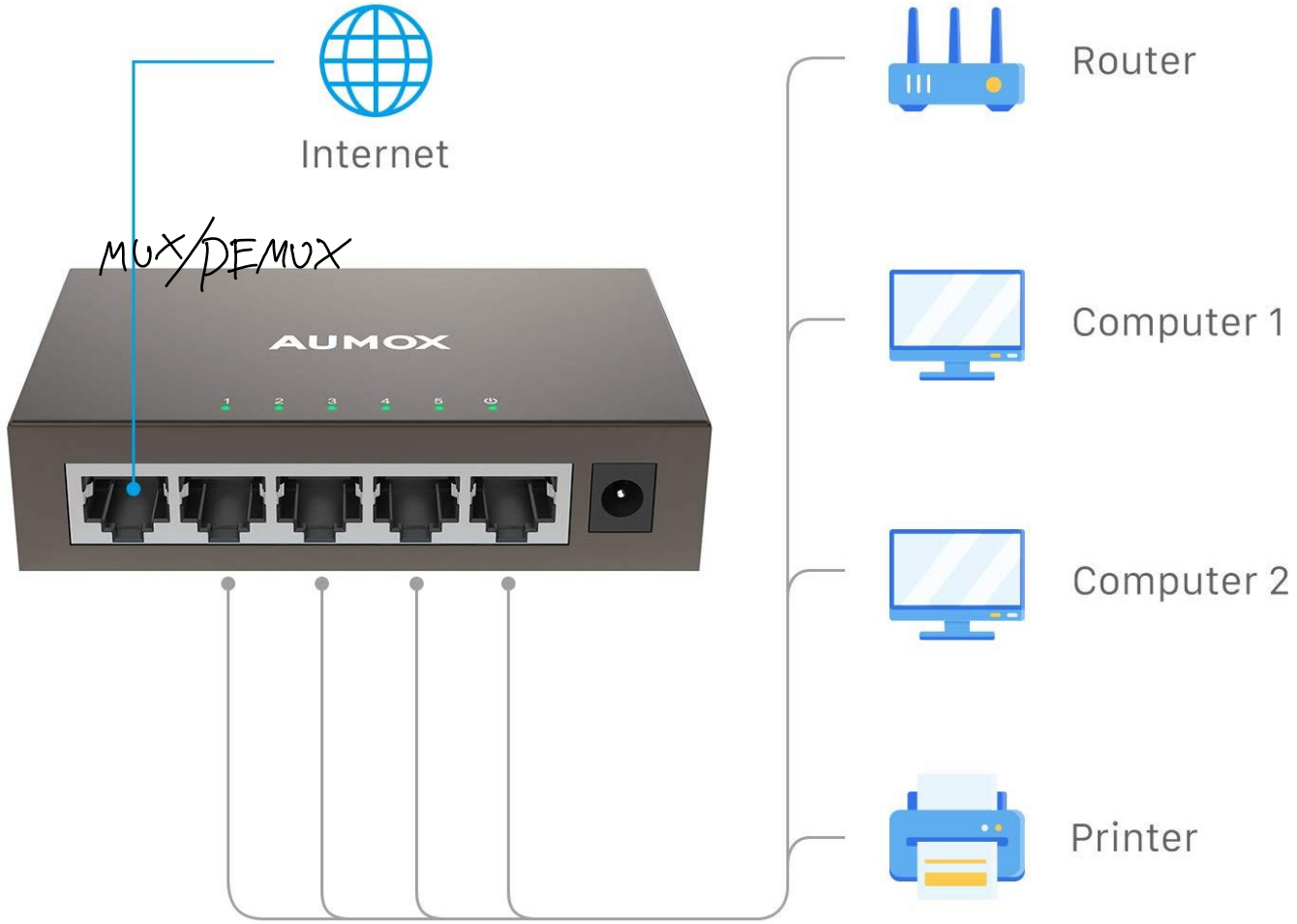
เข้า 1 ออกได้ n ช่อง



MUX + DEMUX


s0
s1
2 to 4
Decoder
d0
d1
d2
d3
2 to 4
Decoder
d0
d1
d2
d3
สาย optic, คลื่น, etc.

Example devices use MUX/DMUX



trai-state gate

TRISTATE GATE

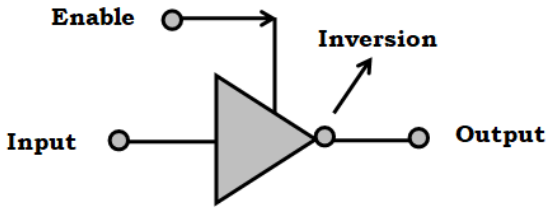
Student will understand the role of tristate gate in the switching circuit.

Student will able to explain the state of high implement in the digital system.

Tristate gate

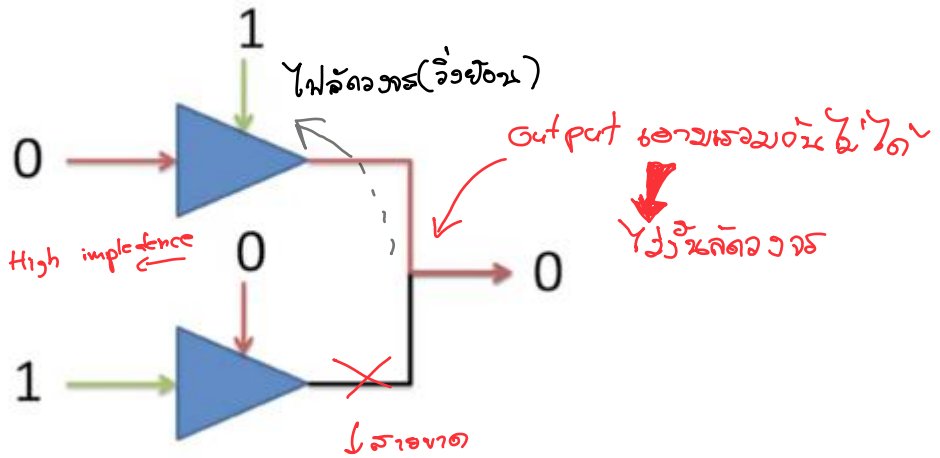
- Three possible logic levels:
  - Logic high (H)
  - Logic low (0V)
  - High impledence (Z) ค่าความต้านทานสูง >1MΩ
- High impendence (Z) occurs when the output behaves like an open circuit (disconnecting).
- High impledence typically exceeding 1MΩ. like open circuit.

↳ สายไฟขาด



Enable	Input	Output
0	0	Hi-Z
0	1	Hi-Z
1	0	1
1	1	0

แต่ก็ขึ้นกับชนิดว่าจะ active ที่ 0 หรือ 1



Tristate gate datasheet and package

SN74LVC1G125 Single Bus Buffer Gate With 3-State Output

1 Features

- Available in the Ultra Small 0.64-mm^2 Package (DPW) With 0.5-mm Pitch
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V_{CC}
- Max t_{pd} of 3.7 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Cable Modem Termination System
- High-Speed Data Acquisition and Generation
- Military: Radar and Sonar
- Motor Control: High-Voltage
- Power Line Communication Modem
- SSD: Internal or External
- Video Broadcasting and Infrastructure: Scalable Platform
- Video Broadcasting: IP-Based Multi-Format Transcoder
- Video Communications System

3 Description

This bus buffer gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G125 device is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

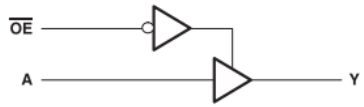
The SN74LVC1G125 device is available in a variety of packages including the ultra-small DPW package with a body size of 0.8 mm × 0.8 mm.

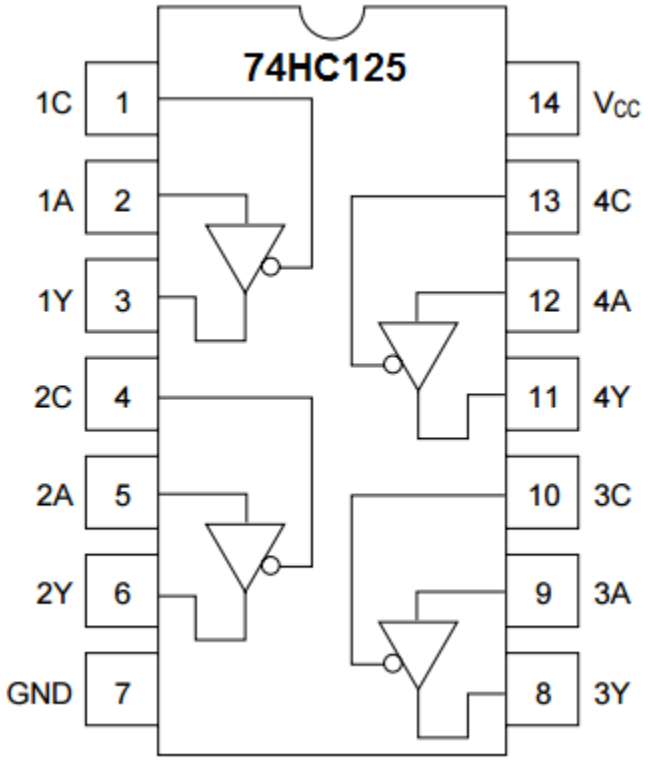
Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
SN74LVC1G125	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
	SON (6)	1.45 mm × 1.00 mm
	DSBGA (5)	1.40 mm × 0.90 mm
	X2SON (4)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic





LATCH AND BUFFER

Student will able to explain the different between the latch and buffer.

Latch vs Buffer

คนสื่อนใหญ่เรียก Buffer หมดทั้งนั้น

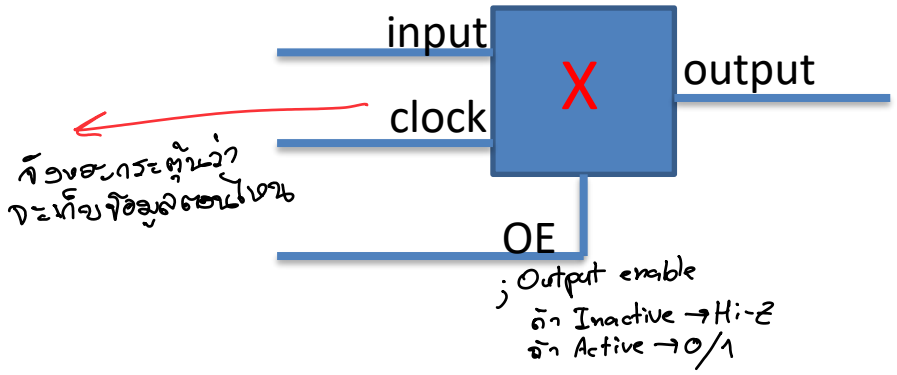
พักข้อมูล

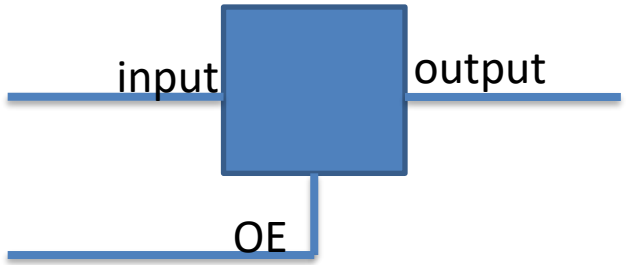
- **Latch**: A latch is used in digital circuits to hold data. The data in the latch remains unchanged until a clearing or enabling signal is sent, which triggers the data to change. Essentially, the latch's primary function is to store memory.

- **Buffer**: A buffer operates with both analog and digital signals. Unlike latches, buffers are not just used for holding memory. They serve additional purposes, such as increasing output power or altering output impedance.

ขับสัญญาณ

Latch/buffer concept





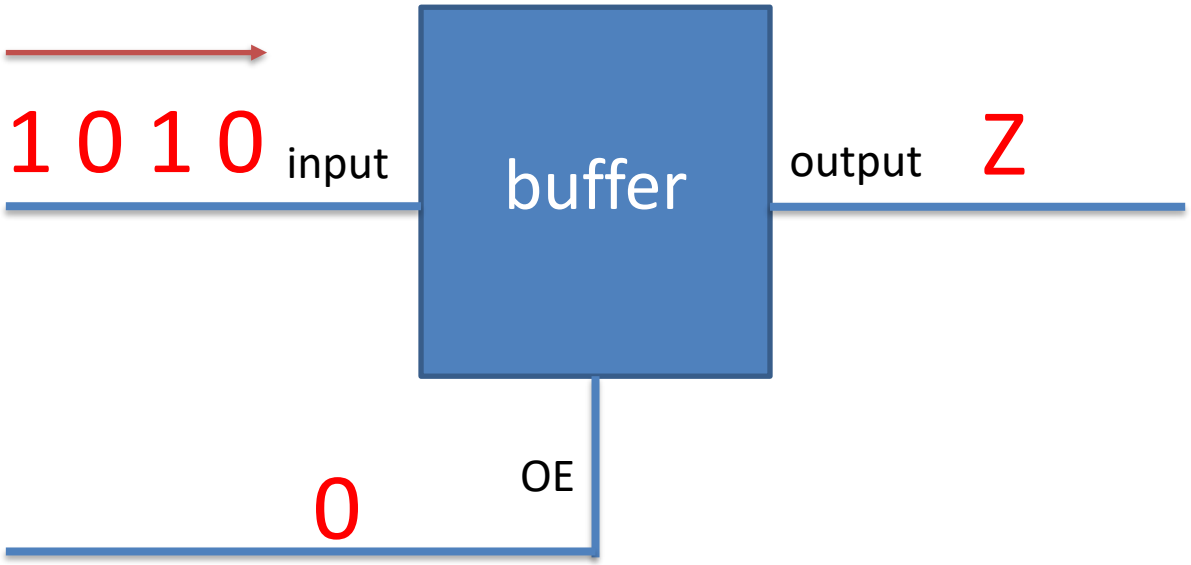
Latch circuit functions

- Holds data from the input signals
- Controls data retention using a clock or enable pin
- Includes an output enable pin that control on/off state of the output signal

Buffer circuit functions

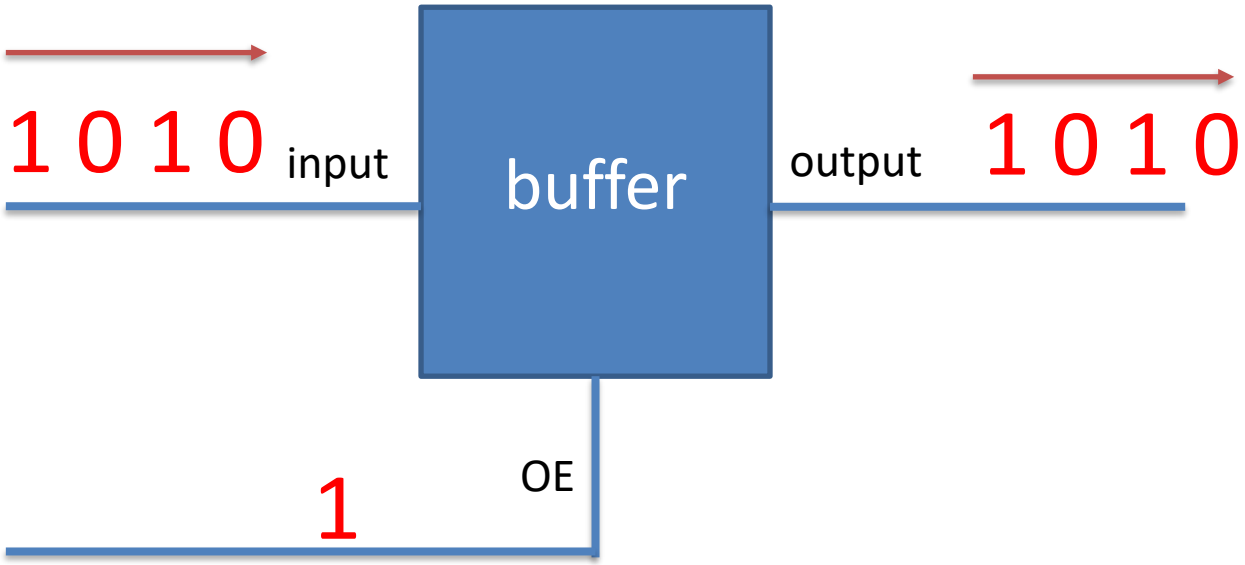
- No hold data
- Pass through data by amplifying the signal
- Some buffer has an enable pin that control on/off state of the output signal

Work of the buffer circuit

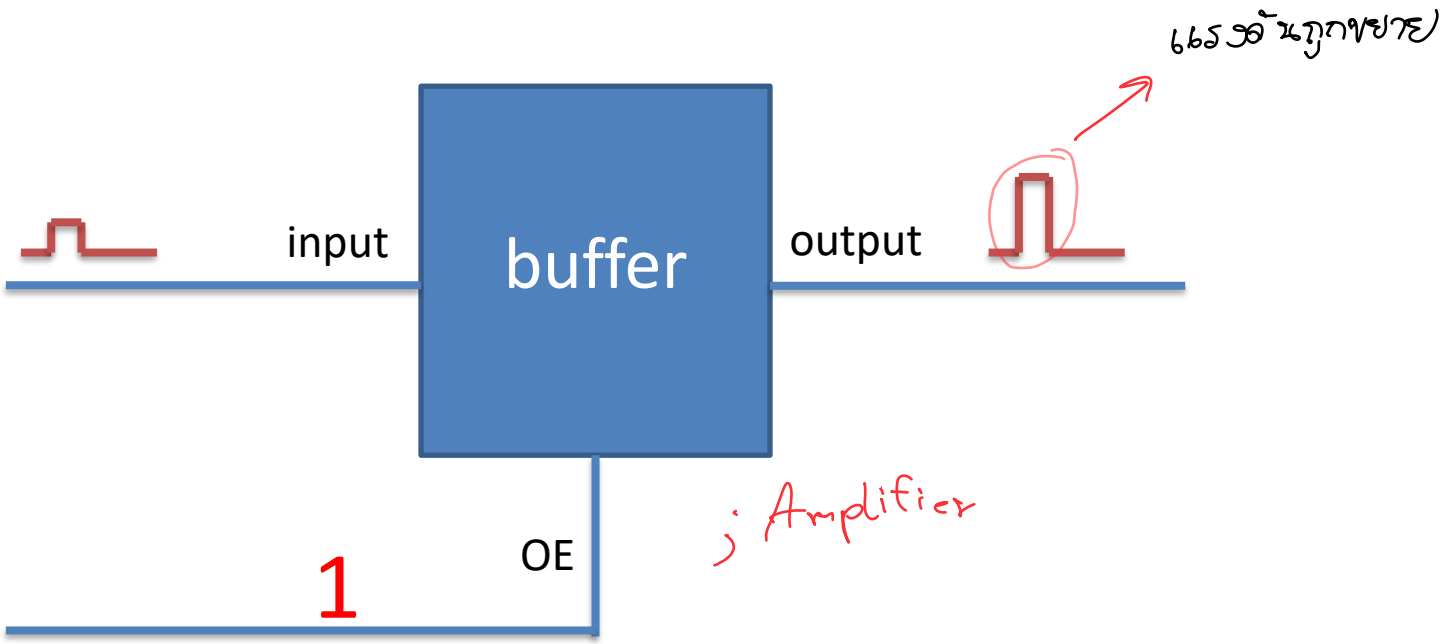


"Z" means a high-impedance state similar to the open circuit.

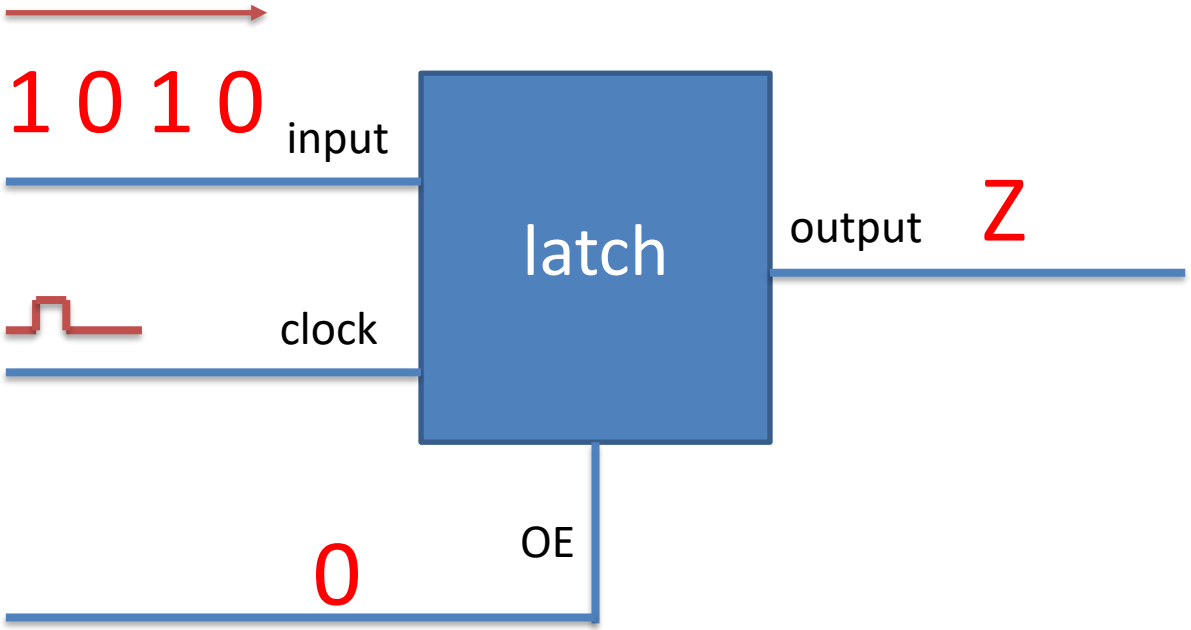
Work of the buffer circuit



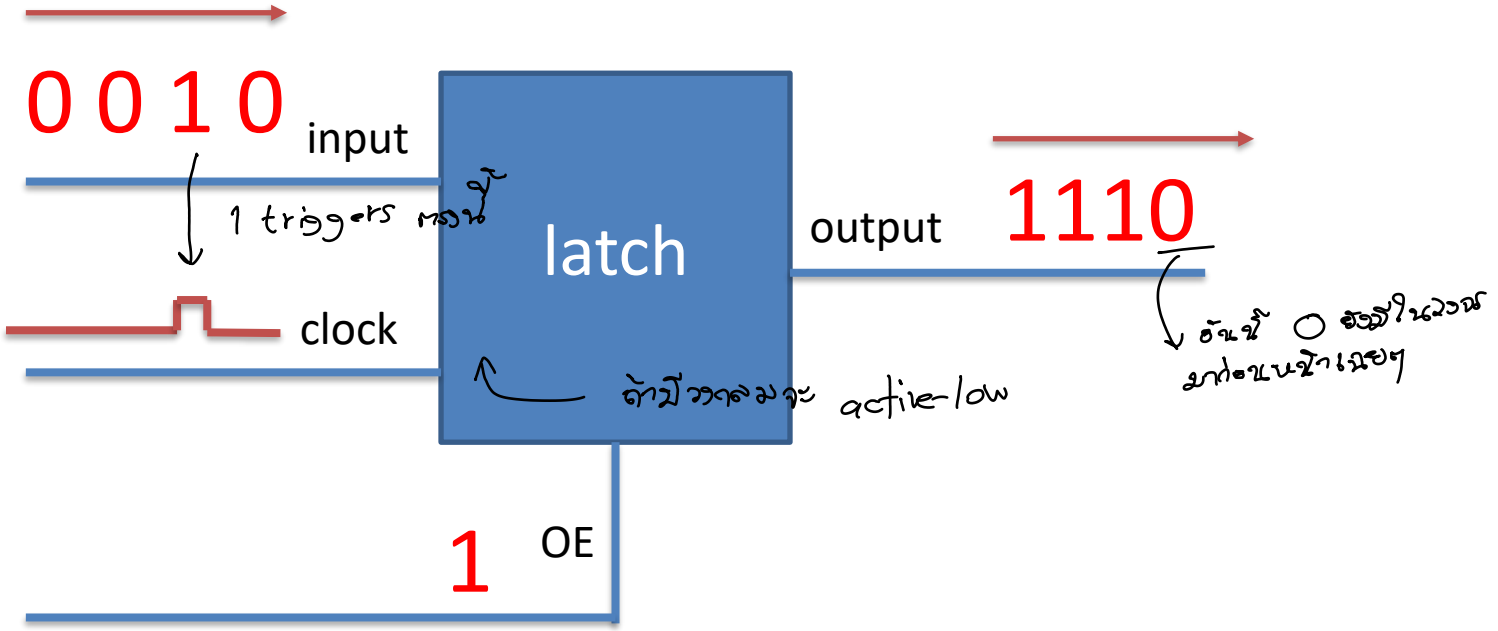
Work of the buffer circuit



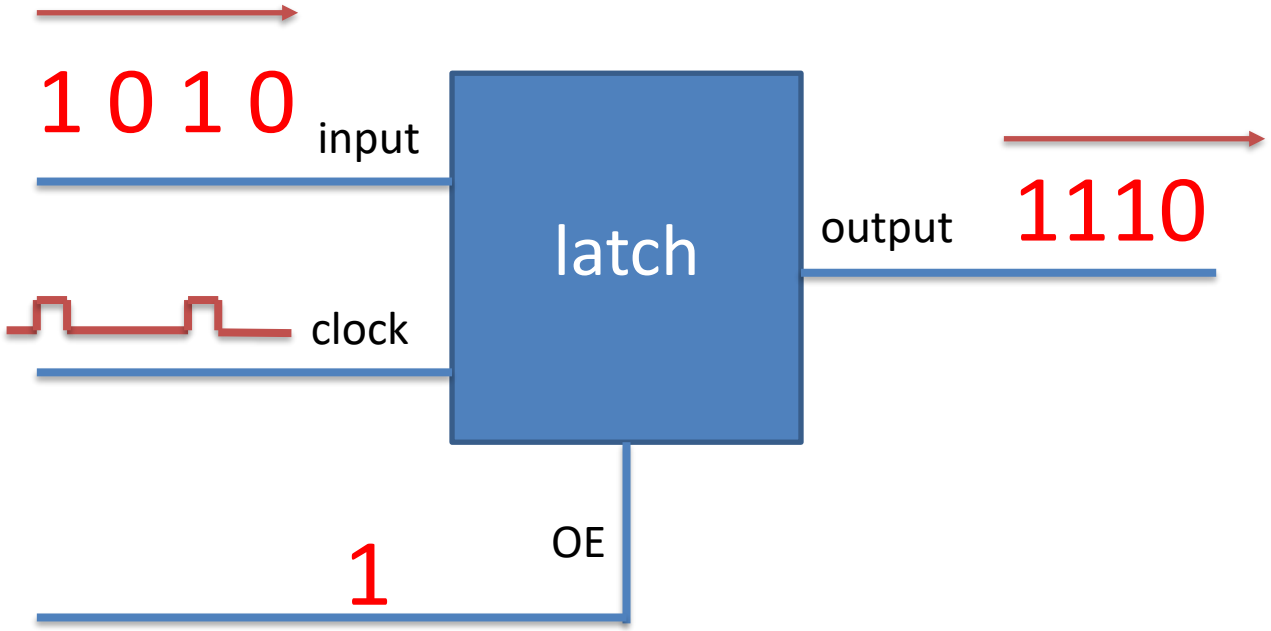
Work of the latch circuit



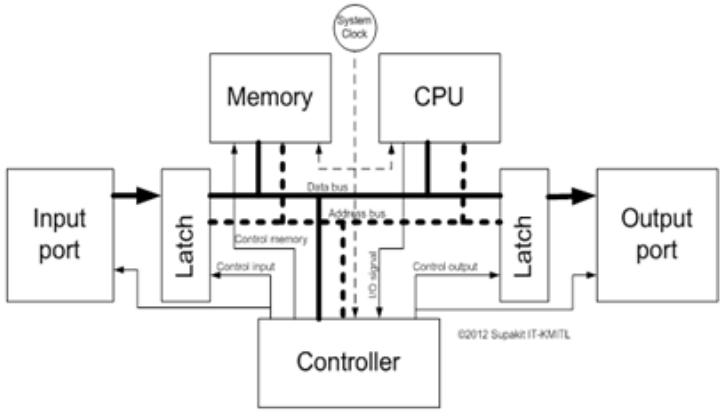
Work of the latch circuit

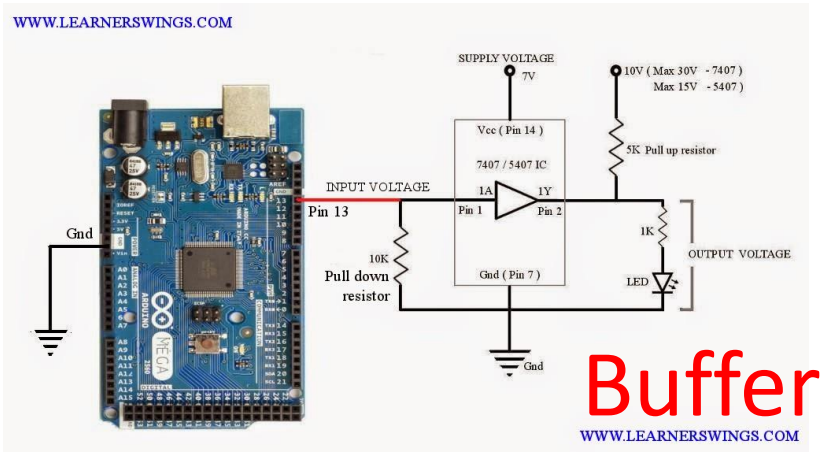


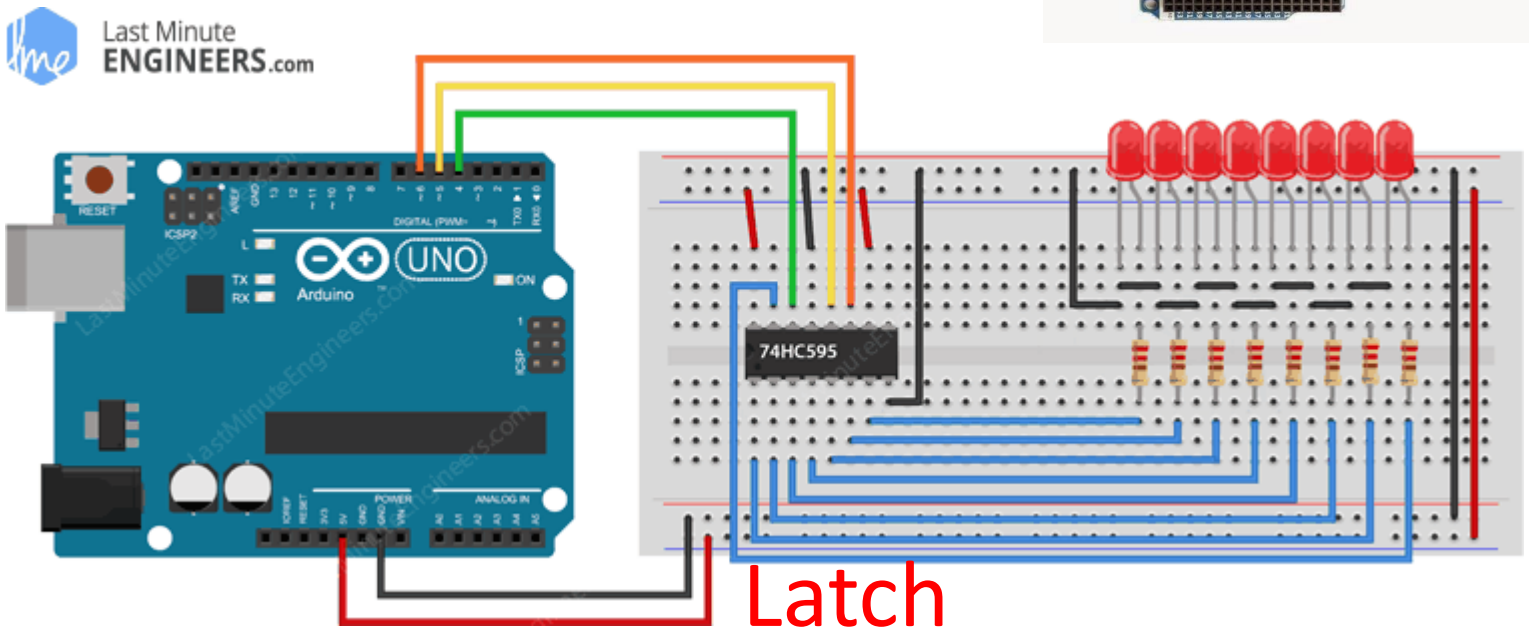
Work of the latch circuit



Latch/buffer in the computer





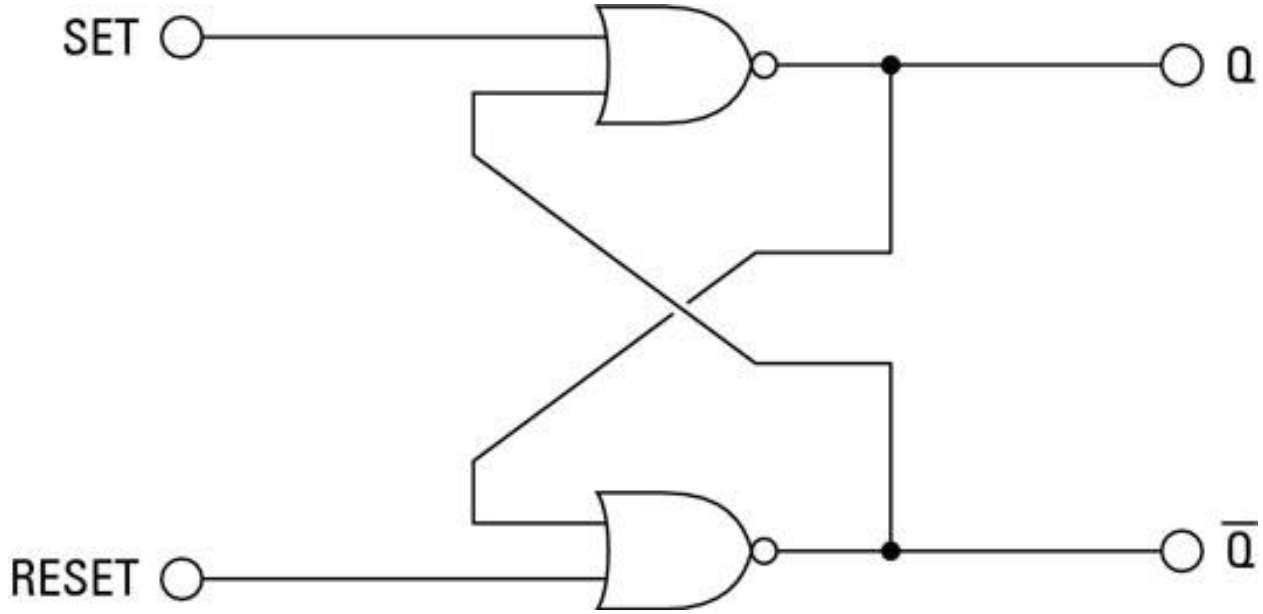


มาจาก Flip-Flop

↳ Latch → ต้นกำเนิด computer

SET-RESET FLIP-FLOP

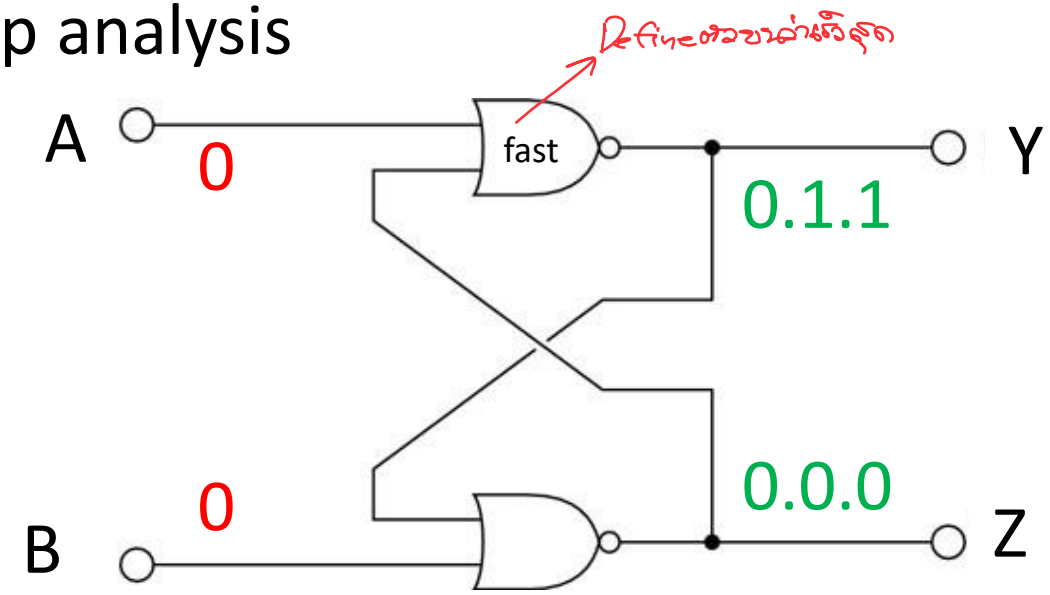
SR Flip-Flop truth table



S	R	Q	State
0	0	Previous state	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Forbidden

เป็น 1 เด็ดที่สุด

SR Flip-flop analysis



NOR

00 1

01 0

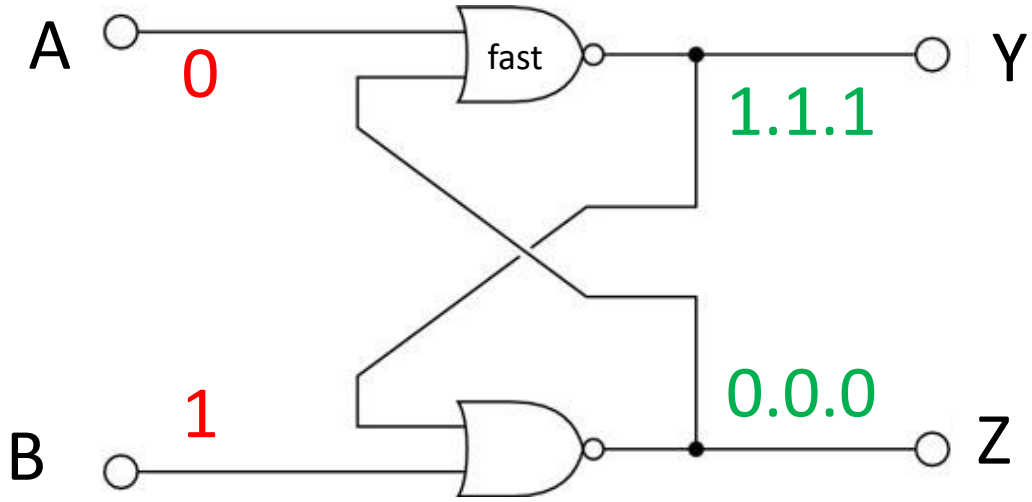
10 0

11 0

Step1

A	B	Y	Z
0	0	1	0
0	1		
0	0		
1	0		
0	0		
0	1		

SR Flip-flop analysis



NOR

00 1

01 0

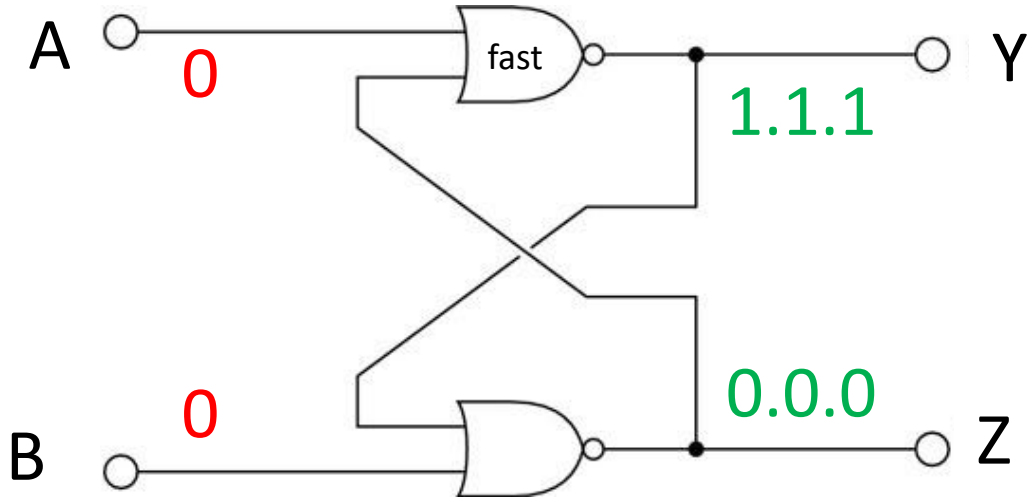
10 0

11 0

Step2

A	B	Y	Z
0	0	1	0
0	1	1	0
0	0		
1	0		
0	0		
0	1		

SR Flip-flop analysis



NOR

00 1

01 0

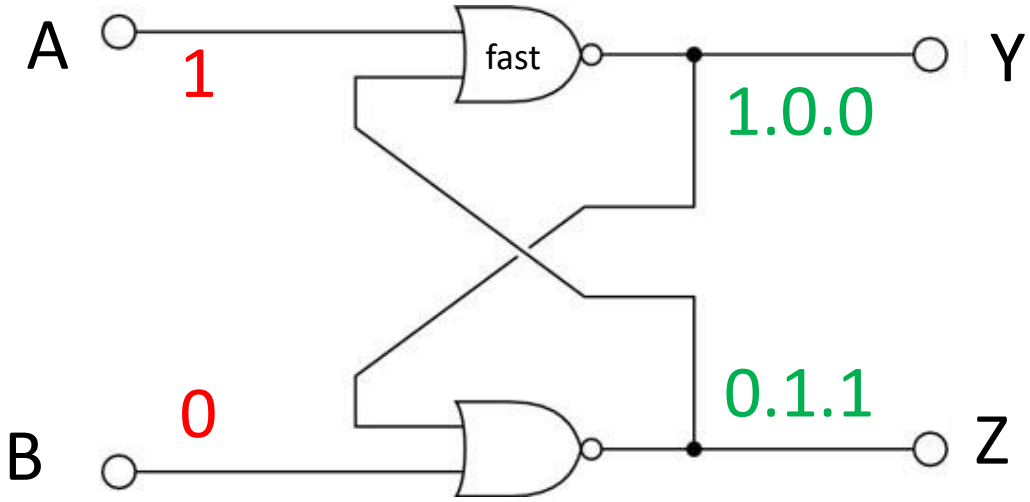
10 0

11 0

Step3

A	B	Y	Z
0	0	1	0
0	1	1	0
0	0	1	0
1	0		
0	0		
0	1		

SR Flip-flop analysis



NOR

00 1

01 0

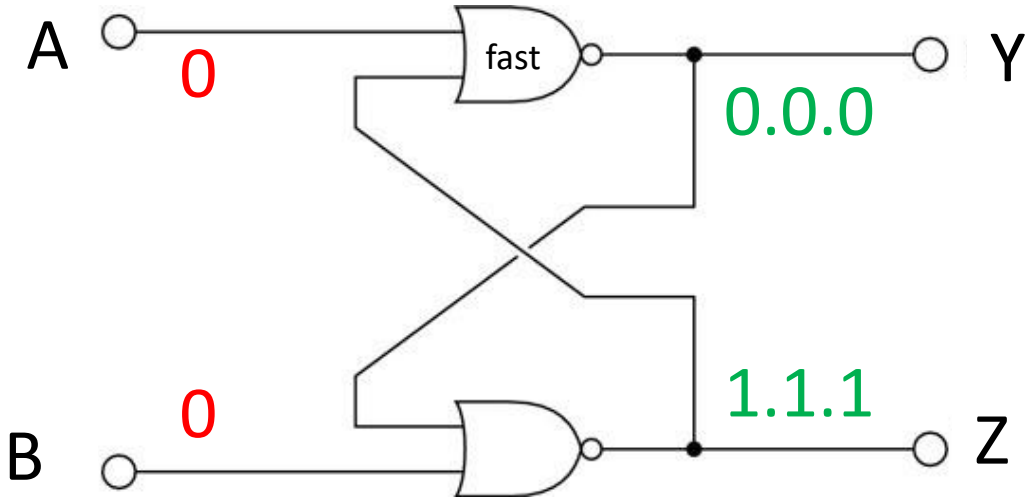
10 0

11 0

Step4

A	B	Y	Z
0	0	1	0
0	1	1	0
0	0	1	0
1	0	0	1
0	0		
0	1		

SR Flip-flop analysis



NOR

00 1

01 0

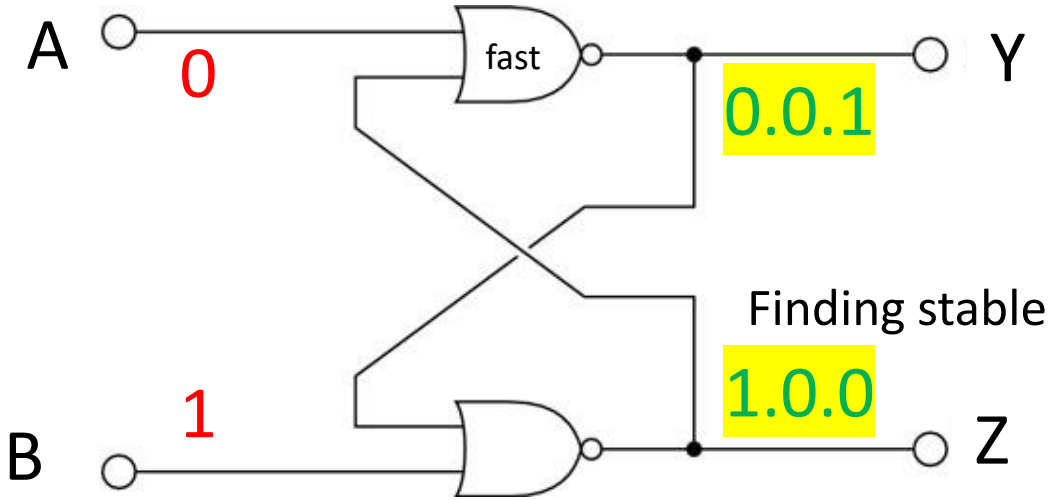
10 0

11 0

Step5

A	B	Y	Z
0	0	1	0
0	1	1	0
0	0	1	0
1	0	0	1
0	0	0	1
0	1		

SR Flip-flop analysis



NOR

00 1

01 0

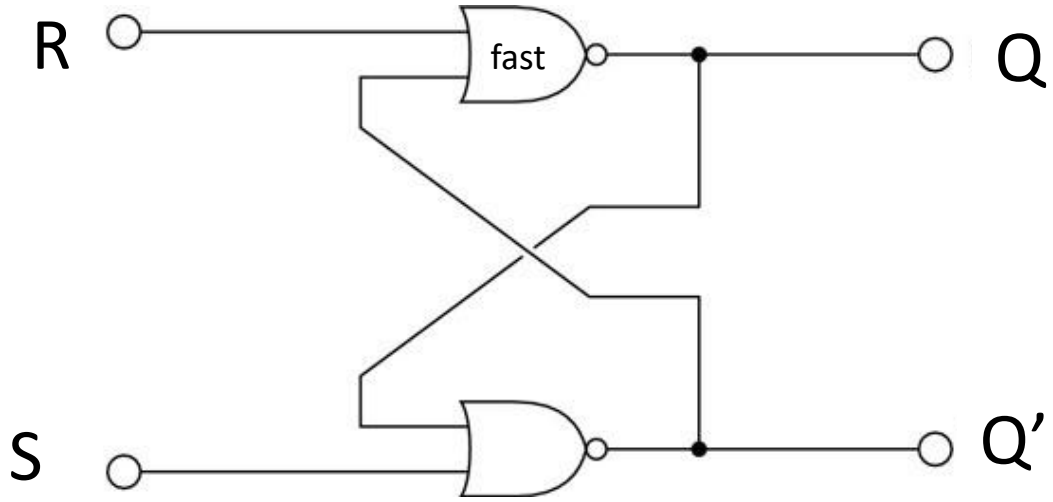
10 0

11 0

A	B	Y	Z
0	0	1	0
0	1	1	0
0	0	1	0
1	0	0	1
0	0	0	1
0	1	1	0

Step6

Truth table of SET/RESET – Flip Flop



NOR

00 1

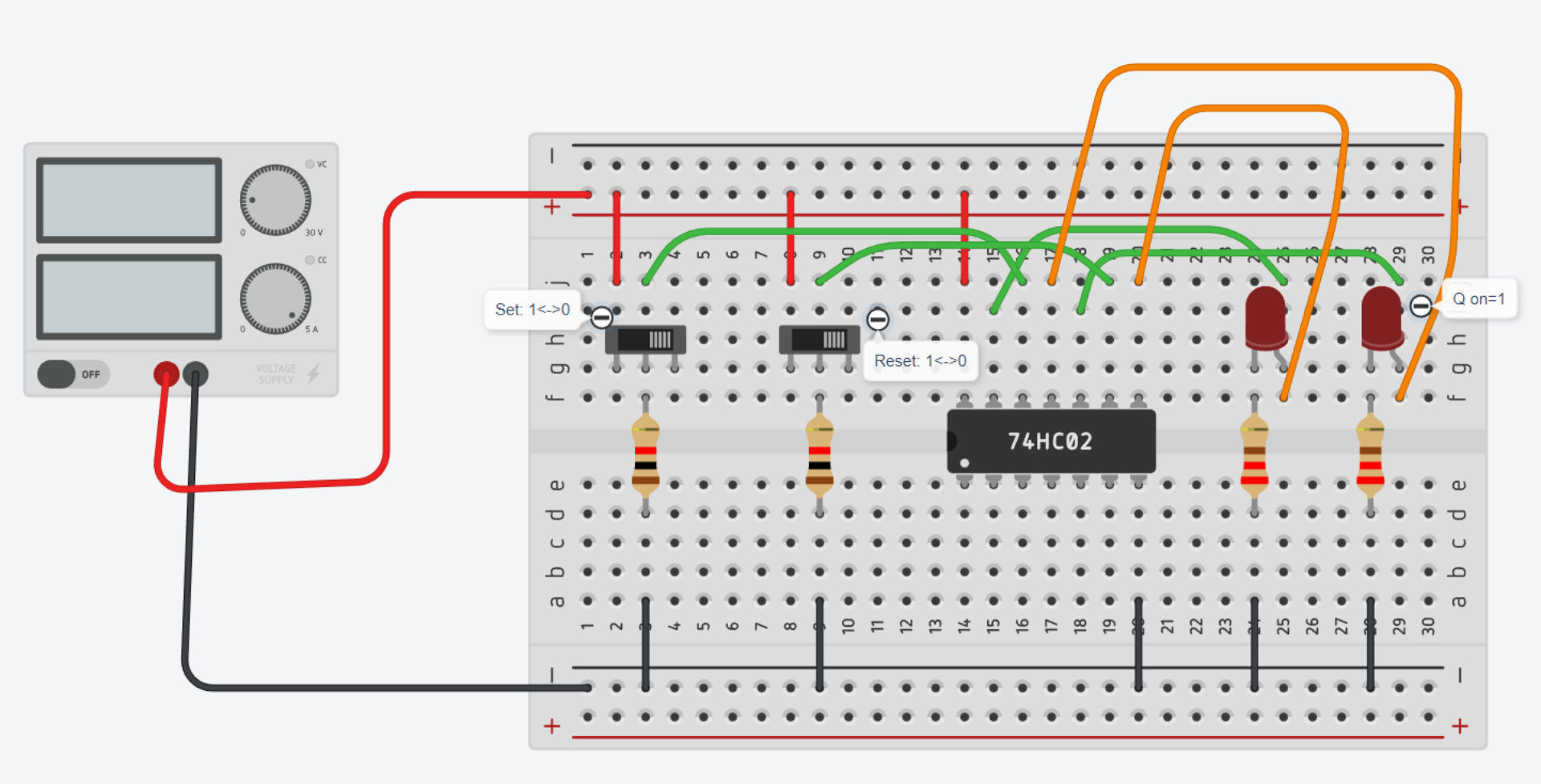
01 0

10 0

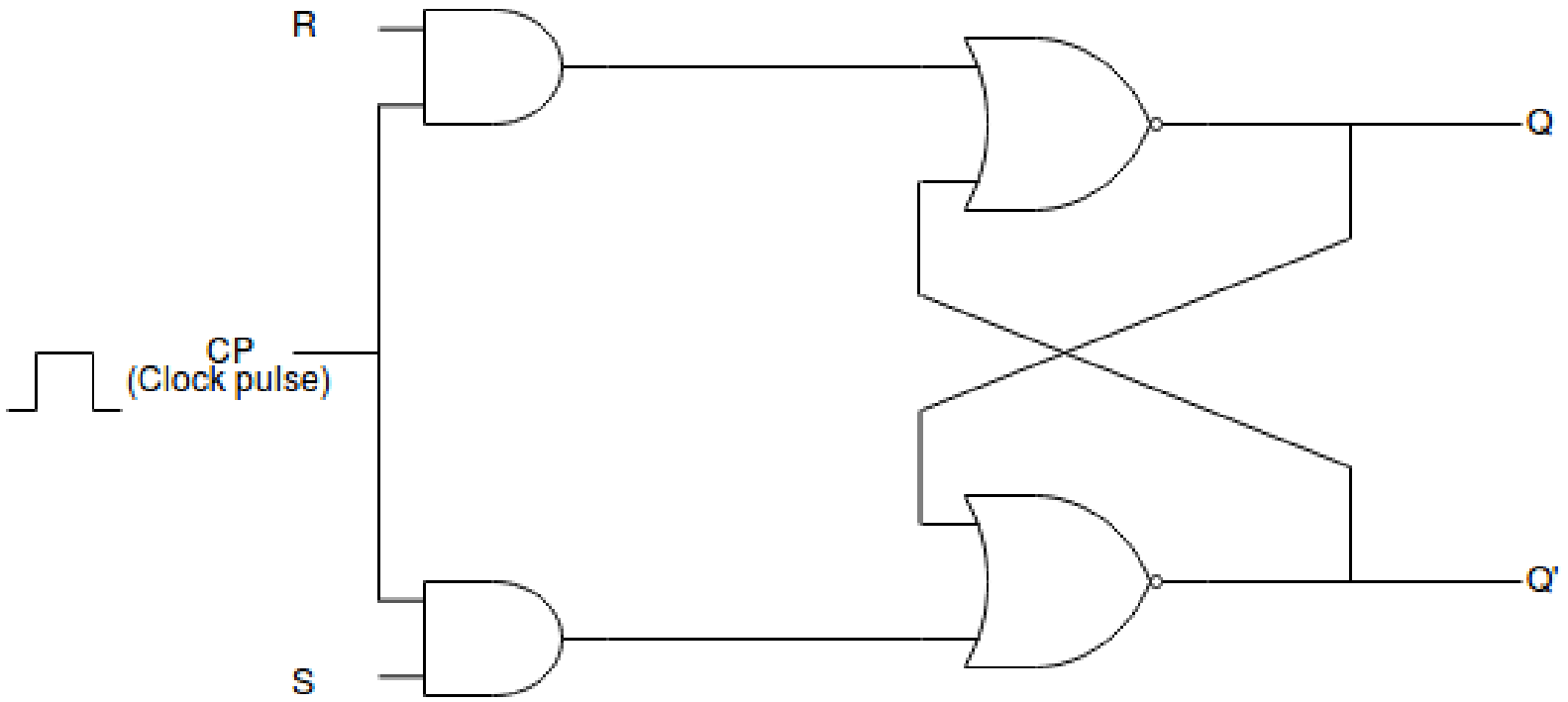
11 0

Reset	Set	Q	Q'	
0	0	1	0	
0	1	1	0	
0	0	1	0	No change
1	0	0	1	
0	0	0	1	No change
0	1	1	0	

Activity 3.1 Build the SR flipflop on ThinkerCAD



Activity 3.2 Build the SR flipflop with clock on ThinkerCAD



Reference