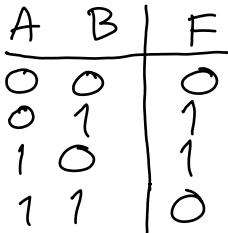
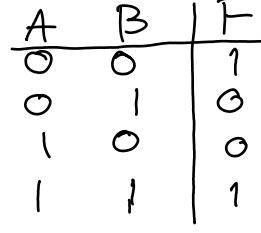


ICS Lecture

Boolean	AND	OR	NOT	NAND	NOR
Logic Gate	$A \cdot B$	$A+B$	\bar{A}	$\overline{A \cdot B}$	$\overline{A+B}$
$\overline{AB+AB}$	XOR	XNOR	$\overline{\bar{A}B+A\bar{B}}$		
$A \oplus B$		$\overline{A \oplus B}$			
					
$\text{output} = 1$			$\text{output} = 0$		
					

ເວລາລຽນຢູ່ນັ້ນ
term ກົດຕັ້ງສ່ວນ
ເຫັນວິທະຍະ

Boolean Algebra Laws & Properties (ກົດຕັ້ງ)

1. $A + BC = (A+B)(A+C)$

2. $A(B+C) = AB+AC$

13. $AB + A\bar{B} = A$
 $A(B + \bar{B}) = A \cdot 1 = A$

14. $A + AB = A$
 $A(1+B) = A \cdot 1 = A$

15. $A + \bar{A}B = A + B$
 $(A + \bar{A})(A + B) = 1 \cdot (A + B) = A + B$

Identity

3. $A + 0 = A$

4. $A + 1 = 1$

5. $A \cdot 1 = A$

6. $A \cdot 0 = 0$

7. $A + \bar{A} = 1$

8. $A\bar{A} = 0$

9. $A + A = A$

10. $A \cdot A = A$

De Morgan's Laws

11. $\overline{A+B} = \bar{A}\bar{B}$

12. $\overline{AB} = \bar{A} + \bar{B}$

ອະນາຍ NOT ໃລ້ວ OR \rightarrow AND, AND \rightarrow OR

Binary

0110
 $\begin{matrix} \uparrow & \uparrow & \uparrow & \uparrow \\ 3 & 2 & 2 & 1 \end{matrix}$
 ดูอย่างนี้ 1 หลัง 0

$$2^2 + 2^1 = 5$$

$$0110_2 = 5_{10}$$

Decimal \rightarrow Binary

ex. 59 ตัวเลข 2^n ที่ 9 จัดสูตรแล้วจะเป็นอย่างไร

$$\begin{array}{r} 59-32=37 \\ \downarrow \text{เหลือ } 27-16 \\ \downarrow 11 \\ \downarrow 3 \rightarrow 2+1 \end{array} \quad \begin{array}{r} = 32 + 16 + 8 + 2 + 1 \\ 1 \quad 1 \quad 1 \quad 0 \quad 1 \quad 1 \\ \downarrow 2^4 \\ 11 \\ 3 \rightarrow 2+1 \end{array} \quad \Rightarrow \text{งบประมาณตัว數 Binary}$$

$$\begin{array}{r} 11 \\ 11011 \end{array}$$

(จะต้องคำนวณ)

Hexadecimal

Hex \rightarrow Dec

A \rightarrow 10
B \rightarrow 11
C \rightarrow 12
D \rightarrow 13
E \rightarrow 14
F \rightarrow 15

ตัวอักษร 15 ตัวเลข 16 ตัว 0 ตัว

3A5 16 ตัว ก่อตัวบวก 1 ตัวบวก

$$= (3 \cdot 16^2) + (A \cdot 16^1) + (5 \cdot 16^0)$$

$$= 768 + 160 + 5 = 933$$

Hex \rightarrow Bin

(A=10)
 16 บวกๆ 4 บิต แล้วต่อไป 4 บิต

$$\begin{array}{r} A9 \\ \downarrow 16 \\ 1010 \end{array} \quad 1001 \quad A9_{16} = 10101001_2$$

Dec \rightarrow Hex

$$16 \cdot 23 = 368$$

368₁₀

$$\begin{array}{r} 382 \\ \downarrow 16 \\ 23 \\ \downarrow 16 \\ 1 \\ \hline 0 \end{array}$$

Remainder \rightarrow 14
 คำนวณเหลือทุก步
 Remainder \rightarrow 7
 Remainder \rightarrow 1
 ดูตัวล่าง \rightarrow ฐาน

Ans. 17E

Bin \rightarrow Hex

11001100

$\hookrightarrow CC_{16}$

01110110

$\hookrightarrow 76_{16}$

Grouping 4 bit
 Binary - 4 bit

Canonical Form

\hookrightarrow SOP; Sum of Product

\hookrightarrow POS; Product of Sum

SOP

- ผล Output ที่เป็น 1 มาก่อน

- Input ของ Output ที่สามารถเขียน

ด้วย 1 ไม่ได้ NOT

ด้วย 0 ได้ NOT

POS

- Output ที่เป็น 0 มาก่อน

- Input ของ Output ที่เป็น 0 ไม่ได้ NOT
 ด้วย 1 ได้ NOT

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

$$F(A, B) = (A+B)(\bar{A}+\bar{B})$$

$$\begin{array}{l} \text{Minterm} \\ \text{M}_0 \cdot M_3 \\ = \prod M(0, 3) \end{array}$$

$$\begin{array}{c|cc|c}
A & B & F \\
\hline m_0 & 0 & 0 & 0 \\
m_1 & 0 & 1 & 1 \\
m_2 & 1 & 0 & 1 \\
m_3 & 1 & 1 & 0
\end{array} \quad F(A, B) = \bar{A}\bar{B} + A\bar{B} + \bar{A}B$$

Minterms

$$\begin{array}{c|cc|c}
A & B & F \\
\hline m_0 & 0 & 0 & 0 \\
m_1 & 0 & 1 & 1 \\
m_2 & 1 & 0 & 1 \\
m_3 & 1 & 1 & 0
\end{array} \quad F(A, B) = M_1 + M_2 = \sum m(1, 2)$$

ຮາບັດສິນໄປ່ມາຮະຫວັດວ່າ SOP ດັບ POS ຍັງ

ex. $F(A, B, C) = \sum m(1, 3, 5, 6, 7) = \prod M(0, 2, 4)$

ຕົວກີ່ໄວ້ໂດຍຊື່ໃນນັ້ນກະຊວງໃນ POS ເພື່ອ

Don't Cares

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	x
1	1	0	x
1	1	1	x

$$F(A, B, C) = M_1 + M_3 + M_4 + d_5 + d_6 + d_7$$

$$= \sum m(1, 3, 4) + \sum d(5, 6, 7)$$

↑ Don't Cares

ຂວາງຕົວໄວ້ລົບມີຄ່າ
Input 3 ຕ້ອນລົບ
ຄວາມຖີ່ມີຄ່າ

Karnaugh Map; K-Map

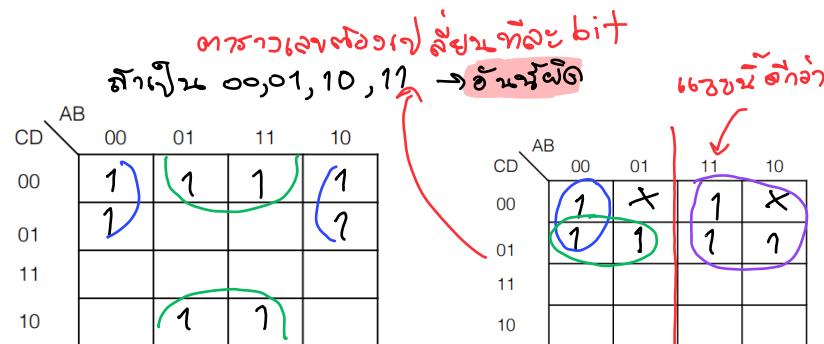
- ອຸ່ນ Output ມາ Truth table ພາບໃຈຈຳກັດໄວ້

- Group 1 ອູ້ຈຳເປັກກົດ ອູ້ຈຳກັດ 2^n - Overlap ດັບໂດຍ

Grouping ທີ່ພລາຍຂ່ອງຍ່າ

CD	AB	00	01	11	10
00	1)				(1)
01					
11					
10	1)			(1)	

4 ຂູ້ນຸ່ງຂັ້ນ → Group ປົດ



ຢາມ/ຄ່າ → Group ປົດ

CD	AB	00	01	11	10
00	1)			1)	
01	1)				
11					
10					

ລັບມີ Don't Cares ແລ້ວ
Group ເພີ້ມມີມີ້ໄດ້ມີລົບມີມີ້
ສັນລັບ → ໄດ້ຕ້າວ່າໄດ້ມີ້ Group ກີ່ໄວ້ນີ້ນີ້

Two-bit Comparator

ເລືດ ເຖິງນິຍົມຂອງຕະຫຼາດນີ້

↪ Return ເຖິງ 0 (False), 1 (True)

A	B	C	D	F1	F2	F3
0	0	0	0	1	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0

ກ່ຽວຂ້ອງປະເພດນີ້

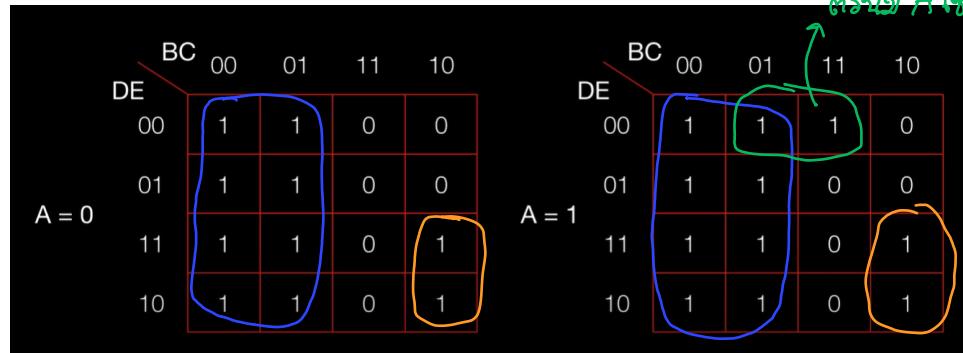
- F1 ເຊື້ອວກ AB == CD

- F2 ເຊື້ອວກ AB < CD

- F3 ເຊື້ອວກ AB > CD

ຈະນີ້ເວັບໄປໃຫ້ຮັກກຳນົດໄລ່
ຈຳກັດວ່າສາມາດນີ້ → 1
ດັວິ່ງຈຶ່ງ → 0

Five Variables K-map

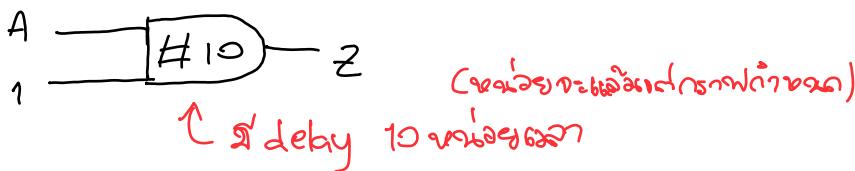


$$F = \overline{B} + \overline{B}\overline{C}D + A\overline{C}\overline{D}\overline{E}$$

ຕັດຫຸ້ມ A ເຊື້ອວກເລື່ອງທີ່ໃຫ້ກຳນົດກວດໃນນີ້

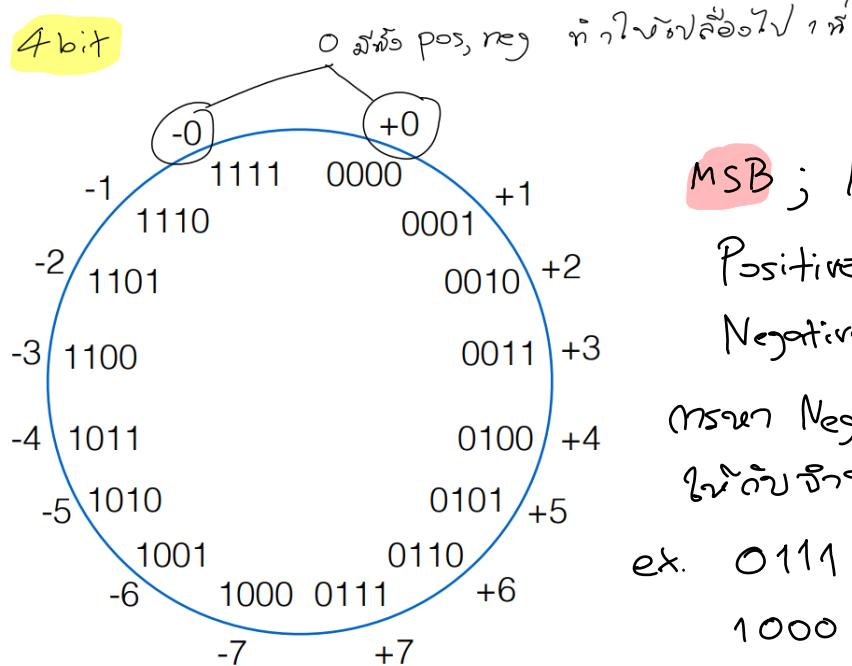
Gate Delay

- ອັນ output ຂອງ logic gate ໄວສຳເນົາດາວໂຫຼວດ
ໄລດ້ກັນກີ ດາວວິດໄດ້ delay ຮະດິນ nanosecond



Number System

One's Complement - System



- ວິທີ \rightarrow 66 ໂະ -6
- ລາຍງານຂອງລົບ ຕະຍເລາ
ກົກລະນະນຸກຫຼັກຕະການນາໄສ compliment
- ສິວທະລູນເກົ່ານົບວ່າວານວັດເພີ່ມ

ເປົ້າ sign bit +
(ເຄື່ອງນັບ)

MSB ; Most significant bit ຜົກຫ້າຍຮຸດ

Positive \rightarrow 0 ເປົ້າ MSB

Negative \rightarrow 1 ເປົ້າ MSB

ມຽນ Negative num ຖໍາໄດ້ໄດຍໍໃນ compliment
ໃນຕົວນີ້ມີ Positive

ex. 0111 (+7) ສະ compliment ຈະໄວ້
1000 (-7)

Addition in One's Complement System

$$\begin{array}{r}
 (+4) \quad 0100 \\
 (-3) \quad \underline{1100} \\
 \hline
 0000
 \end{array} +$$

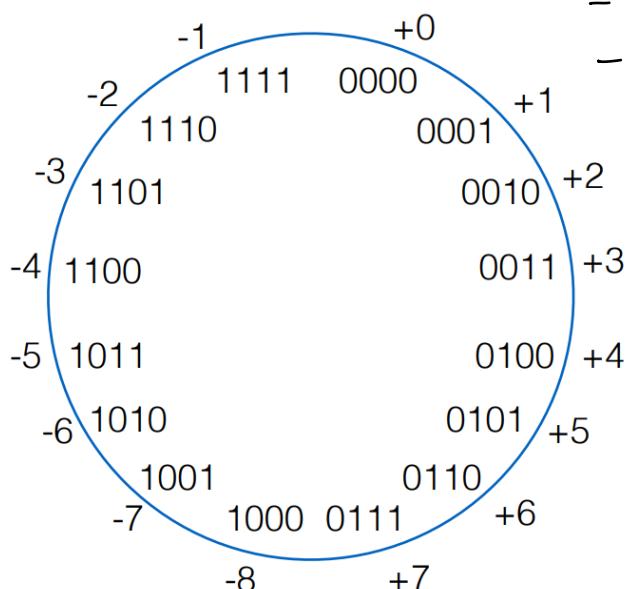
1 ການຫັດລື້ອນ
 ເບີ່ອານກົງກົດວ່າ

$$\begin{array}{r}
 (-4) \quad \begin{matrix} 1 \\ 0 \\ 11 \end{matrix} \\
 (+3) \quad \underline{\begin{matrix} 00 \\ 11 \end{matrix}} \\
 \hline
 \begin{matrix} 1 \\ 1 \\ 10 \end{matrix}
 \end{array} +$$

1+1=0 ແລະ ອັກກົດ 1
 ເລີ່ມຈຳດັດ 1

$$\begin{array}{r}
 1011 \\
 1100 \\
 \hline
 0111 \\
 \hline
 1000
 \end{array} +$$

Two's Complement System



- ໄວ້ລົດ -0 ແລ້ວ, ອື່ນຕໍ່ +0
- ເນື້ນ -8 ເຈົ້າ
- Addition ຕ້ອກຄົ່ນຂະໜາດ
ເຖິງຕັດໄປໄລ້ແລ້ຍ

Sign bit

0 ເປົ້າ Positive
1 ເປົ້າ Negative
(ເຫັນ One's Complement)

ການຈາກໃຈຂະໜາດ Negative ຂໍາໄລ້ໂລຍ້ນ ຫາ Compliment
ຂຽນຂະໜາດກີ່ມີສຳເນົາ Magnitude ຢັດວັດທີ ແລ້ວ +1

Addition in Two's Complement

ຕ້ອກຄົ່ນຂະໜາດ
ຄັດຫົ່ງ

$$\begin{array}{r} 1 \\ \hline 1100 \\ + (-4) \\ \hline 1101 \\ + (-3) \\ \hline \underline{\underline{1001}} \\ (-7) \end{array}$$

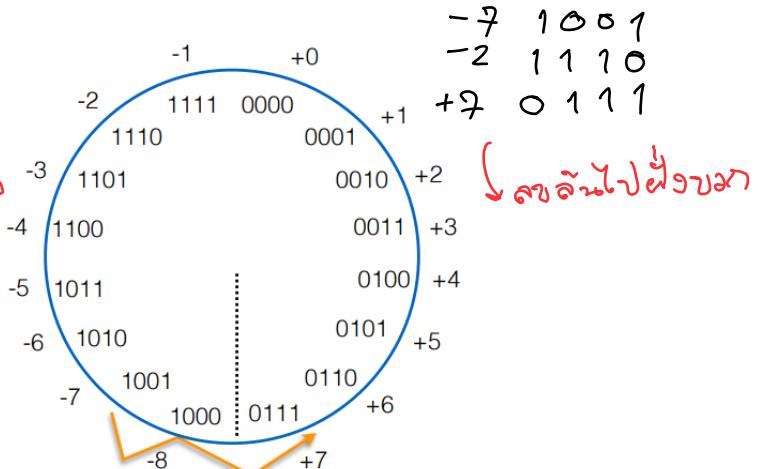
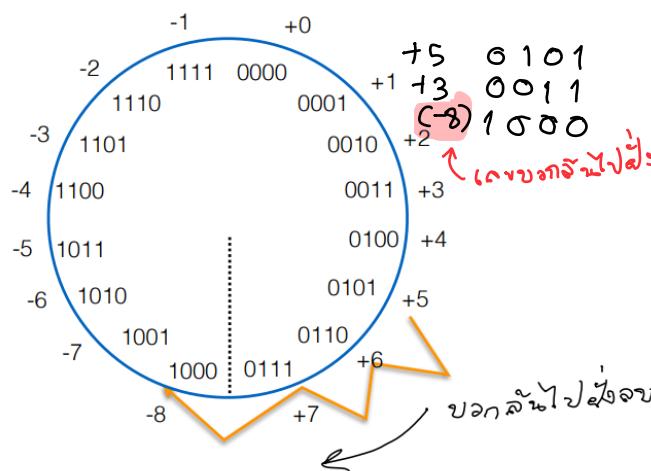
$$\begin{array}{r} 0101 \\ + (+5) \\ \hline 1011 \\ + (-5) \\ \hline \underline{\underline{0000}} \\ \end{array}$$

$$\begin{array}{r} \text{ແລ້ວຕ້ອນກີ່ມີສຳເນົາ } (-5) \\ \uparrow \\ 1011 \\ \downarrow \text{compliment} \\ 0100 \\ 1 \\ \hline 0101 \\ = (+5) \end{array}$$

Overflow

- ດົນ (+) + ດົນ (+) \rightarrow ດົນຫຼັງ (-)
- ດົນ (-) + ດົນ (-) \rightarrow ດົນຫຼັງ (+)

- ຄົ້ນ Bit ຈຶກຕົວ Overflow ຈະເກີດໄດ້ນັ້ນຊອນ
- ຈຳກັດກົບອັດກິນໃຫຍ່ລູ່ເດືອນກ່າວຮັບຈະວຸນວັນ (ເລືອນ Two's Complement
ວິຈິດຕັດ)



Checking For Overflow

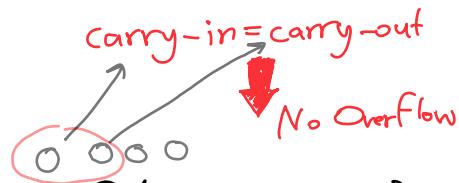
- 607 Gate XOR ຂາງຮະຍຸກຕິຫຼືສຳ

- ເນັ້ນໄວ່ເດີຕ່າງOverflow ກົດ

- ບັນ Carry-in \neq Carry-out \rightarrow ຕີດOverflow

carry-out (ຄວາມປັບປຸງທີ່ຕົວນັ້ນ)

$$\begin{array}{r}
 \text{carry-in} \quad (\text{ຄວາມປັບປຸງ}) \\
 \text{carry-in} \quad (\text{ຄວາມປັບປຸງ}) \\
 \begin{array}{r}
 \text{0 } 1 \quad 1 \quad 1 \\
 \text{0 } 1 \quad 0 \quad 1 \\
 \hline
 \text{0 } 0 \quad 1 \quad 1 \\
 \hline
 \text{1 } 0 \quad 0 \quad 0
 \end{array} \\
 (+5) \quad \downarrow \quad \text{ຕີດ overflow} \\
 (+3) \quad \quad \quad \\
 (-8)
 \end{array}$$

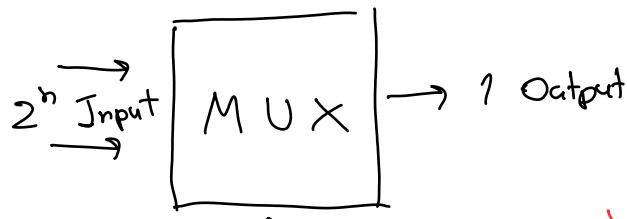


$$\begin{array}{r}
 \text{0 } 1 \quad 0 \quad 0 \\
 \text{0 } 1 \quad 0 \quad 1 \\
 \hline
 \text{0 } 1 \quad 1 \quad 1
 \end{array} \quad (+5) \quad (+2) \quad (+7)$$

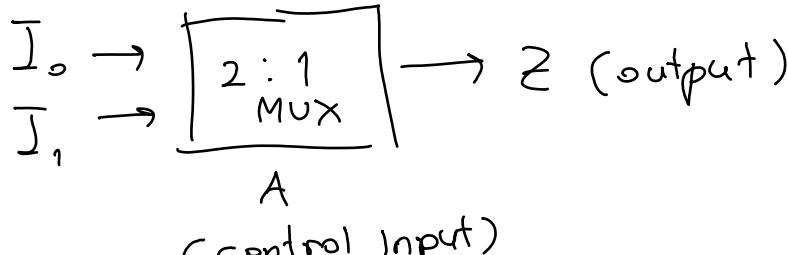
MUX ; Multiplexer / Selector

- ສູນ data ຂະຍຸຕົວ, ມີຂາຍ control input, output ນອກ 1 ອົກ

- 2^n Data Input, n control input, 1 Data Output



2 input
2 : 1 Mux (MUX ແບບຍໍ່ຍິ່ງ)



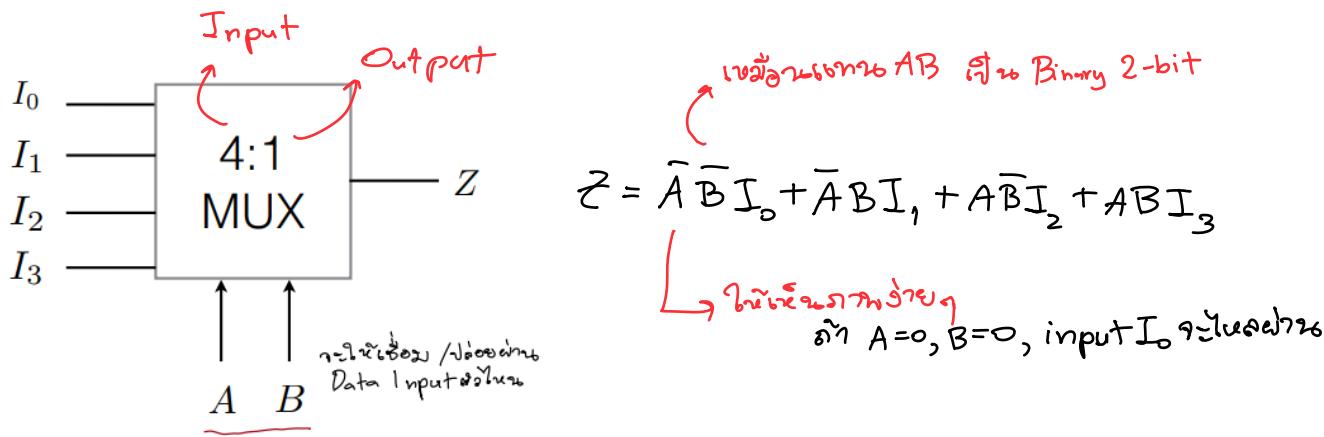
ເລີ່ມຕົ້ນ A ເຖິງໂຕຣິຍ (I in Binary)
Output ດີຈະຈົບຕັ້ງ I (I in Binary ລົ້ມ)
Input ນອກ A (n) ທີ່ກິ່ນໄຫວ output (Z)
ສົ່ງຕັ້ງ I_n

		A ເຖິງ 0 ລົ້ມ ກິ່ນໄຫວ	Z
I ₁	I ₀	A	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

A ເຖິງ 1
output ສົ່ງຕັ້ງ I,
Z ລົບຍື່ນ 0

ເຈົ້າມືຂົນ SOP
ຊັ້ນ A ເຖິງ 0/1

$$\begin{array}{r}
 \text{A} \quad \text{Z} \\
 \hline
 0 \quad I_0 \\
 1 \quad I_1
 \end{array} \quad Z = \bar{A}I_0 + A I_1, \quad (\text{ສາມດັກ NOT})$$



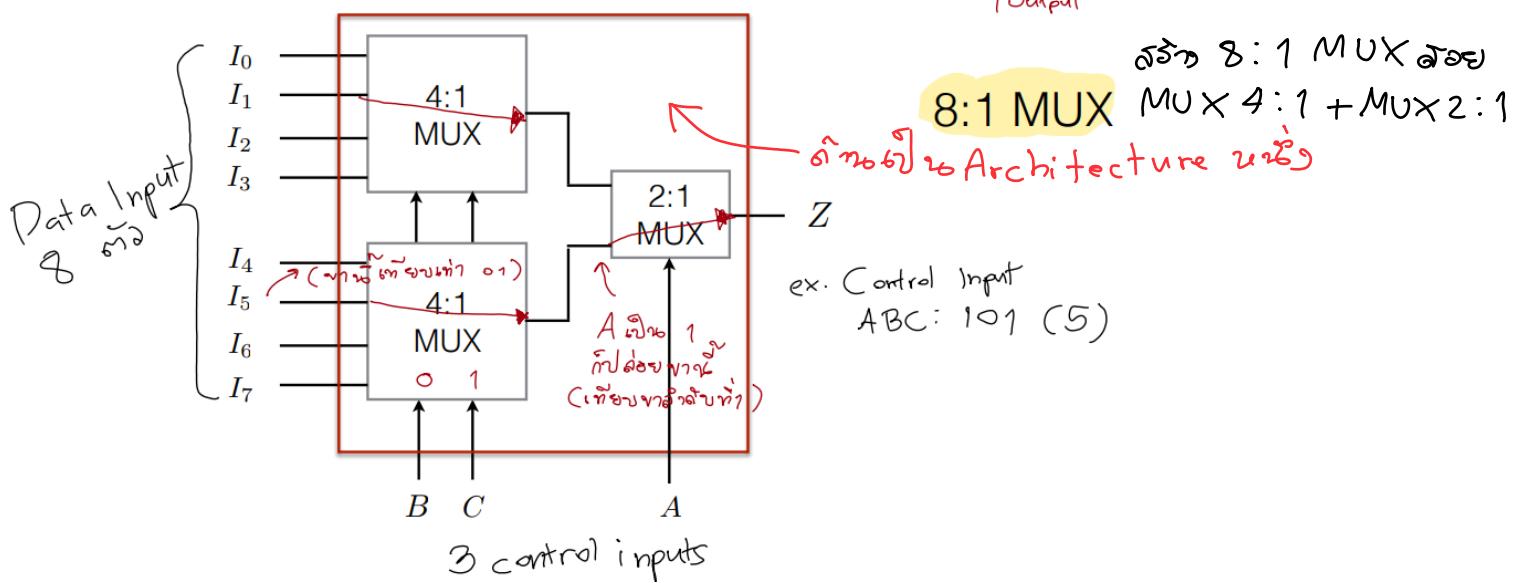
2^n : 1 MUX သီဆိုရှိနိုင်

$$Z = \sum_{k=0}^{2^n-1} m_k \cdot I_k$$

m_k ပါ ၁။ k-th သူ၏ control input

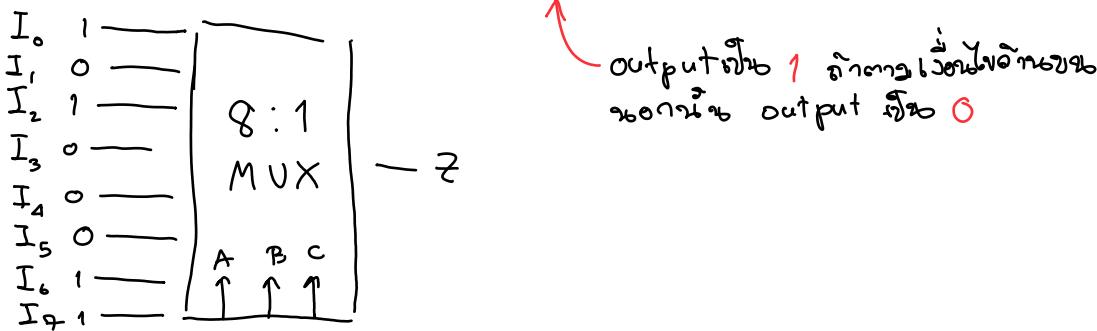
- ရေစာမျက်နှာ အတွက် 8:1 MUX ဖြစ်လိုက်နိုင်

ပုဂ္ဂန်တော် (ပုဂ္ဂန်တော်) ဖြစ်လိုက် 8:1 MUX မှာ 8 Data Input, 3 Control Input, 1 Output



MUX as Logic Building Block

- မြတ် MUX သီဆိုနိုင်သူ၏ SOP
 - 6 ခုခု I_i တဲ့ ဒါ ၁ လာမ်းကို သီဆိုနိုင်၏ minterm_i, တော်မှာ ဒါ ၀
- ex. $F(A, B, C) = m_0 + m_2 + m_6 + m_7 = \bar{A}\bar{B}\bar{C} + \bar{A}BC + AB\bar{C} + ABC$



Smaller Design of MUX

- ລົກວຽກໃນເລືອດໄລ້ຕໍ່ອັງຍານແຕ່ control input ເຊິ່ງຂອງລົກ

- ລະ control input ຍຸດ 1 ຕົວ

ຈົດກຳລົງສັງຕິພົມ, ພິຈານາ C

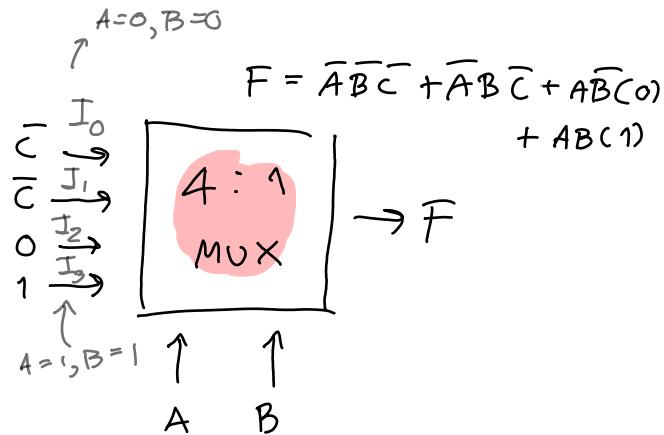
A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

ຮູບກໍາສັງຕິພົມ
ມີຄວາມສອນິຫຼົງ
ເນື້ອໃຈວ່າ $F = \bar{C}$ ດັວວັນຫຼຸງ

\bar{C}

0

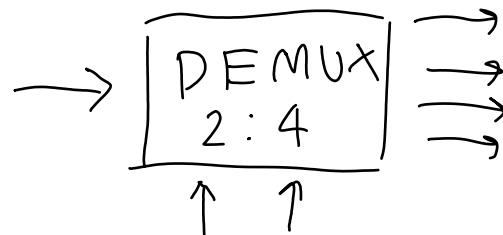
1



ຮູບ
ສຶກຮຽນທີ່ໄດ້ຮັບກໍານົດ Data Input n ຕົວ
 - ເລືອດອິນຸກ $n-1$ ຕີວາເປົ້າ control input
 - ອິນຸກ 1 ຕີວາທີ່ເປັນລົດ ຈະເຖິງ data input
 ບໍ່ມີ MUX ກ່ອນັດໆ 0 ແລະ 1

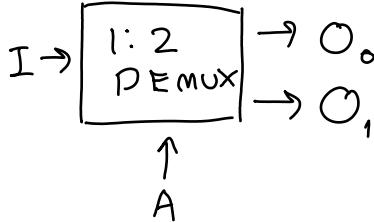
DEMUX; De multiplexer

- 1 Data Input
- n control signal
- 2^n output lines



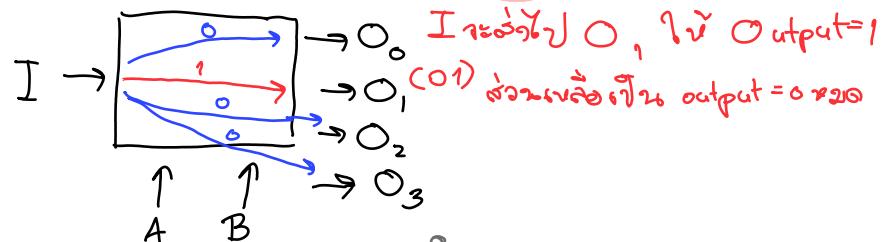
1 : 2 DEMUX

↑ control signal



2 : 4 DEMUX

ຮັບຂະໜາດ $A=0, B=1$



$$O_0 = \bar{A}I$$

$$O_1 = A\bar{I}$$

$$O_0 = \begin{matrix} \circ \\ \circ \\ 1 \end{matrix} \bar{A}I$$

$$O_1 = \begin{matrix} \circ \\ \circ \\ 1 \end{matrix} A\bar{I}$$

$$O_2 = \begin{matrix} 1 \\ \circ \\ \circ \end{matrix} A\bar{I}$$

$$O_3 = \begin{matrix} 1 \\ 1 \\ \circ \end{matrix} A\bar{I}$$