



Chapter4: Counter and DAC & ADC Part-I

Asst.Prof.Dr.Supakit Nootyaskool

Digital to Analog Converter

Objective

- Recognize the difference between rising edge/falling edge trigger.
- Explain the input, output, and truth table of the flip-flops.
- Understand the concept of frequency division circuit.
- Describe the process of counter circuit counting number up or down.
- Explain and illustrate the concept of conversion from analog signal to digital signal.

Topic

- Combinational logic vs Sequential logic circuit
- Rising/Falling edge trigger
- JK-flipflop
- D-flipflop
- T-flipflop
- Frequency division circuit
- First-in first-out circuit
- Counter circuit
- Analog signal to Digital signal concept

COMBINATIONAL LOGIC CIRCUIT AND SEQUENTIAL LOGIC CIRCUIT

To describe the difference between the combinational logic circuit and the sequential logic circuit.

World of digital logic circuit

Digital Circuit

Combinational
logic circuit

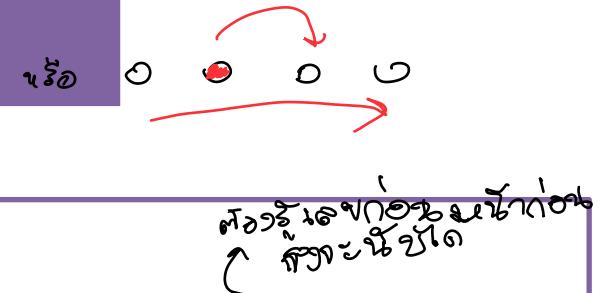
Sequential
logic circuit

Key characteristics

Combinational logic circuit

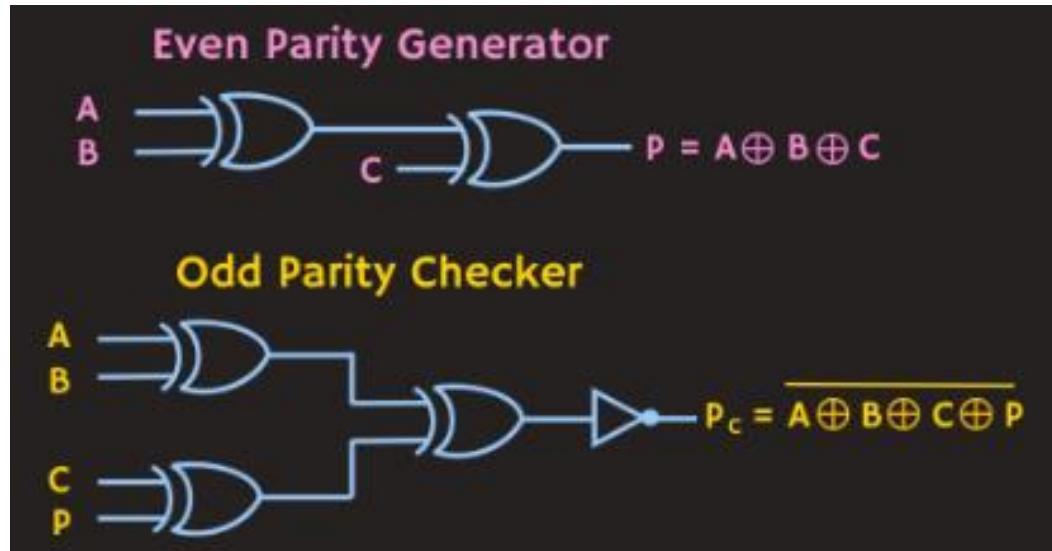
- No memorization នៅពីភាពតាំង ex. Decoder
- Output instant in time

Sequential logic circuit

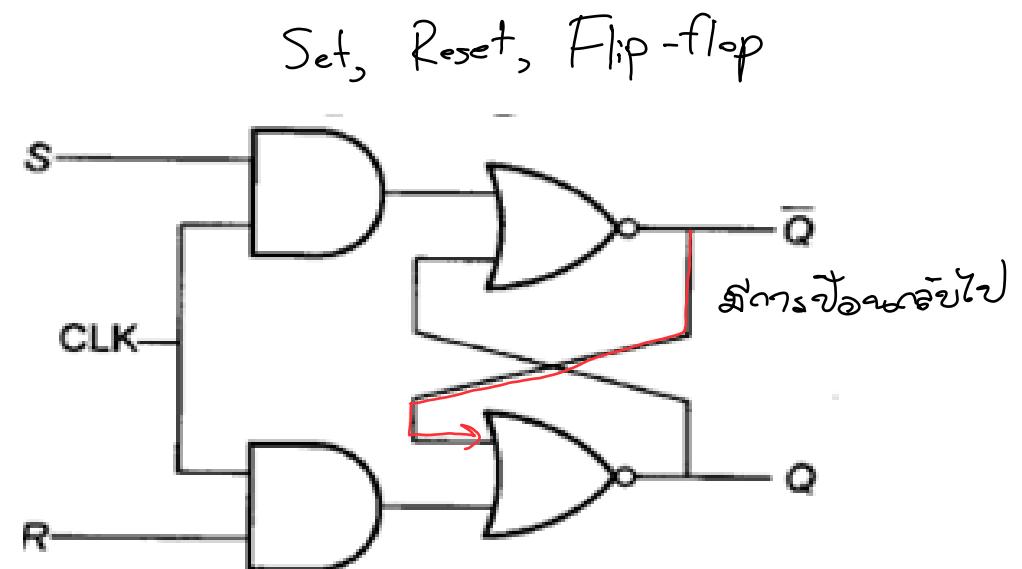


- Memorization ex. Counter (ចុចូល)
- Output depends on a previous state
- Use a clock signal to control the work

Combinational logic circuit



Sequential logic circuit

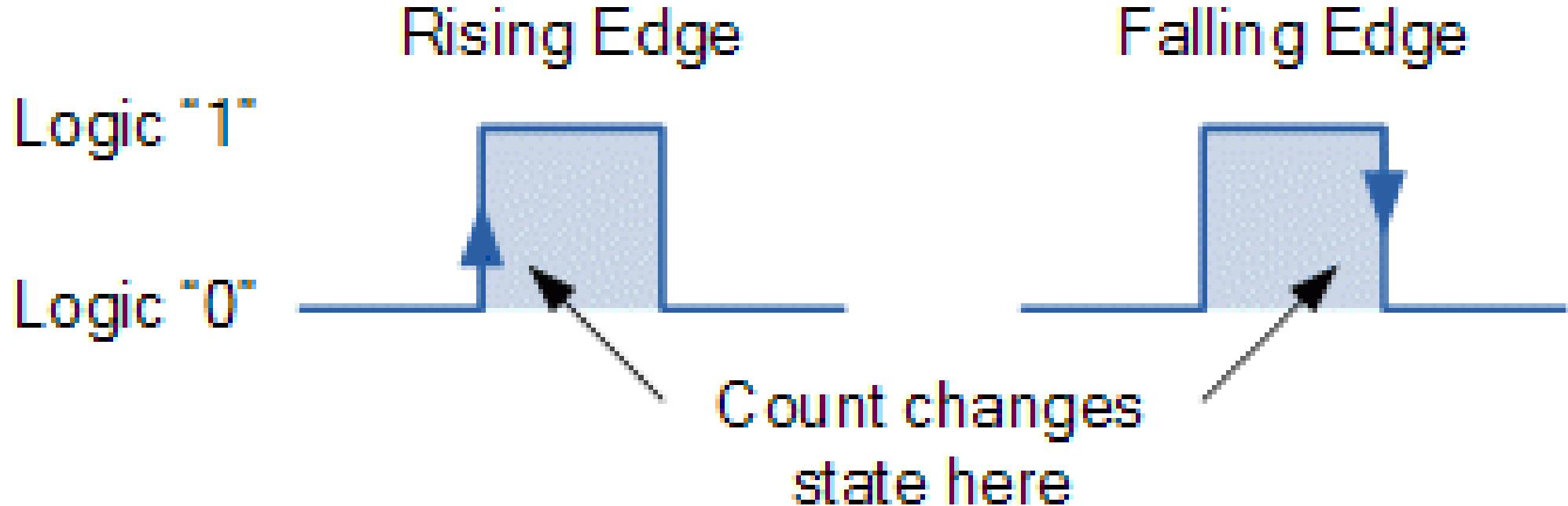


- วงจรฟีดแบค feedback

RISING AND FALLING EDGE TRIGGER

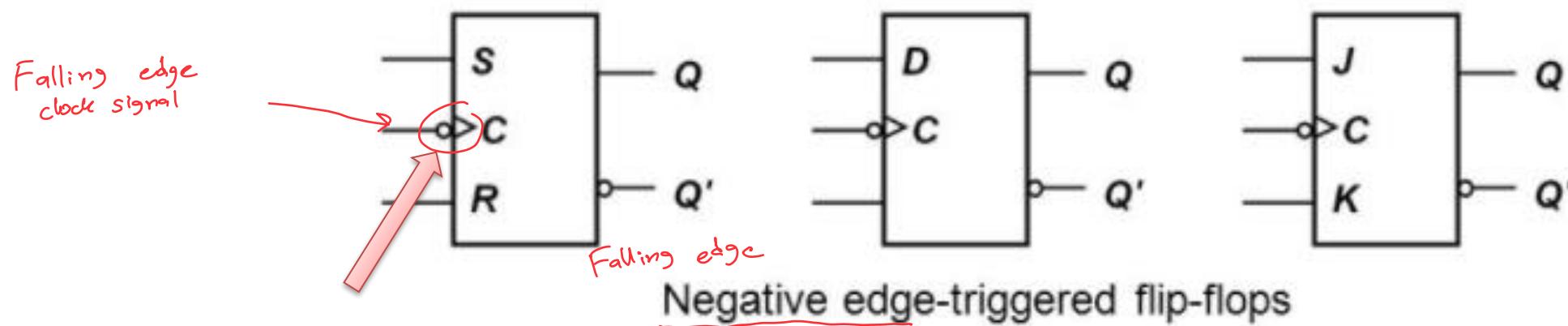
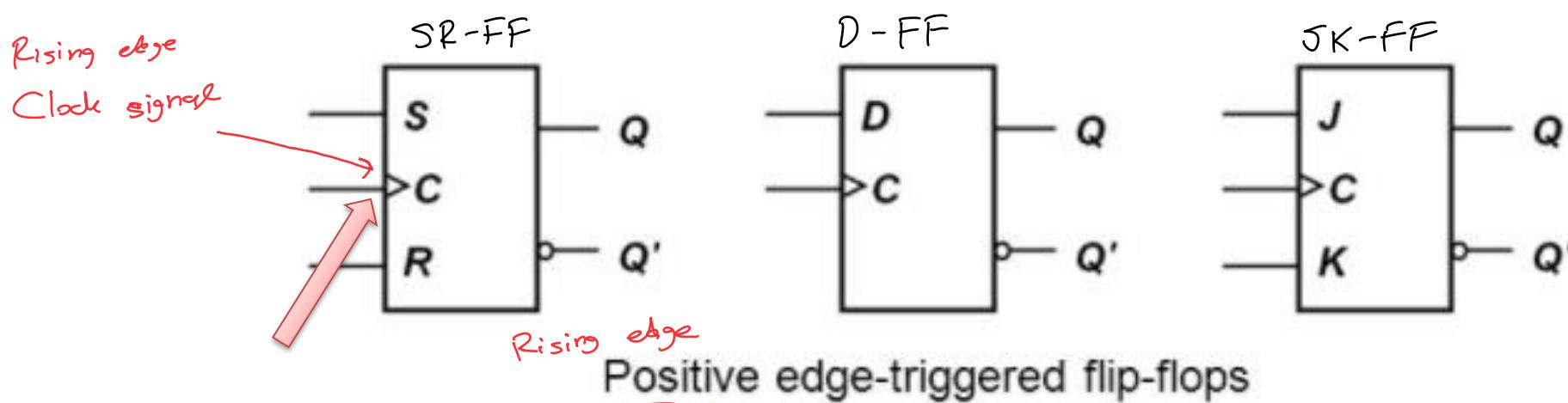
To understand the clock trigger in the digital ICs between rising and falling edge.

Rising/Falling edge trigger



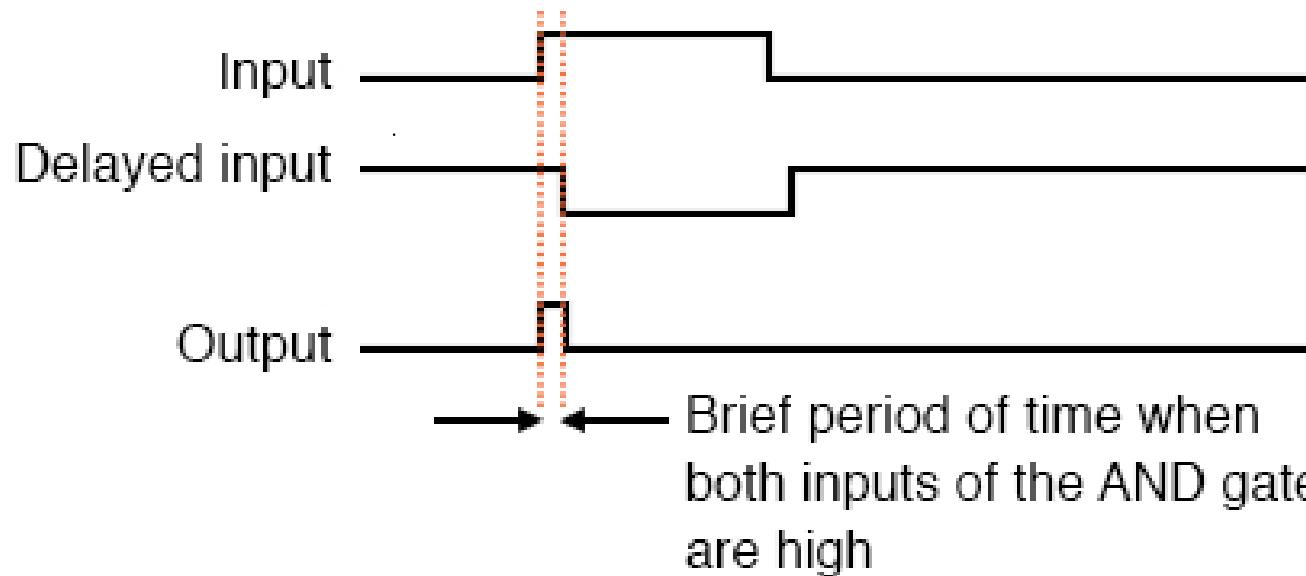
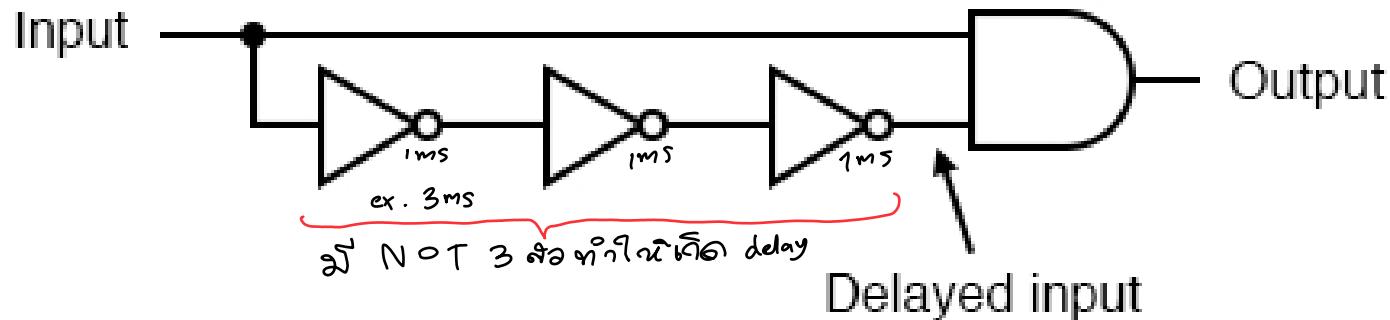
Logic ឧបតម្រូវការការពារនៃសម្រាប់ការ
(ការការពារការពារ)

Flip-flop symbols in rising/falling edge trigger



Some textbook for rising/falling edge trigger called positive/negative edge trigger

Circuit detects positive edge trigger



Rising and Falling edge detection

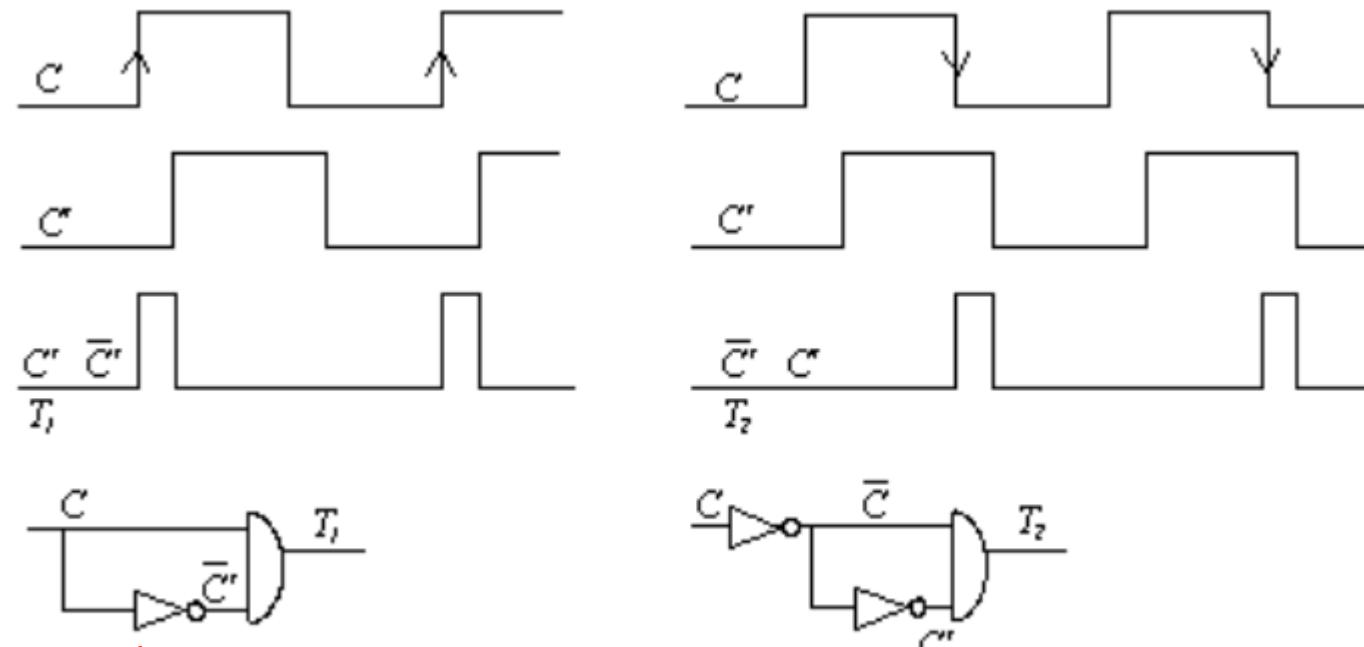
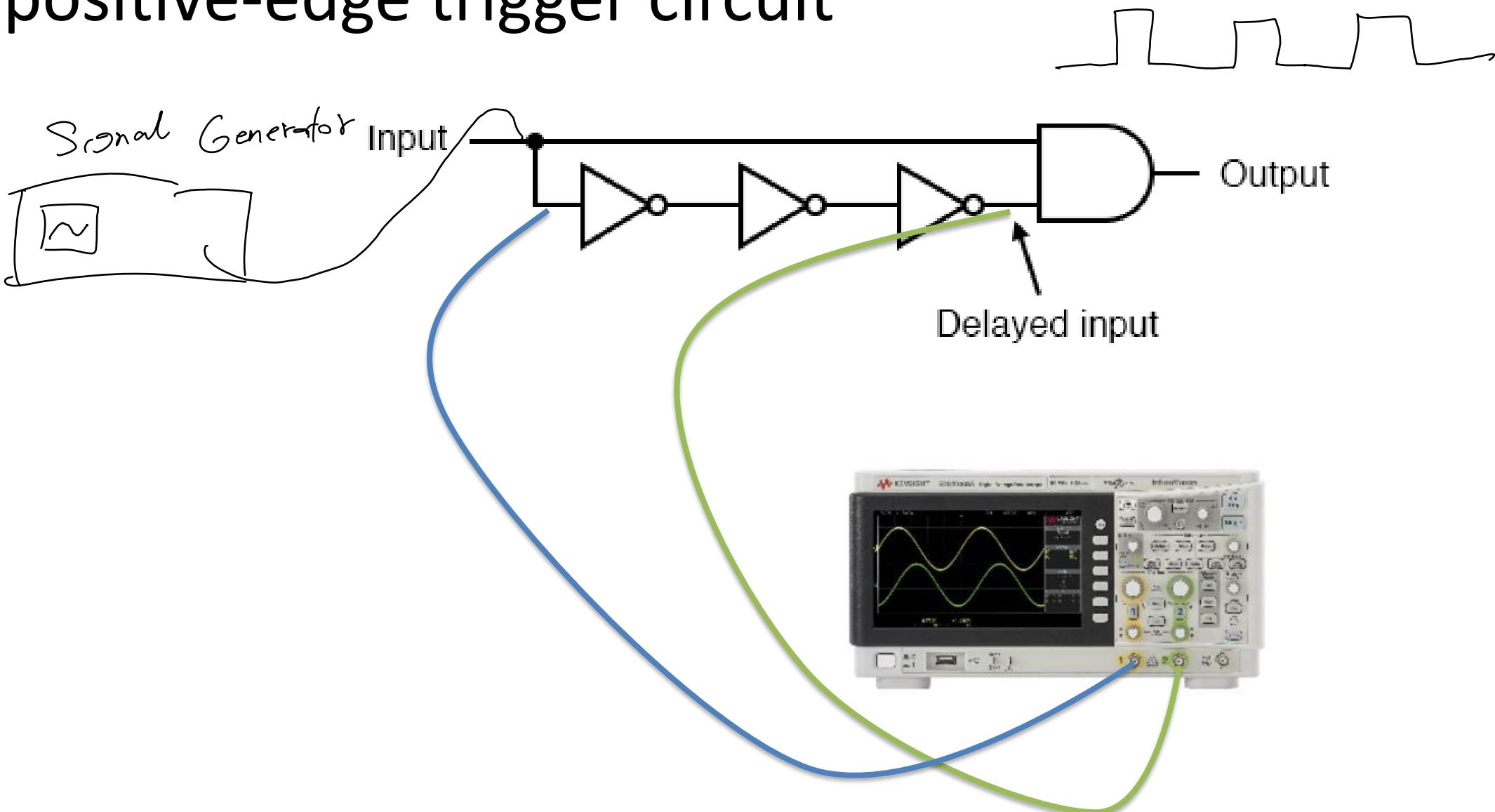


Figure 1. Edge detection circuits.

ఈ నోట లేదా
తాగిని నోట కి గొంతుగా గొప్ప

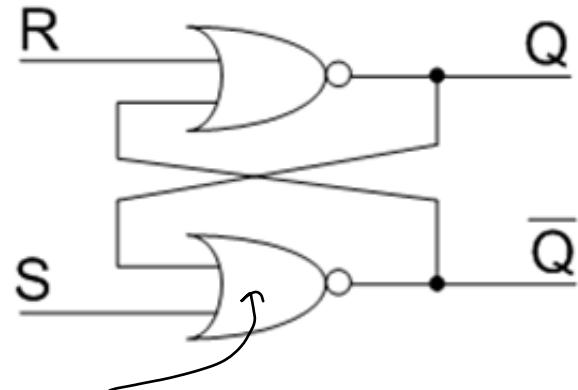
Activity 4.1 Delay time measurement in the positive-edge trigger circuit



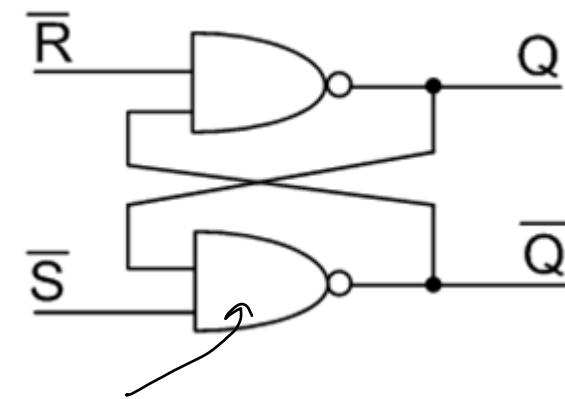
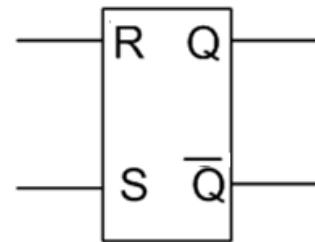
SR FLIP-FLOP

Set-Reset Flip-flop (SR-flipflop)

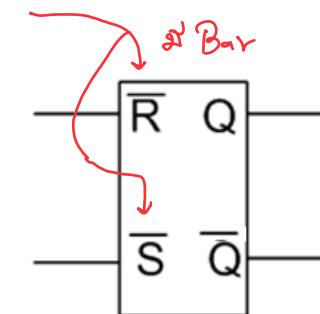
SR flipflop is two types by the structure of logic gate.



NOR gate SR-flipflop

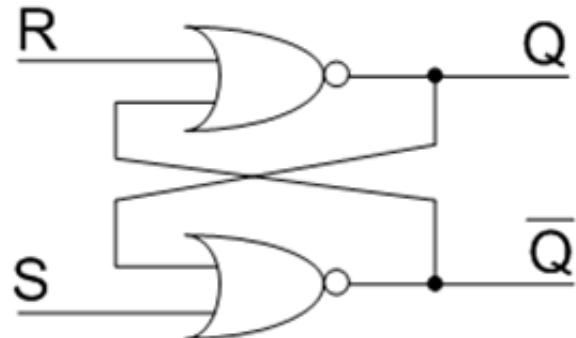


NAND gate SR-flipflop

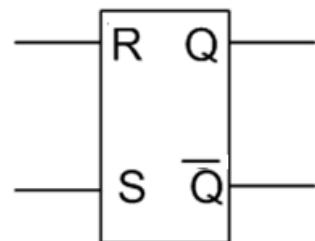


Set-Reset Flip-flop (SR-flipflop)

Truth table



NOR gate SR-flipflop



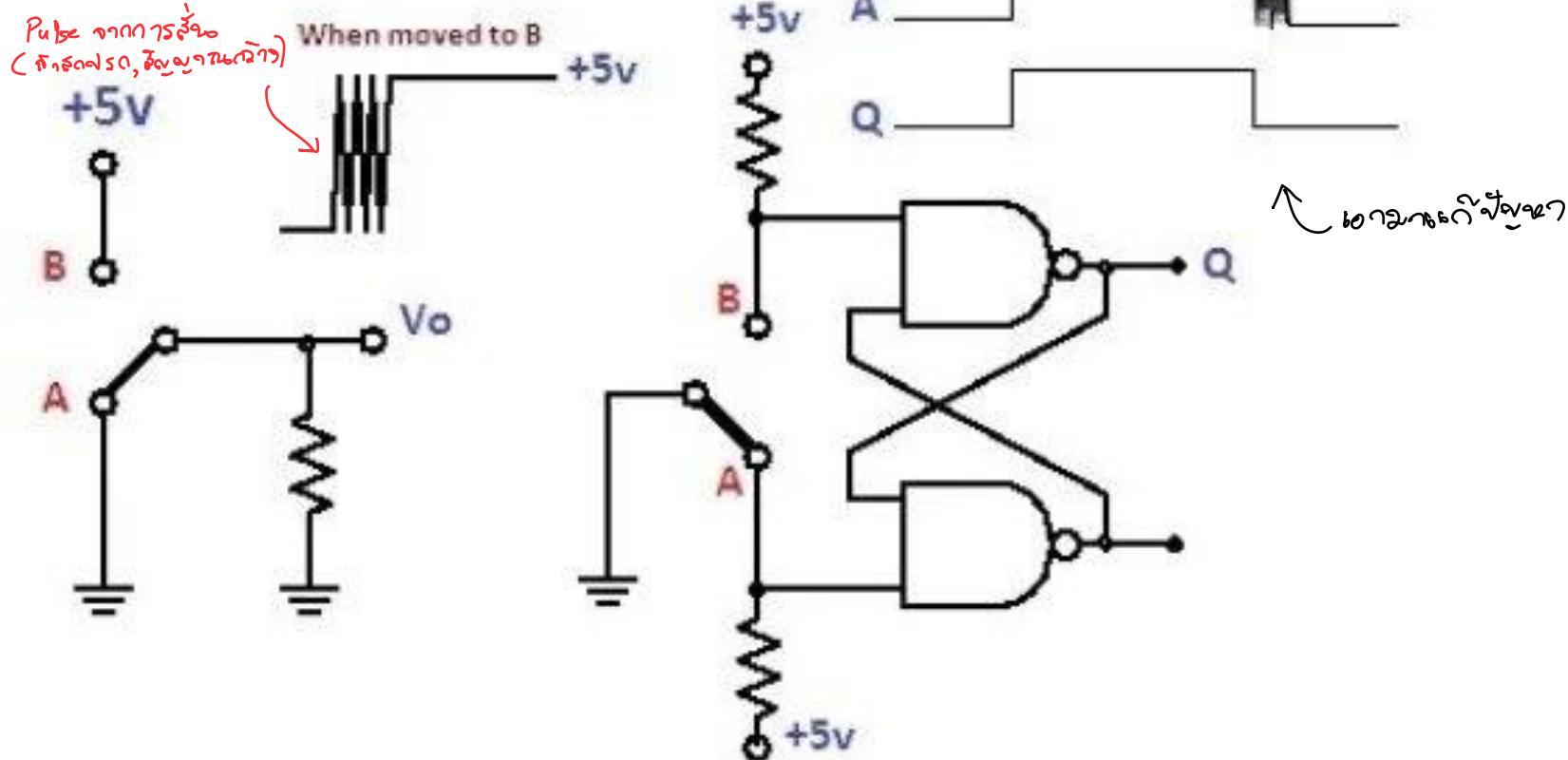
S	R	Q
0	0	No change \rightarrow state 保持
0	1	1 = Set \leftarrow 1 ასაკანი
1	0	0 = Reset \leftarrow 0 ასაკანი
1	1	Restrict Combination

S	R	\xrightarrow{Q}	Q	S	R	\xrightarrow{Q}	არა შეძლება
0	1	\rightarrow	1	0	0	\rightarrow	
0	0	\rightarrow	1				
				1	0	\rightarrow	0
				0	0	\rightarrow	0

Example application uses SR-flipflop

- Debounced switch

www.electroSome.com

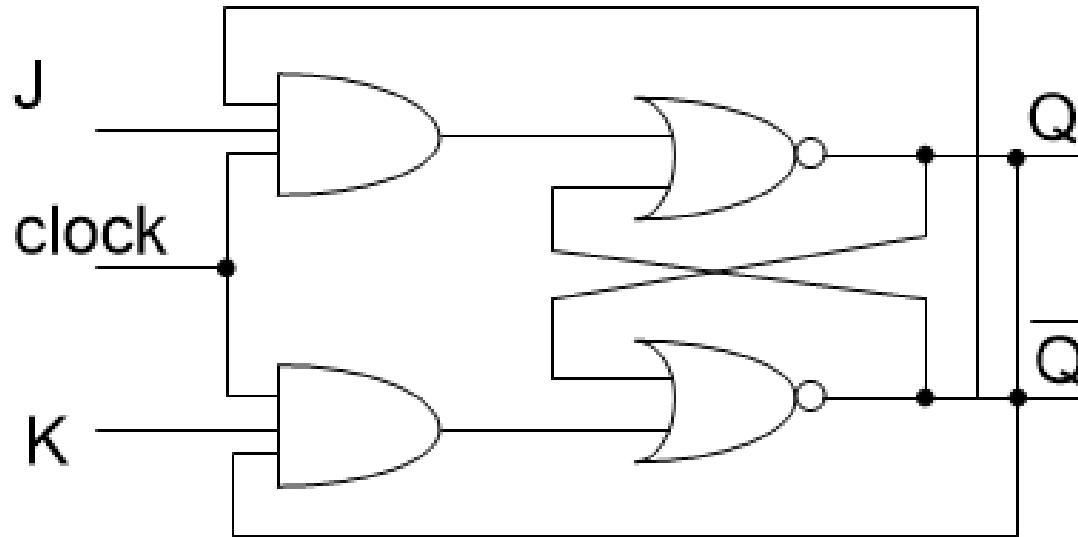


JK FLIP-FLOP

To understand a trouth table of JK flip-flop and known difference between JK and RS flip-flop.

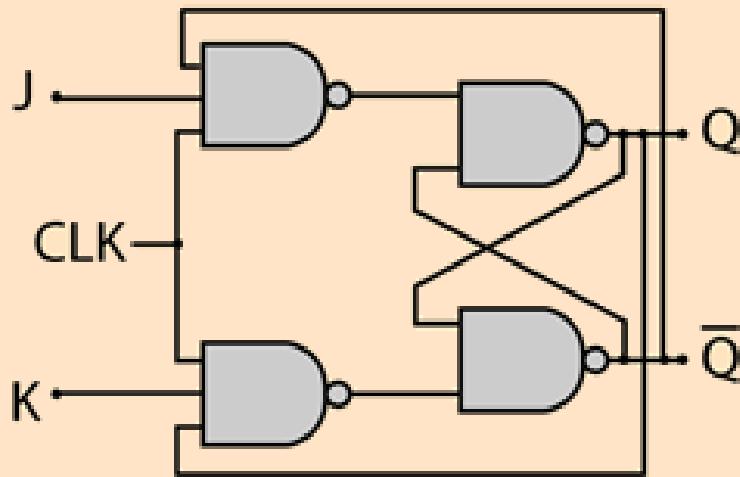
JK Flip-flop

SR-FF ໄຟລ່ຈົນຂະດາວທີ່ງໆ

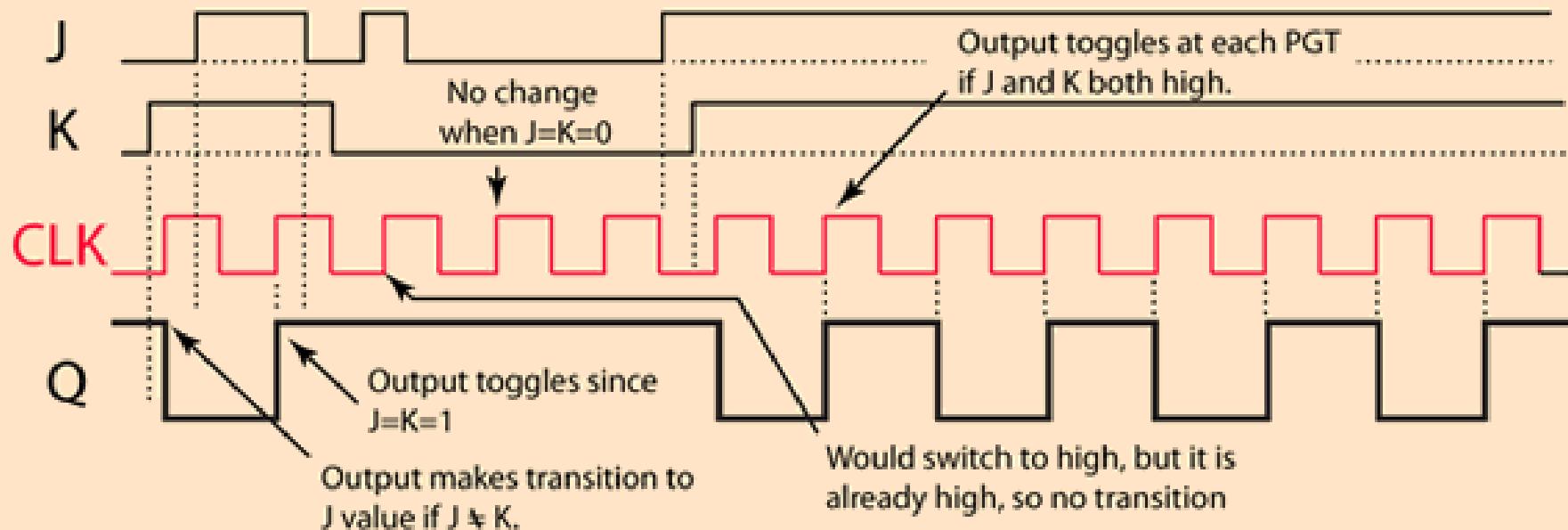


- Invented by Jack Kilby
- The JK flip-flop modified from SR flip-flop by adding a clock input to prevent the invalid output condition that occurs when both S and R are equal to logic “1”.

Switching Example: J-K Flip-Flop



The positive going transition (PGT) of the clock enables the switching of the output Q . The "enable" condition does not persist through the entire positive phase of the clock. The J & K inputs alone cannot cause a transition, but their values at the time of the PGT determine the output according to the [truth table](#). This is an application of the versatile [J-K flip-flop](#).



JK Flip-flop Truth table

Input 3 ตัว

จุดประกาย Logic ≈ 15

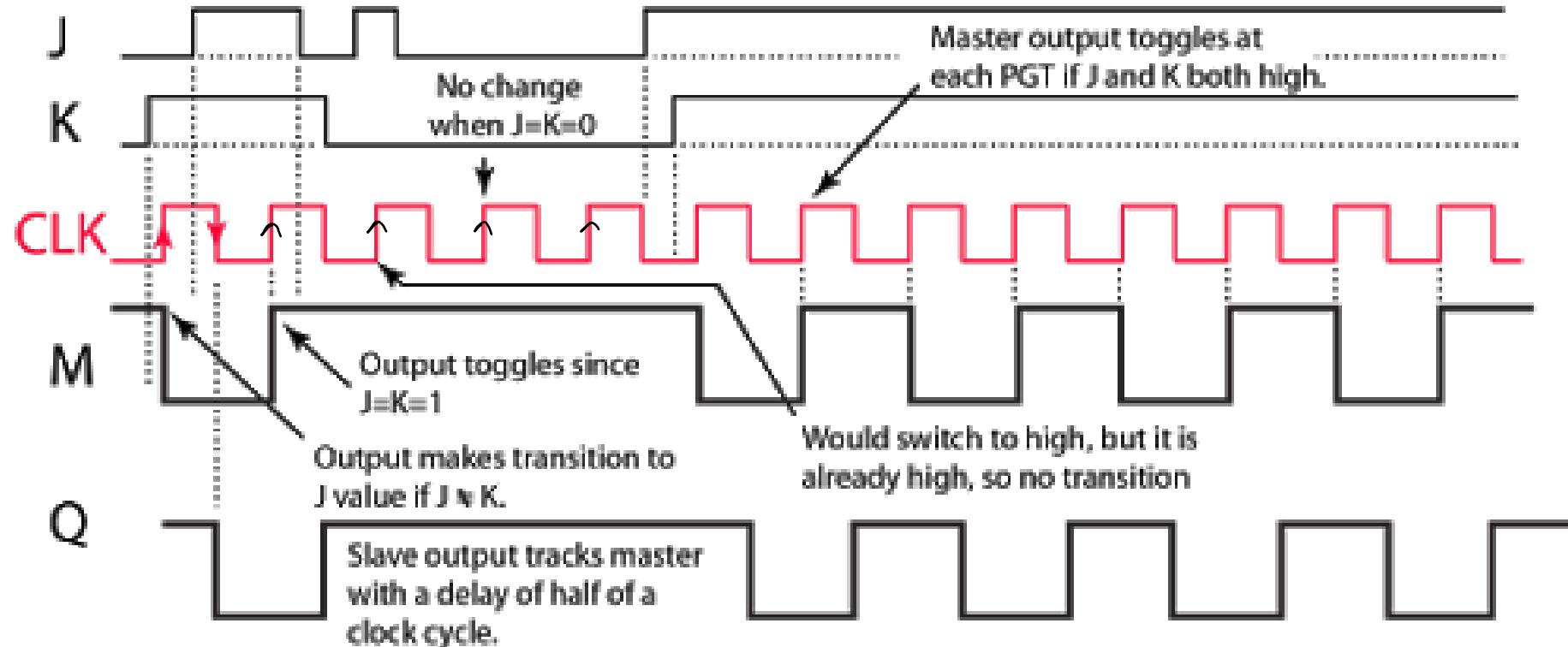
Clk	J	K	Q	Description
No clock	?	?	?	No change
	0	0	?	No change
	0	1	?->0	Reset
	1	0	?->1	Set
	1	1	0->1 1->0	Toggle ; ลับปุ่ม

ระยะเวลา clock/2

JK flip-flop in timing states

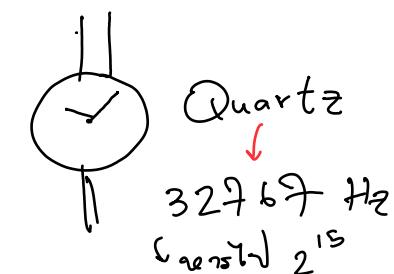
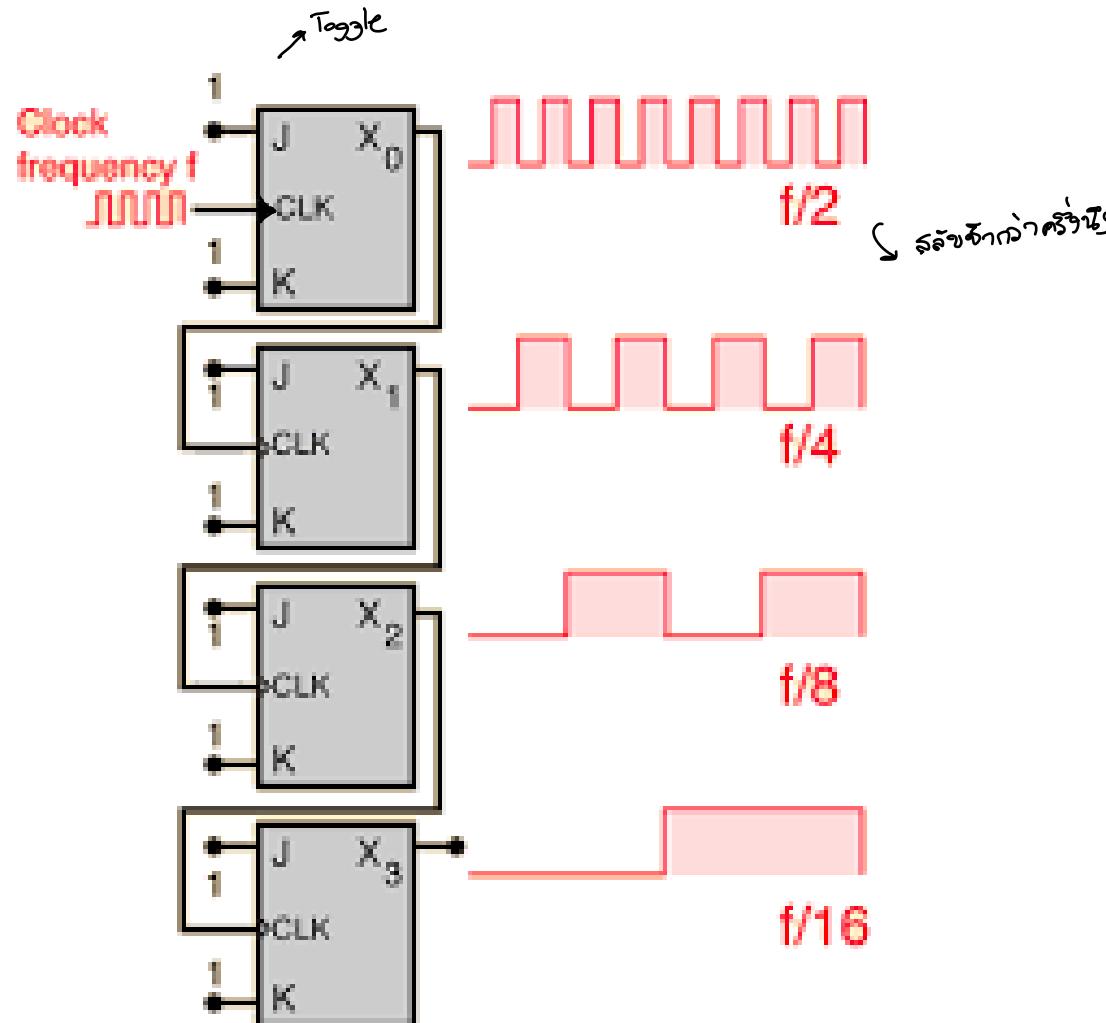
Timing Diagram

Clock កំណត់ទិន្នន័យ



Application used JK flip-flop

ඉංජිනේරුව්

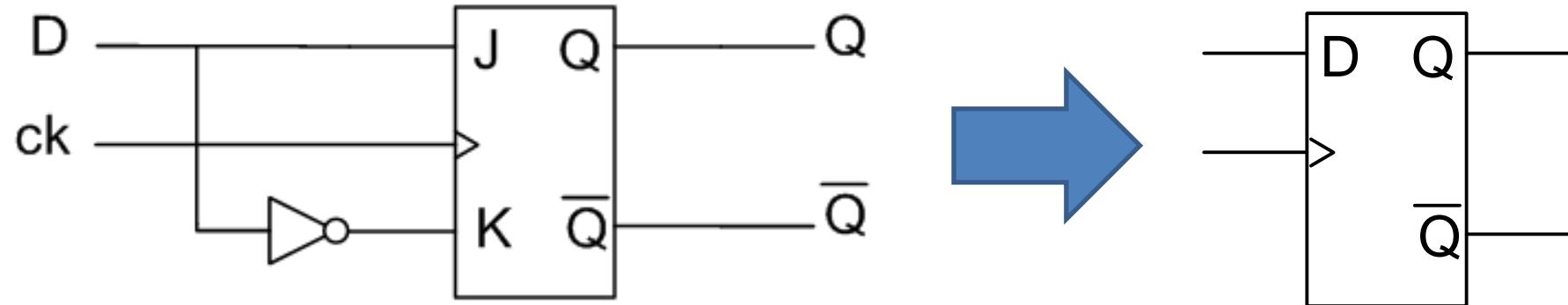


D FLIP-FLOP AND T FLIP-FLOP

↳ ආගැනුවල නිර්මාණය කළ යුතු සෑවනා

JK
↳ ප්‍රාග්‍රැම්මා
↳ මූල්‍ය තෝගලේ මෙහෙයුම් (ඉග්‍රැස් සෑවනා නිර්මාණය කළ යුතු binary)

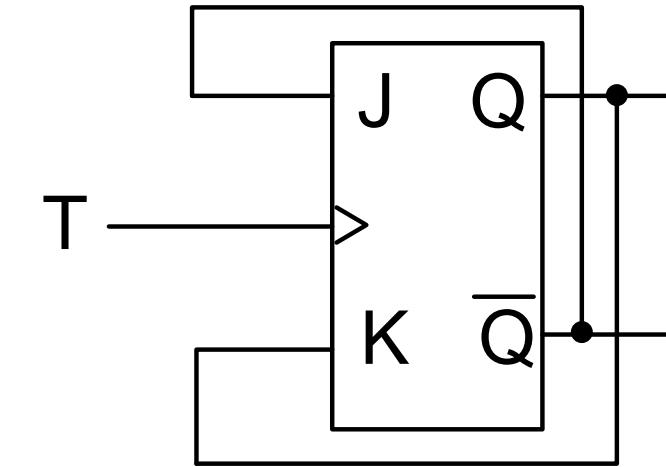
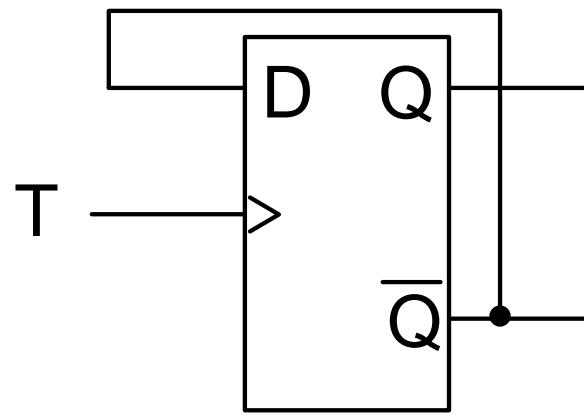
Making D flip-flop from JK



Clk	J	K	Q	Description
No clock	?	?	?	No change
	0	1	?->0	Store "0"
	1	0	?->1	Store "1"

T Flip-flop from D and JK

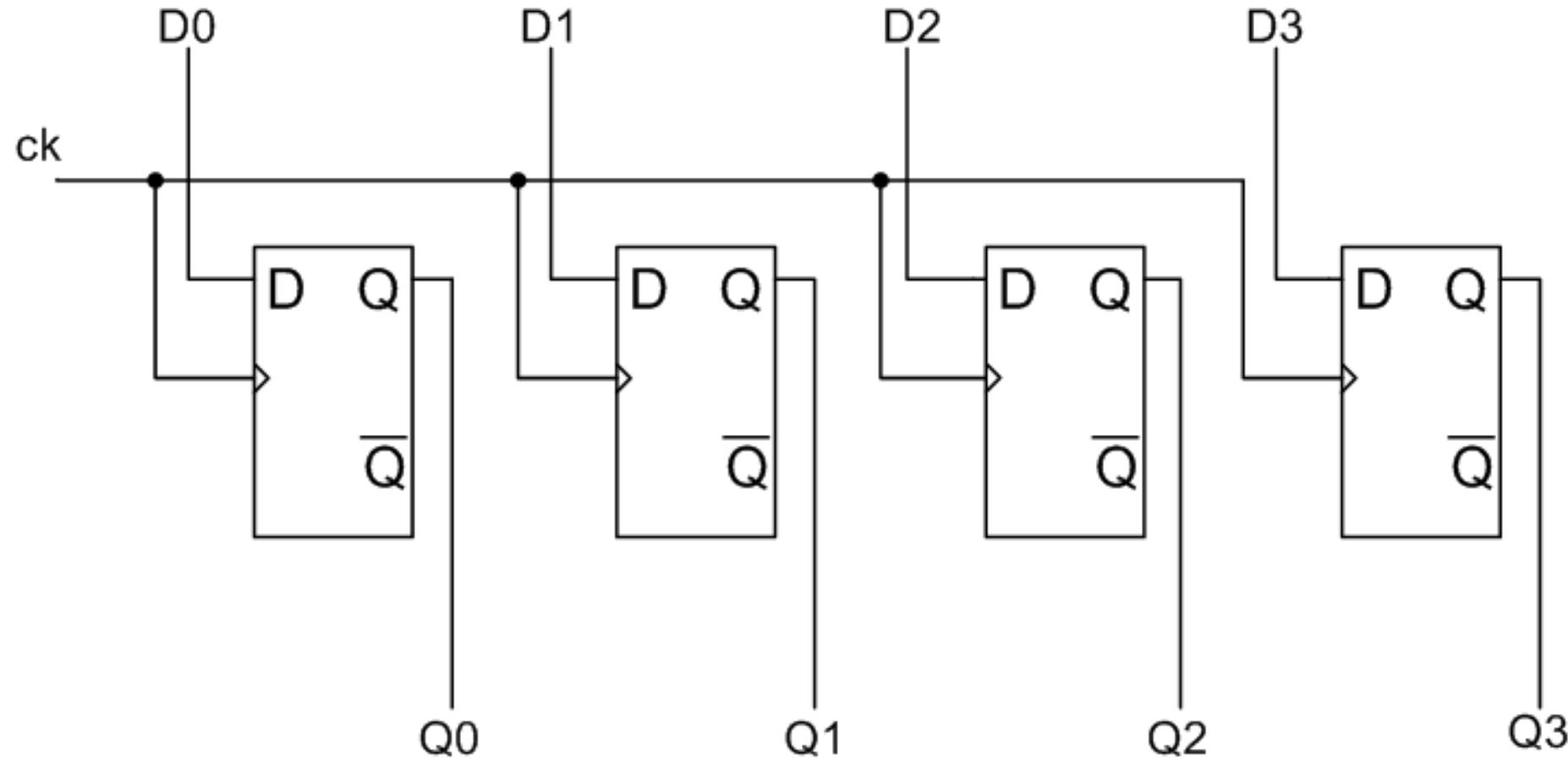
↳ ගුණාක්‍රම තෝගල
ex. උවස වෙත මෙහෙයුම්



Clk (T)	Q	Description
No clock	?	No change
	?->0 ?->1	Toggle

4-BIT LATCH CIRCUIT

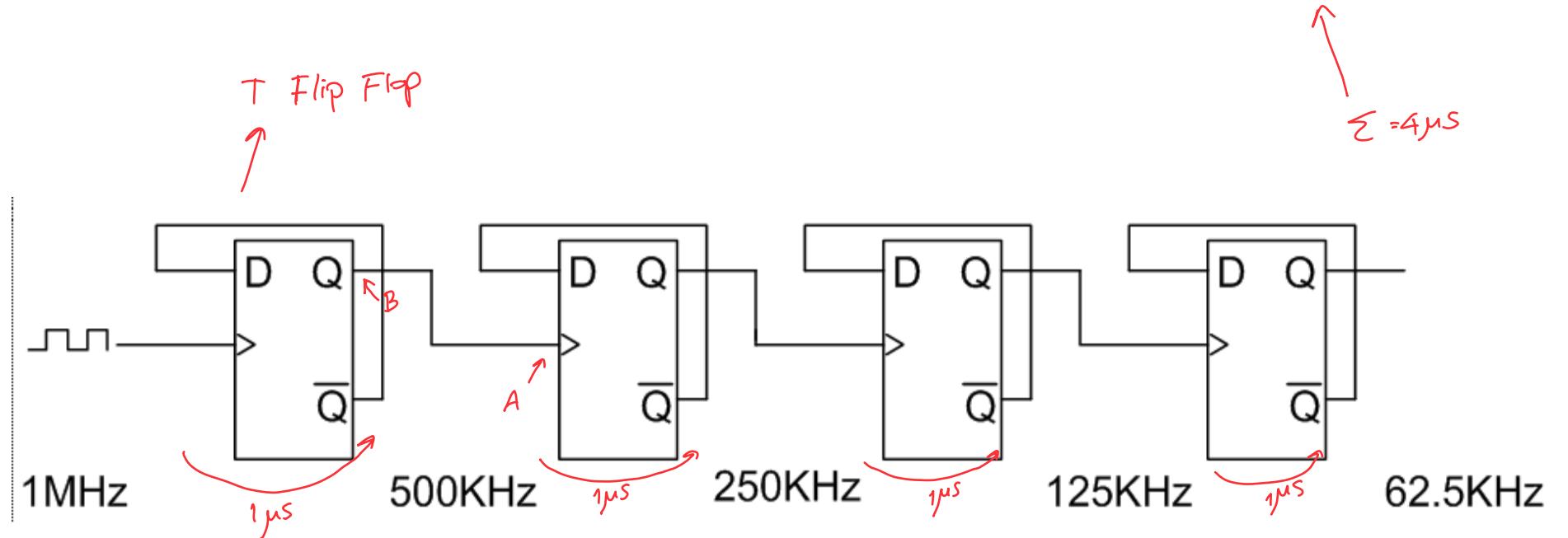
4-bit Latch circuit



FREQUENCY DIVISION CIRCUIT

Frequency division circuit

ចំណាំ: កិច្ចការណីតសេវា



ទី 4 នៃ 4 នឹងបានរាយការណ៍

First in, First out, බ්‍රිංග්‍රැම මෙහෙතුම්

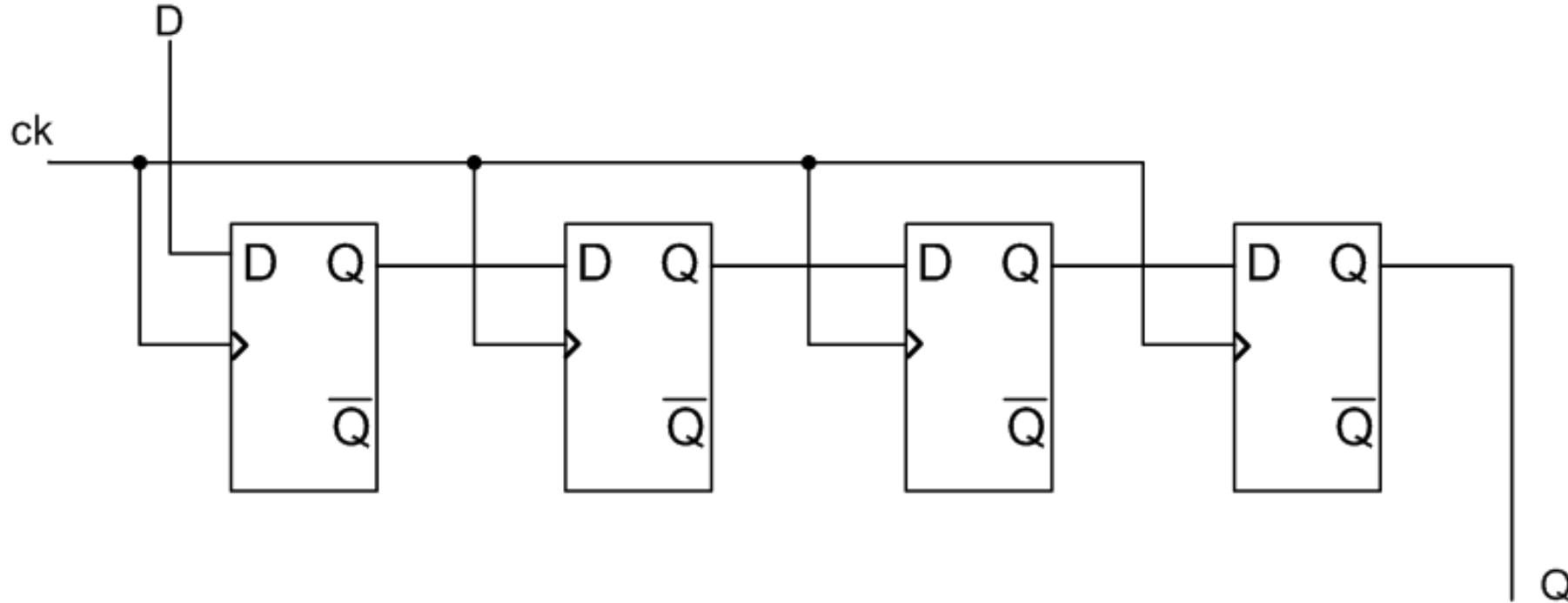


4-BIT FIFO CIRCUIT

4-bit First-in First-out (FIFO)

memory over serial

t_3
1011
 t_5
1111



COUNTER

Counter circuit

- A counter circuit is a binary counting circuit.
- The counter circuit has two kinds:
 - Asynchronous counter circuit, known as “a ripple counter”
 - Flip-flops are not clocked simultaneously.
 - Propagation delay
 - Synchronous counter circuit
 - Flip-flops are triggered simultaneously by the same clock signal.
 - No propagation delay.

* លោកស្រីនឹងប្រាប់ពីរដូចជា

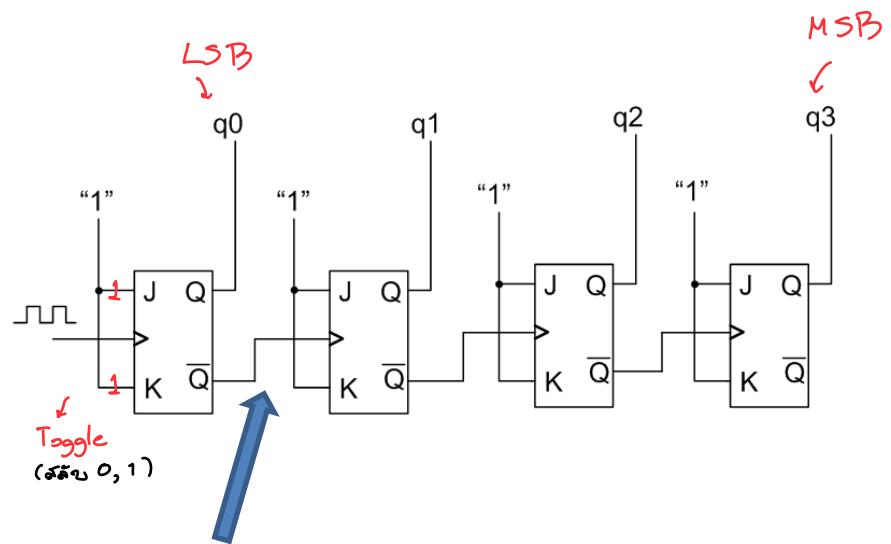
Hardware ទុក
ប្រព័ន្ធដែលបានគេហទំនាក់ទំនង ↑
IOT ↑

Asynchronous
counter circuit

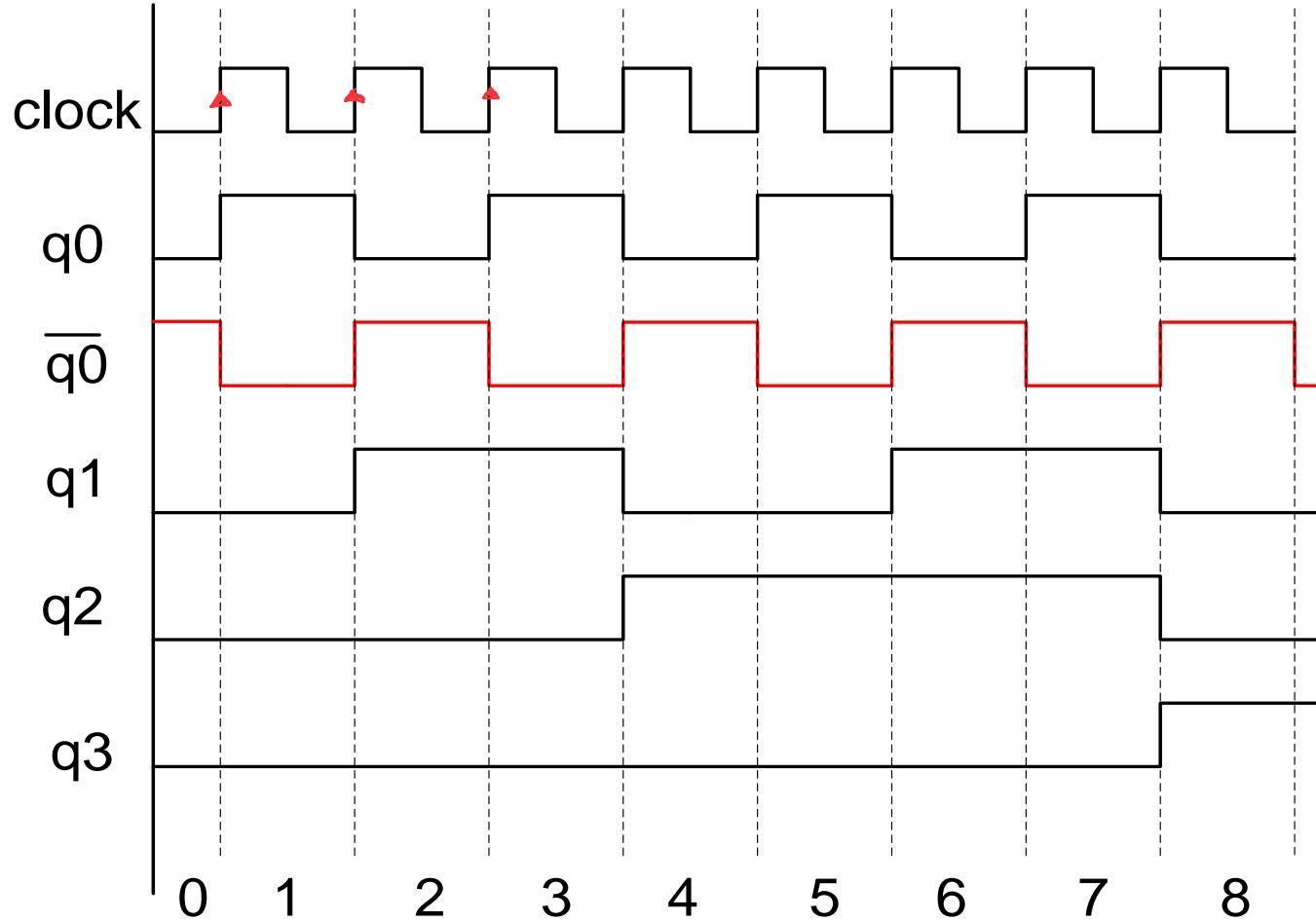
Synchronous
counter circuit

~~Exam~~

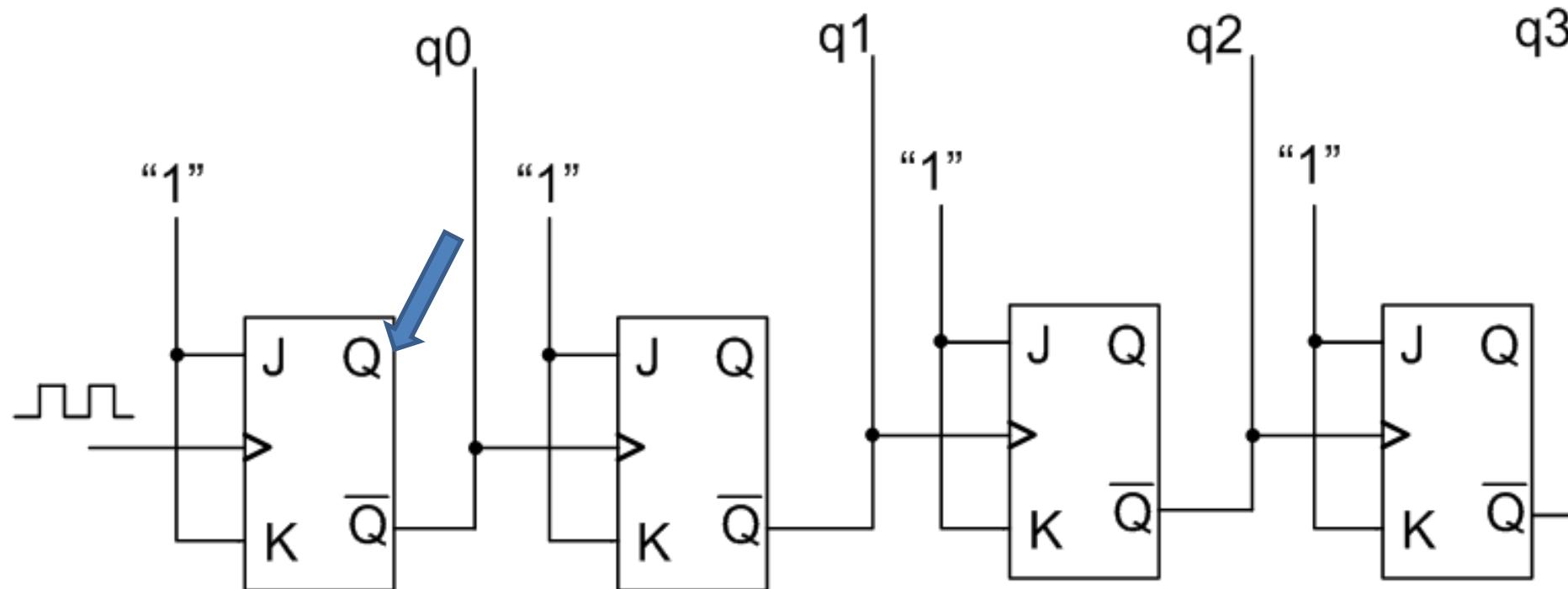
Asynchronous counter circuit



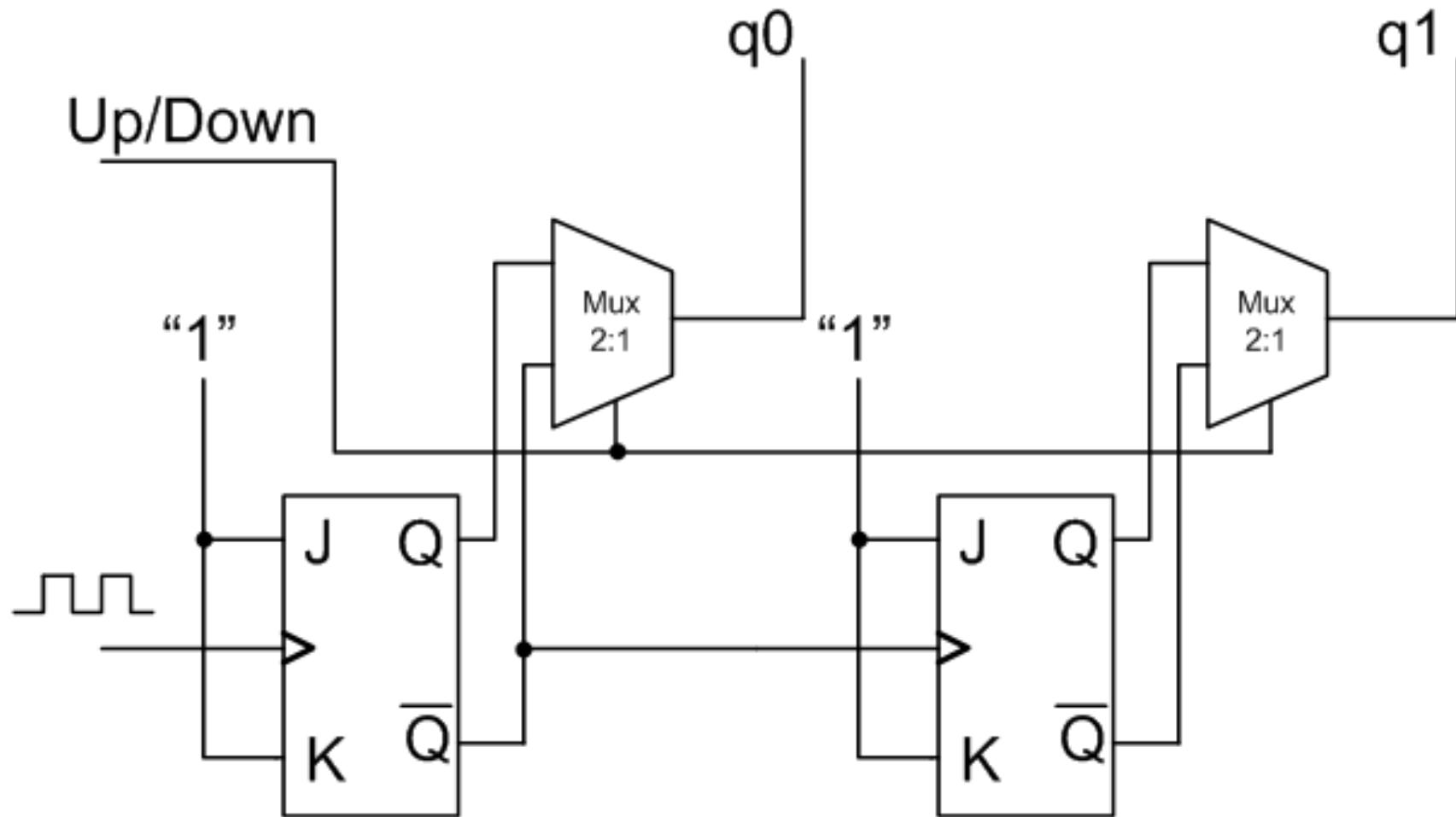
மீ எலோ தீவிளை பூப்பான்
ms/ns



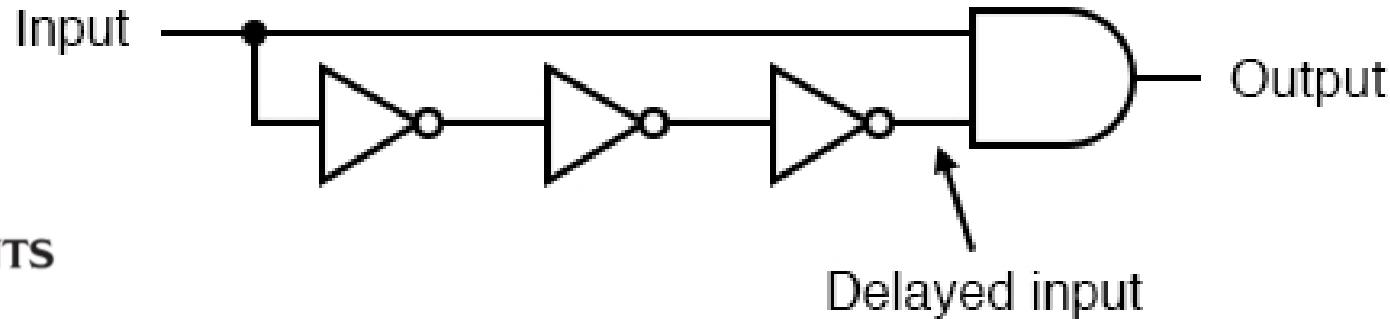
Count down



2-bit Asynchronous count up/down circuit



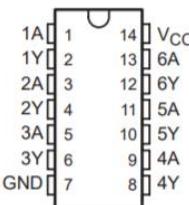
Delay-time problem in asynchronous counter circuit



**SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS**

SDLS029C – DECEMBER 1983 – REVISED JANUARY 2004

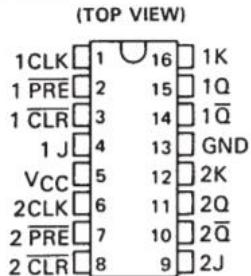
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S04 SN74S04			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	$R_L = 280 \Omega$, $C_L = 15 \text{ pF}$	3	4.5		ns
t_{PHL}				3	5		

Asynchronous counter issue



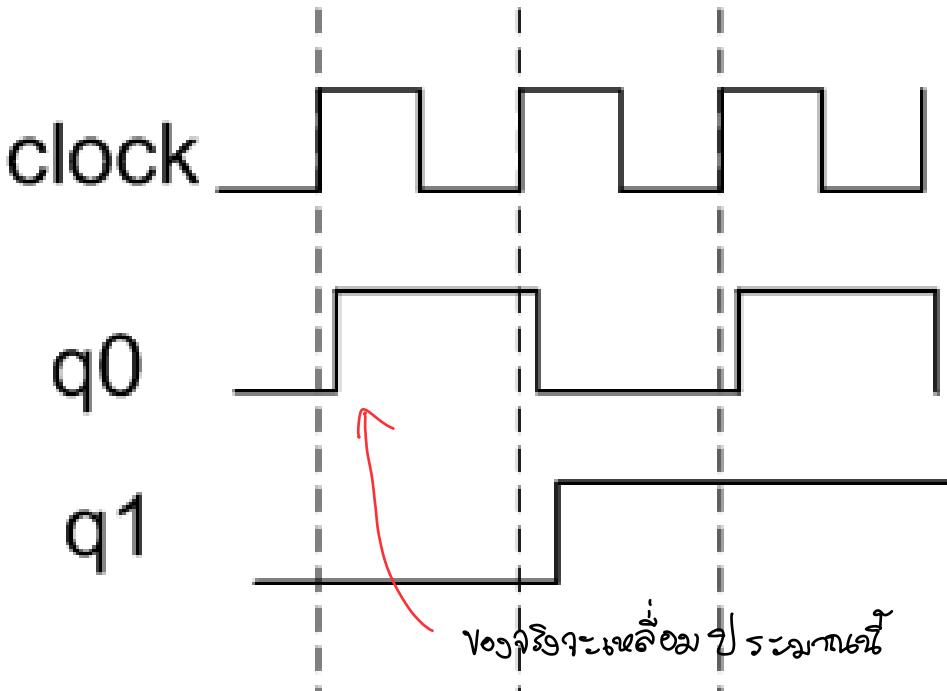
'76
FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	J K	Q	\bar{Q}
L	H	X	X X	H	L
H	L	X	X X	L	H
L	L	X	X X	H [†]	H [†]
H	H	⊟	L L	Q ₀	\bar{Q}_0
H	H	⊟	H L	H	L
H	H	⊟	L H	L	H
H	H	⊟	H H	TOGGLE	

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

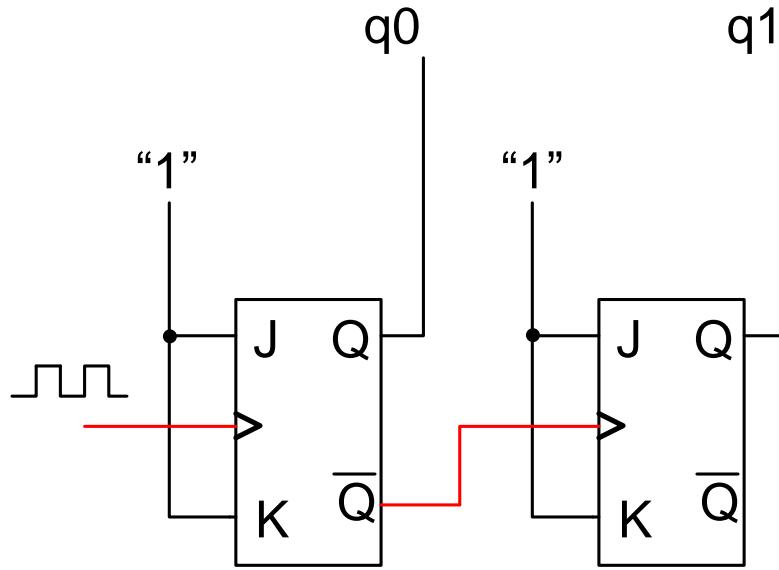
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			UNIT
			MIN	TYP	MAX	
f_{max}			30	45		MHz
	t_{PLH}	PRE, CLR or CLK	15	20		ns
			15	20		ns

Time Propagation
from Low to High

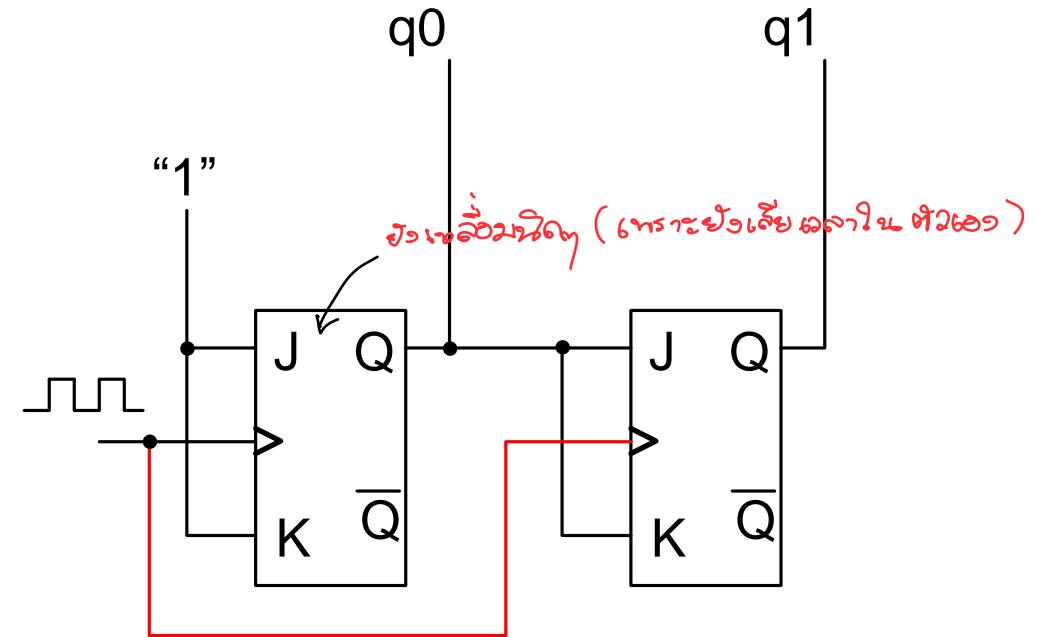


เมื่อ device ต่อตัว
เวลาจะ detect ไม่ได้

Asynchronous vs Synchronous counter

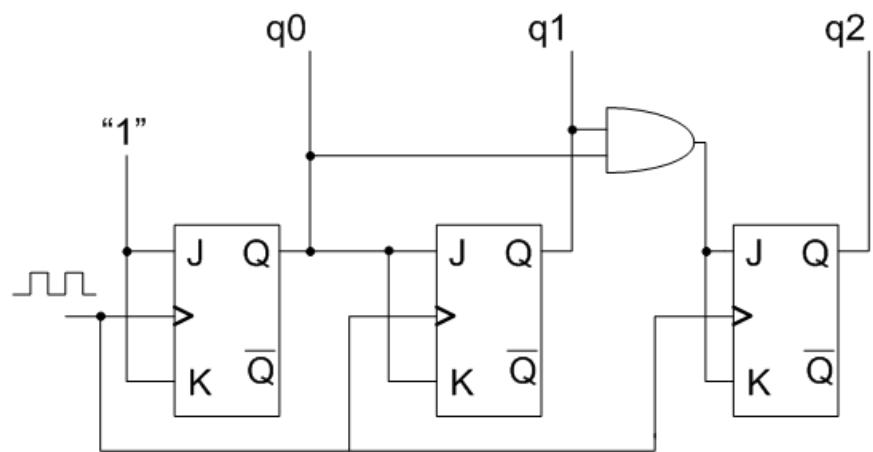


- Clock or control signal getting from previous states
- Easy design the counter circuit.
- Not suitable for a **critical time** system.
- **Radiotherapy, MRI, Microwave**
→ **Medical Equipment** (Engineering)



- A clock signal controls all states
- Complexity for design counter circuit.
- Proper for the critical time system

Example 3-bit synchronous counter-up



?

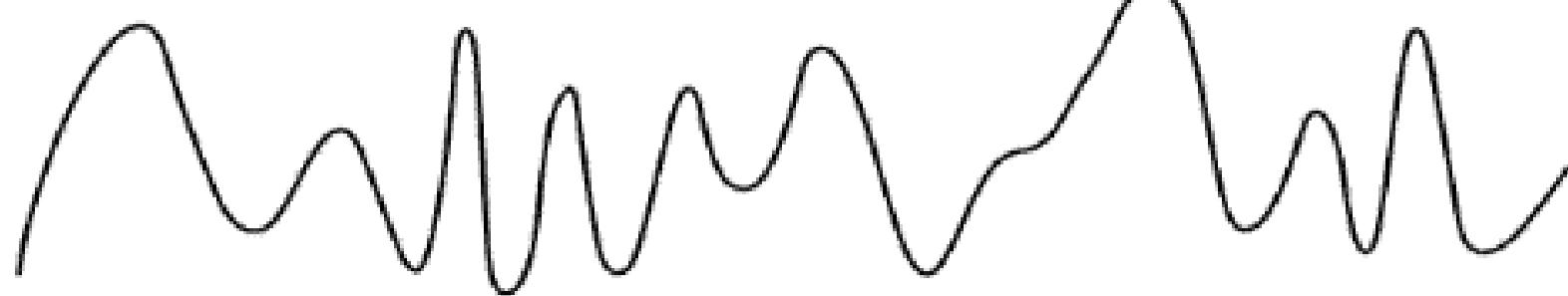
ลำดับ ck	Q2	Q1	Q0	อธิบาย
1	0	0	0	นับ 0
2	0	0	1	นับ 1
3	0	1	0	นับ 2
4	0	1	1	นับ 3 เนื่องจาก q0 and q1 = 1
5	1	0	0	นับ 4 เกิด toggle ที่ q2
6	1	0	1	นับ 5
7	1	1	0	นับ 6
8	1	1	1	นับ 7 เนื่องจาก q0 and q1 = 1
9	0	0	0	นับ 0 เกิด toggle ที่ q2

ANALOG SIGNAL AND DIGITAL SIGNAL

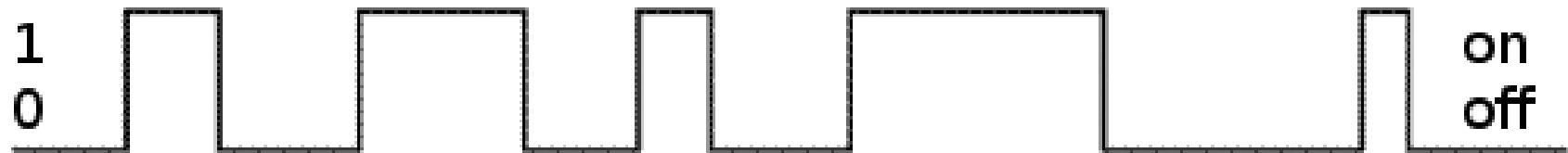
Analog signal vs Digital signal

Analog Signal

ពន្លឹងបញ្ចប់
continuous



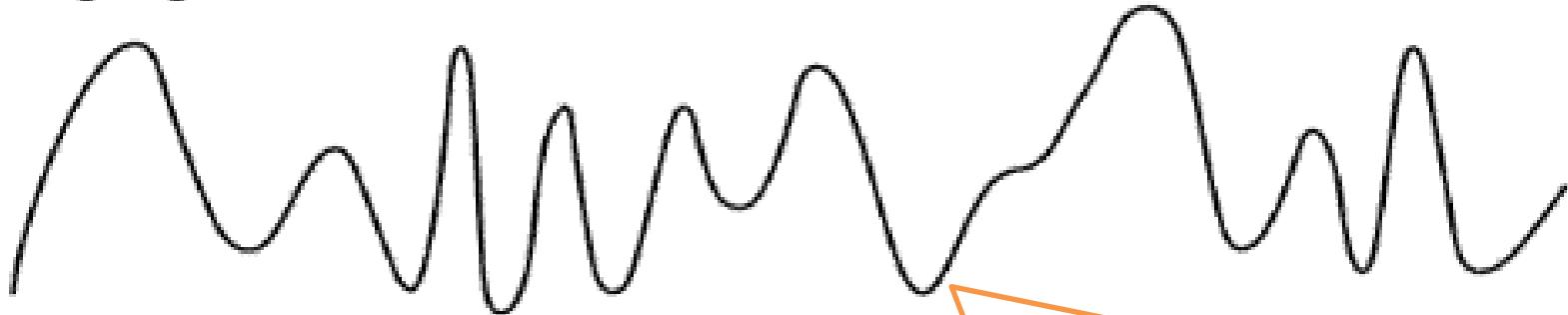
Digital Signal



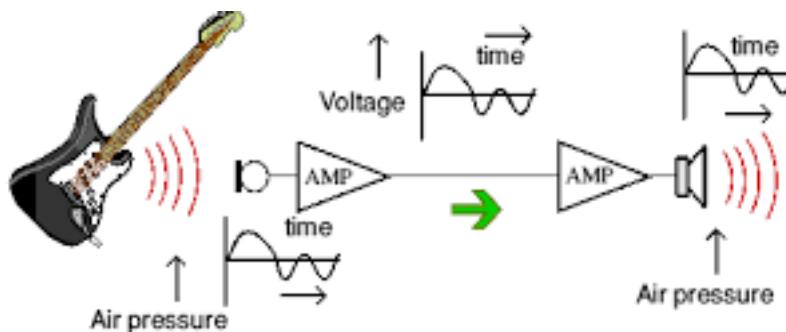
ក្រឡើងបញ្ចប់
discrete

Analog signal vs Digital signal

Analog Signal

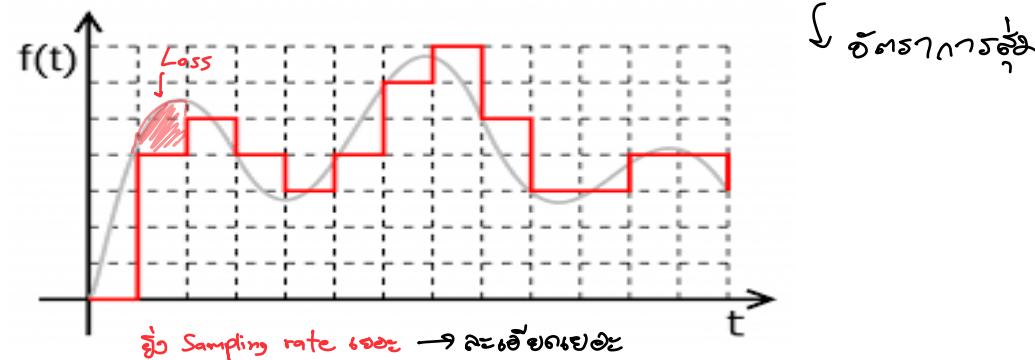


Analog signals are continuous-time signals changing the wave from continuously.

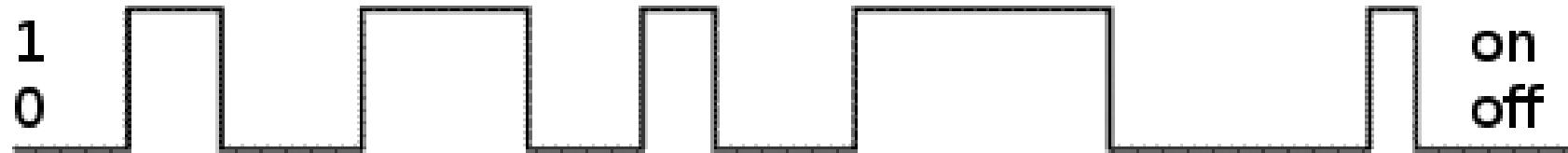


Ana

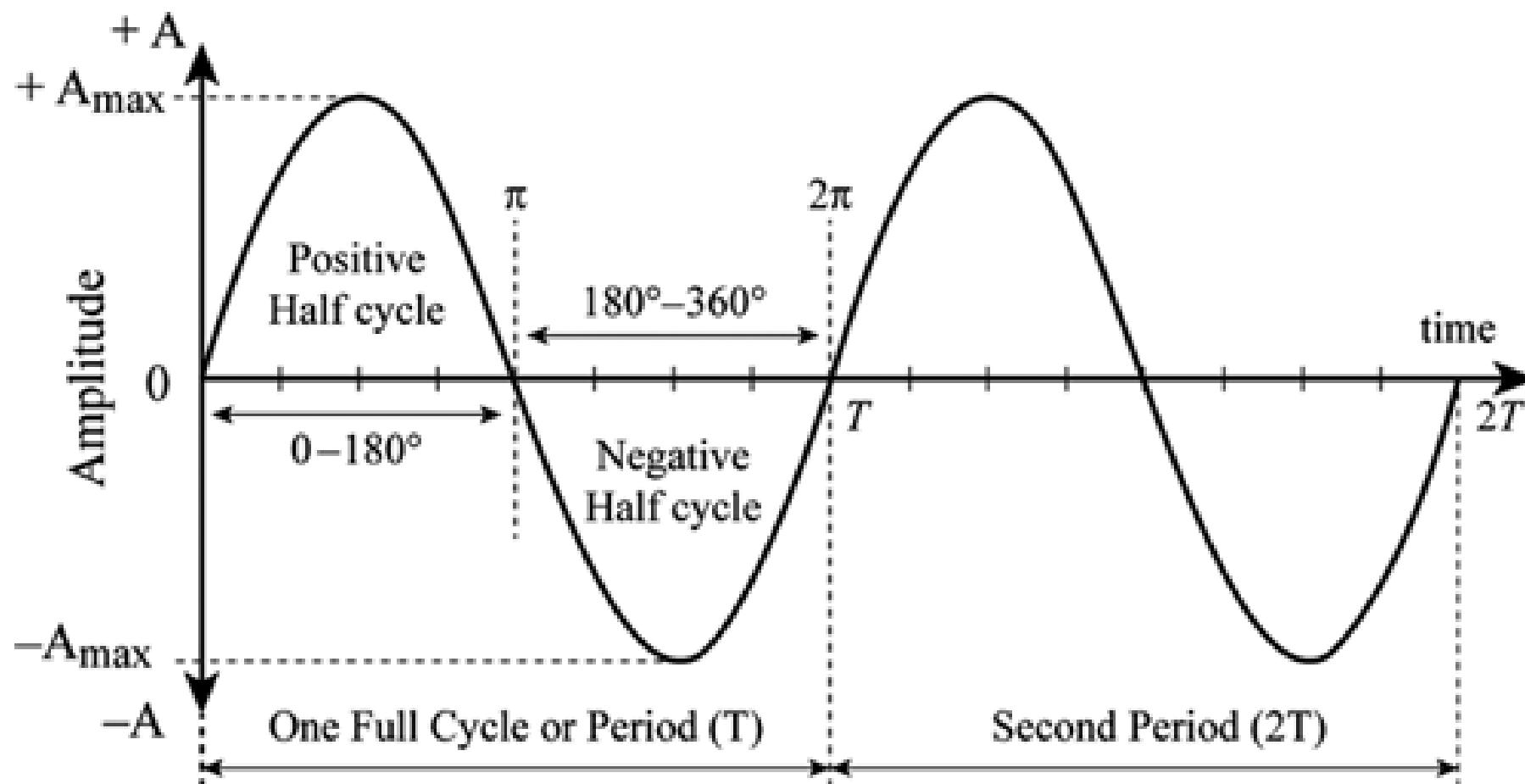
Digital signals are discrete-time signals limited by number of bits and the **sampling rate**.



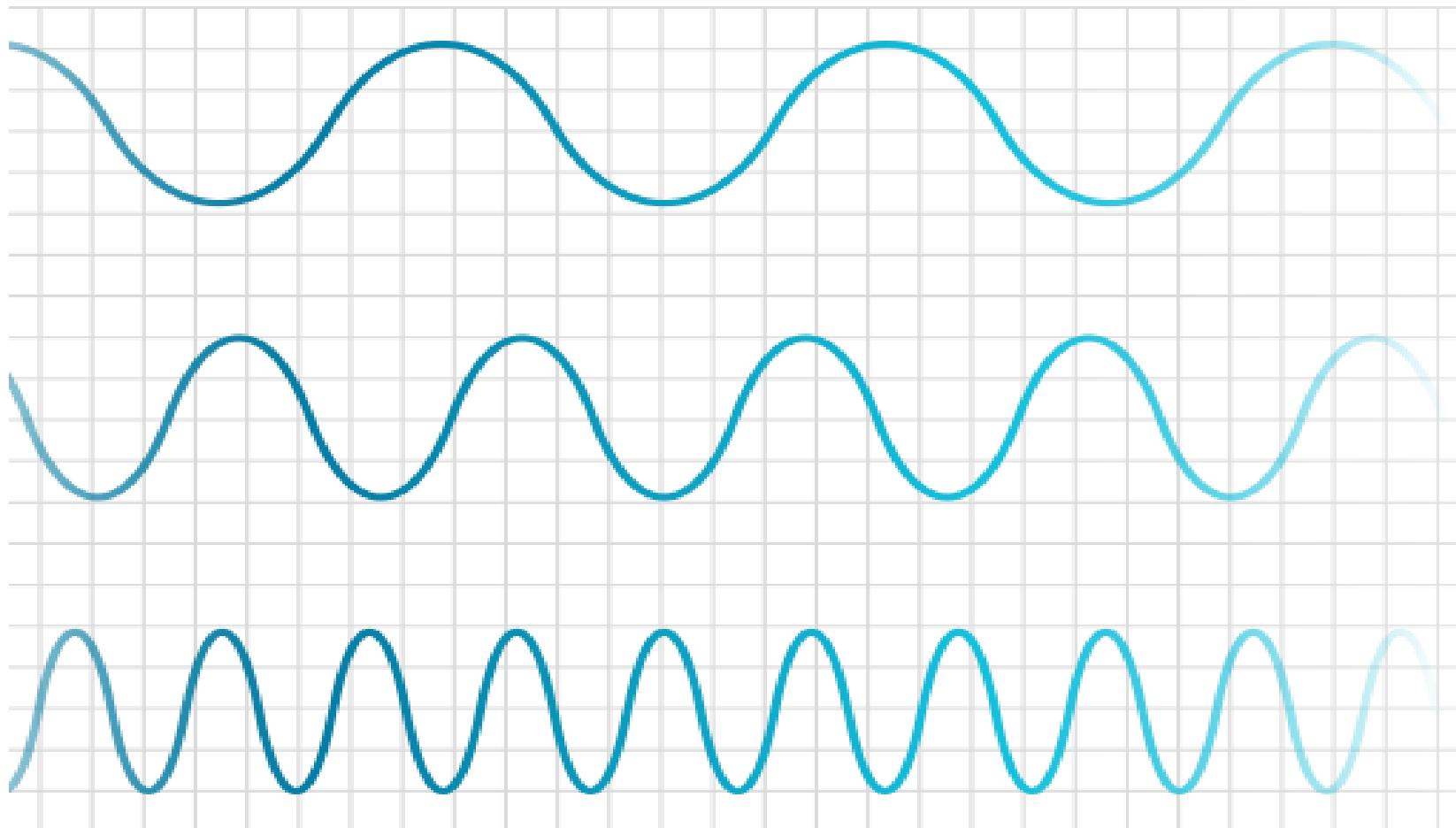
Digital Signal



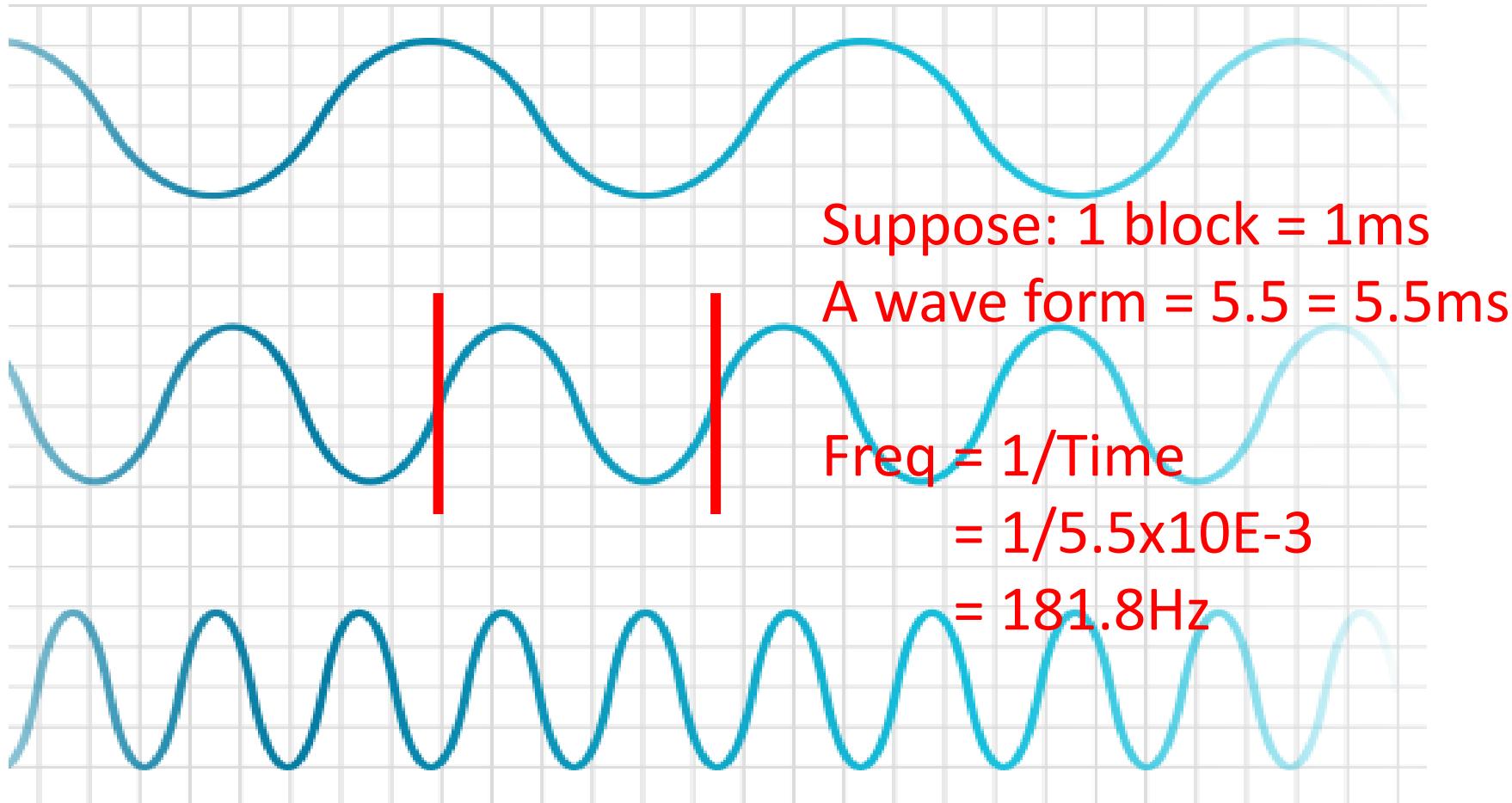
Signal Property



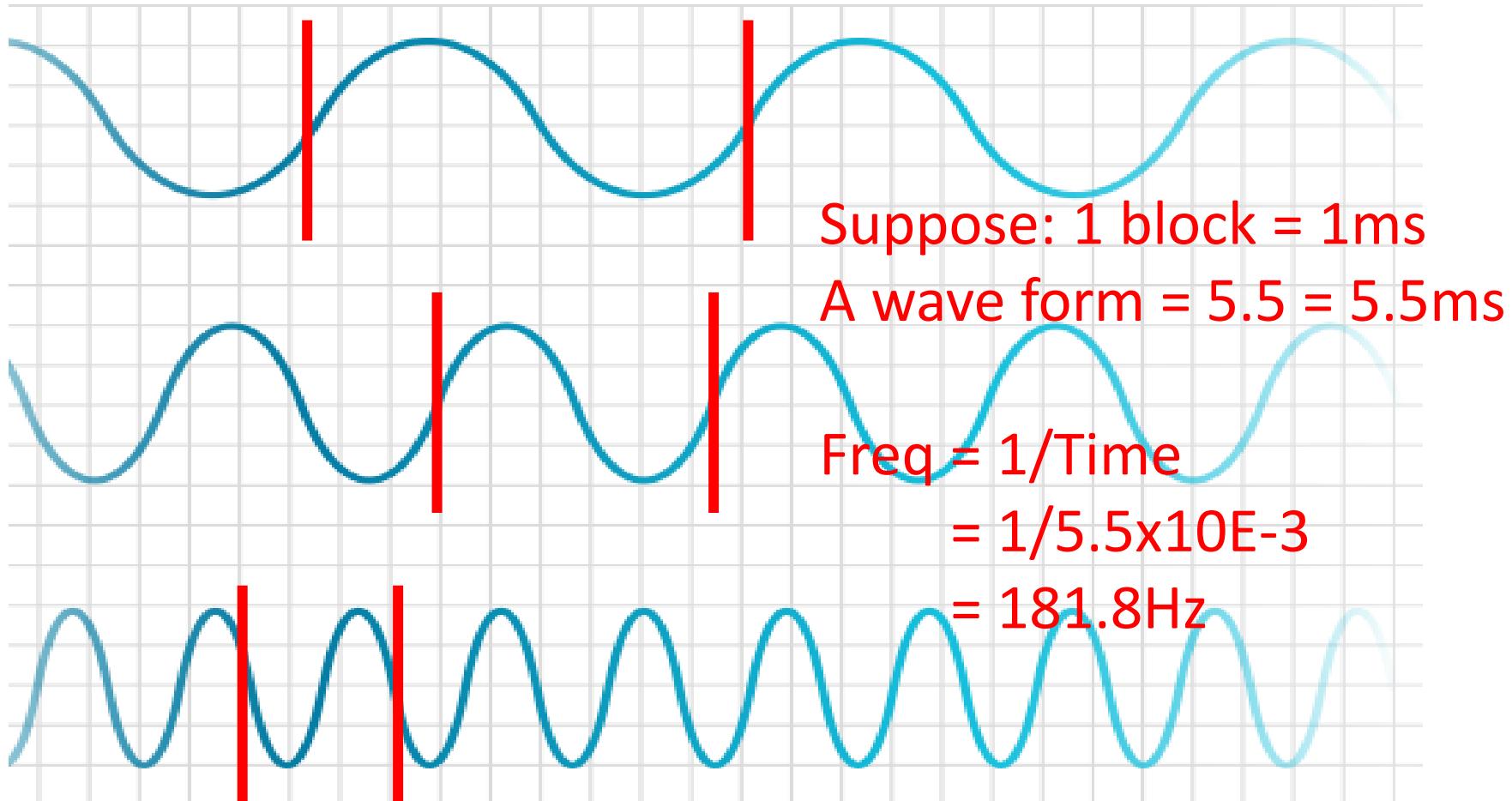
Which one is the low frequency?



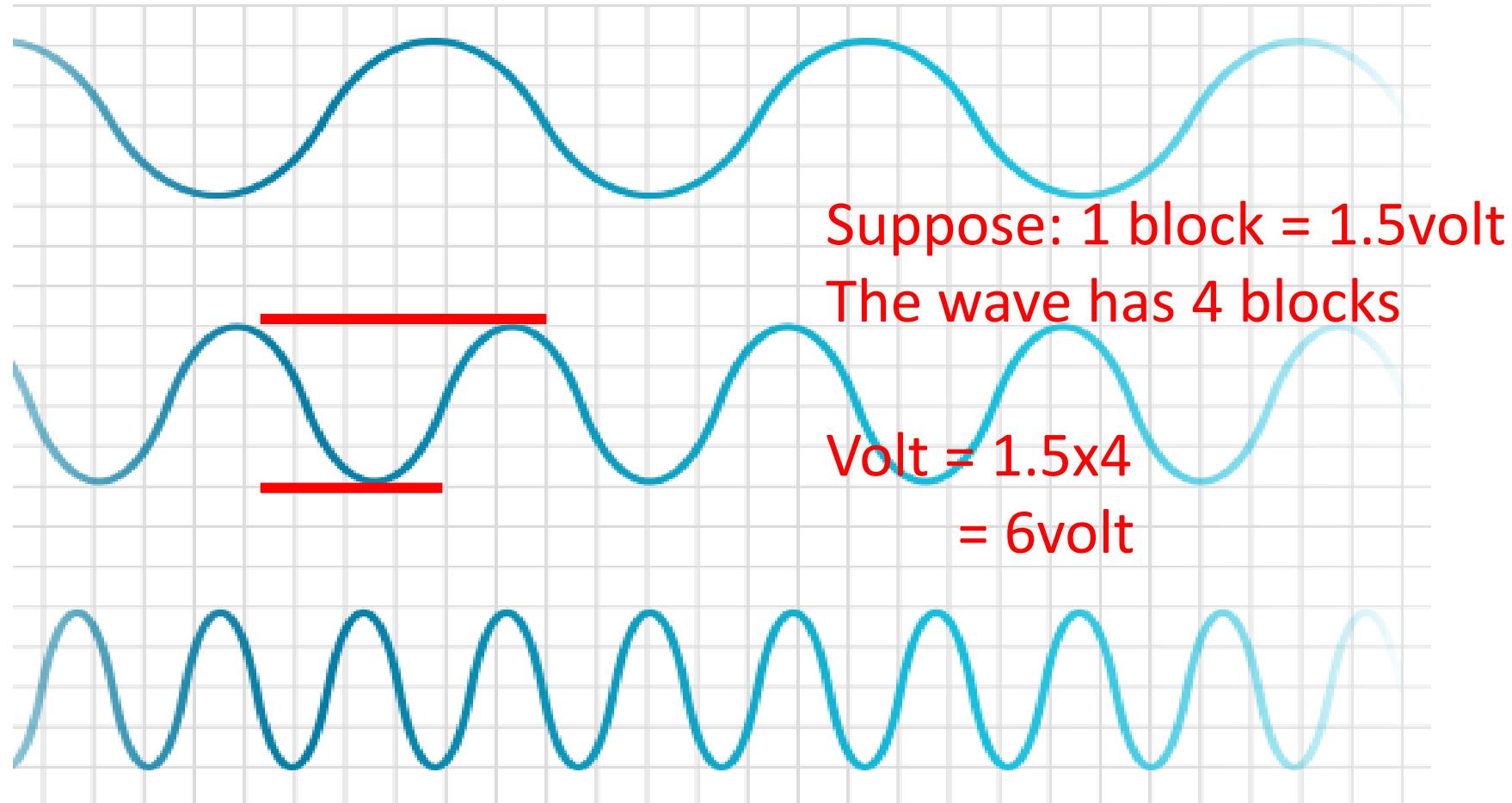
Which one is the low frequency?



Activity 4.2 Frequency calculation

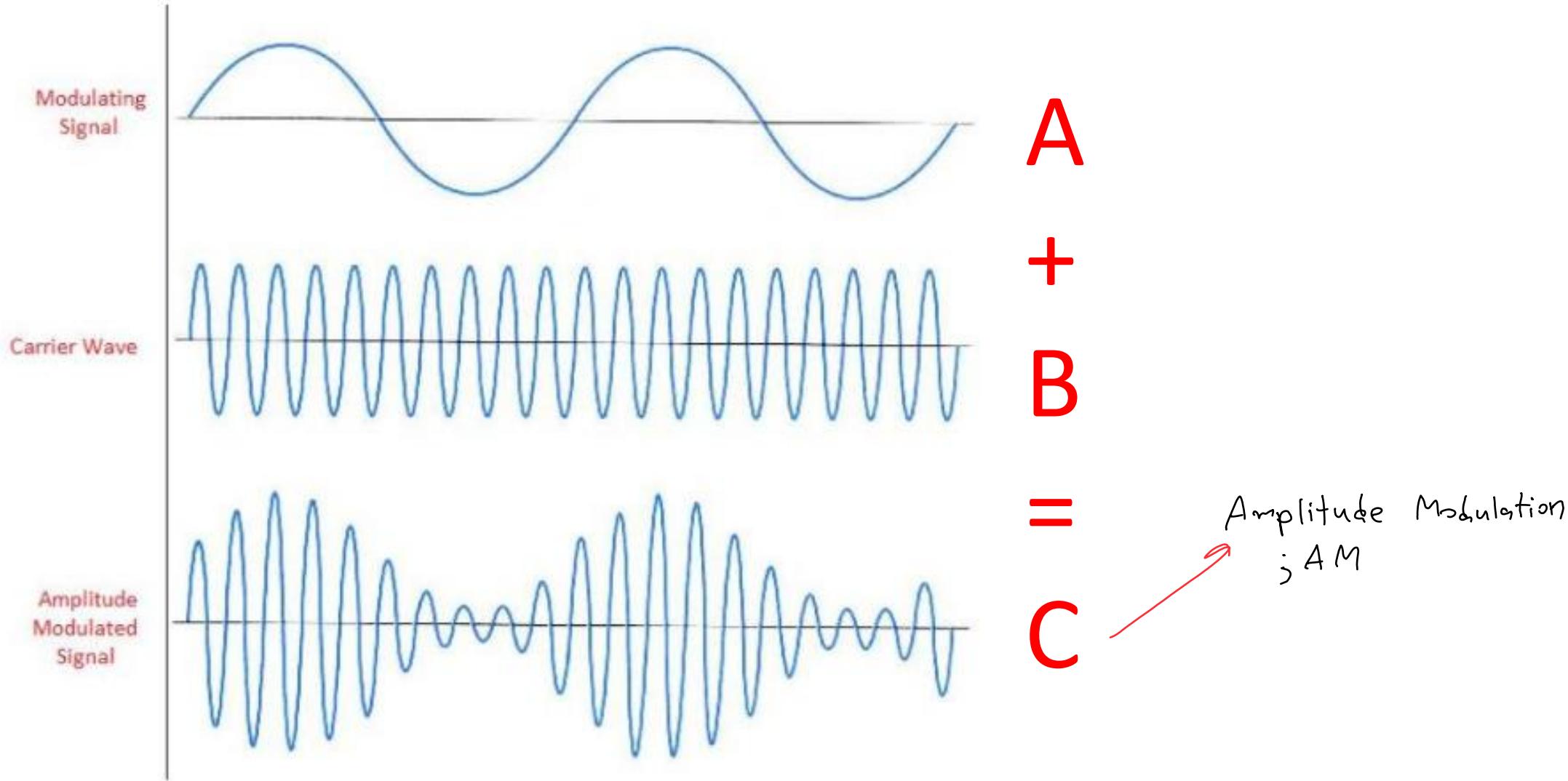


Amplitude, Voltage, Level

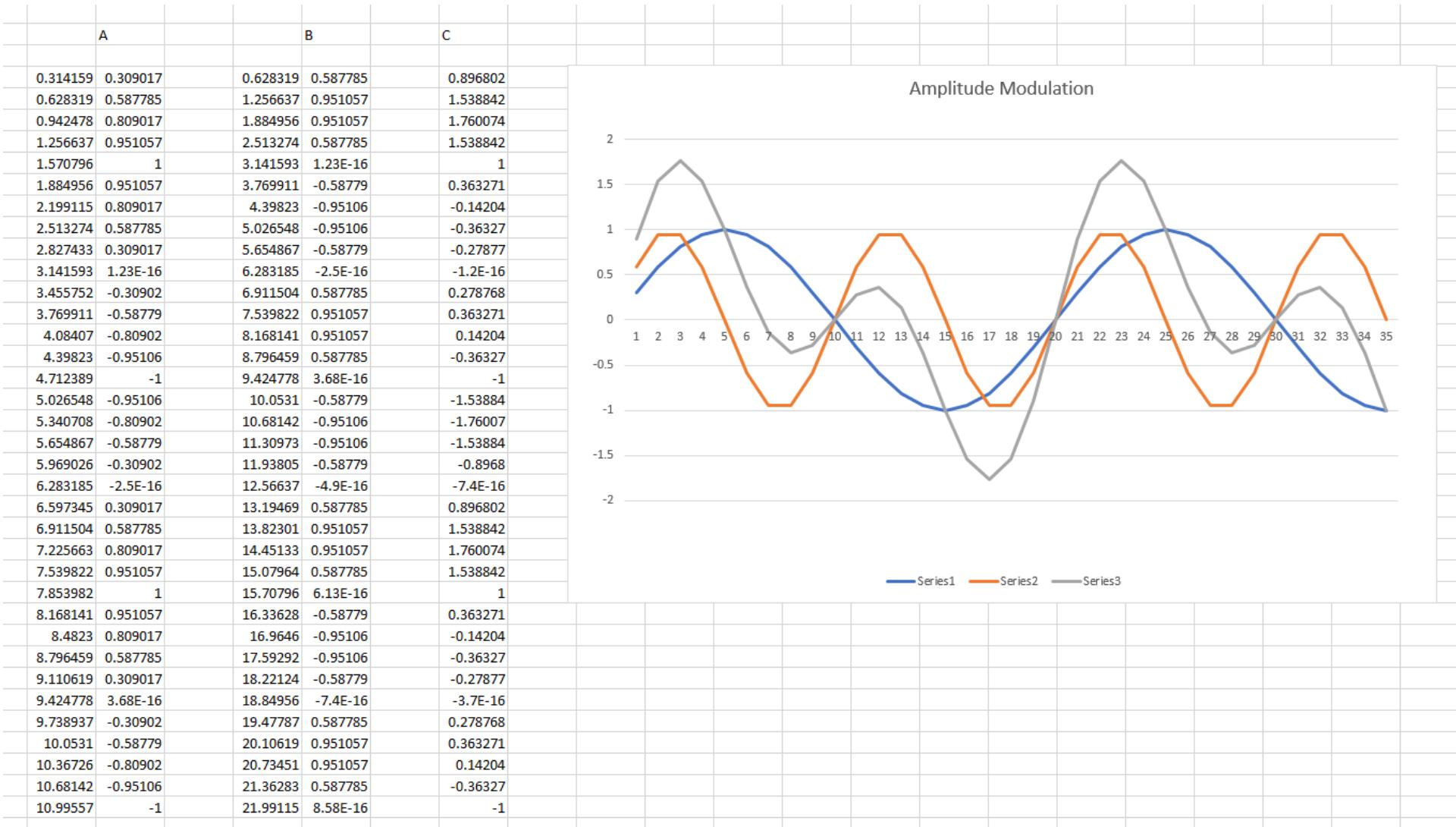


Modulation

ការលើនសម្រេចការណ៍
អាជីវការវិត្យលេខា



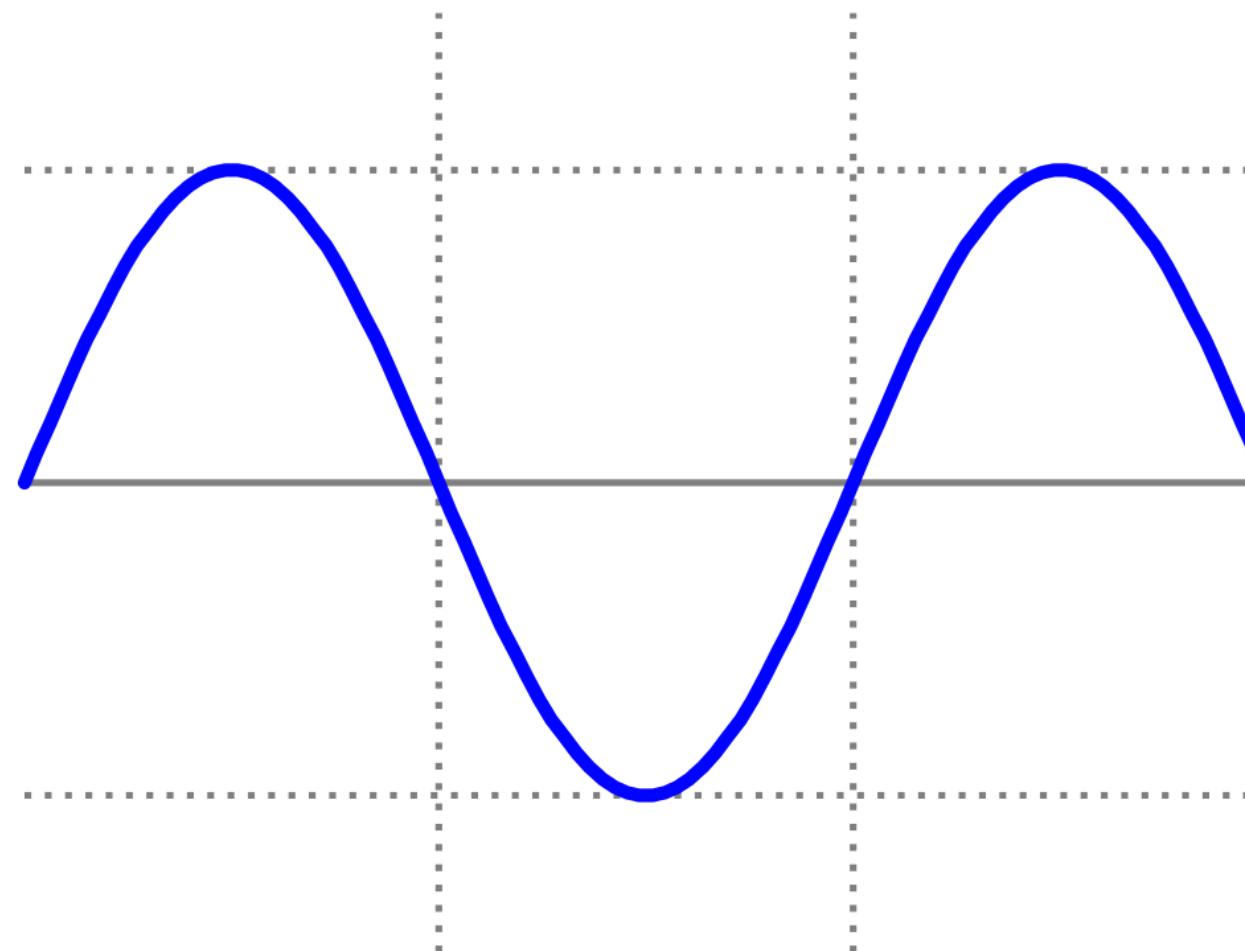
Activity 4.3 AM Simulation with Excel



Convert Analog Signal to Digital Signal

- Step1: Analog signal

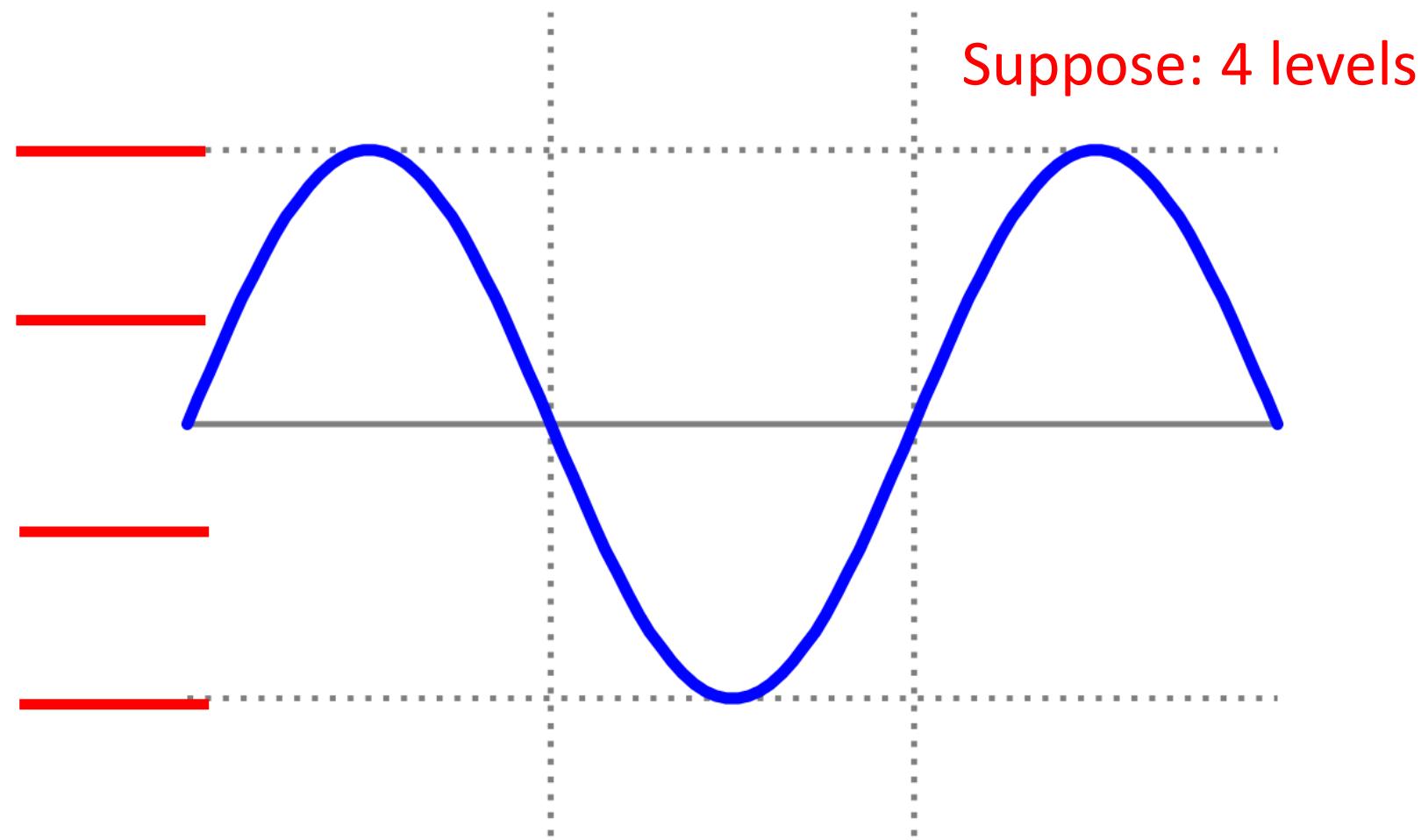
* Exam



2 Bits
00 01 10 11
4 levels

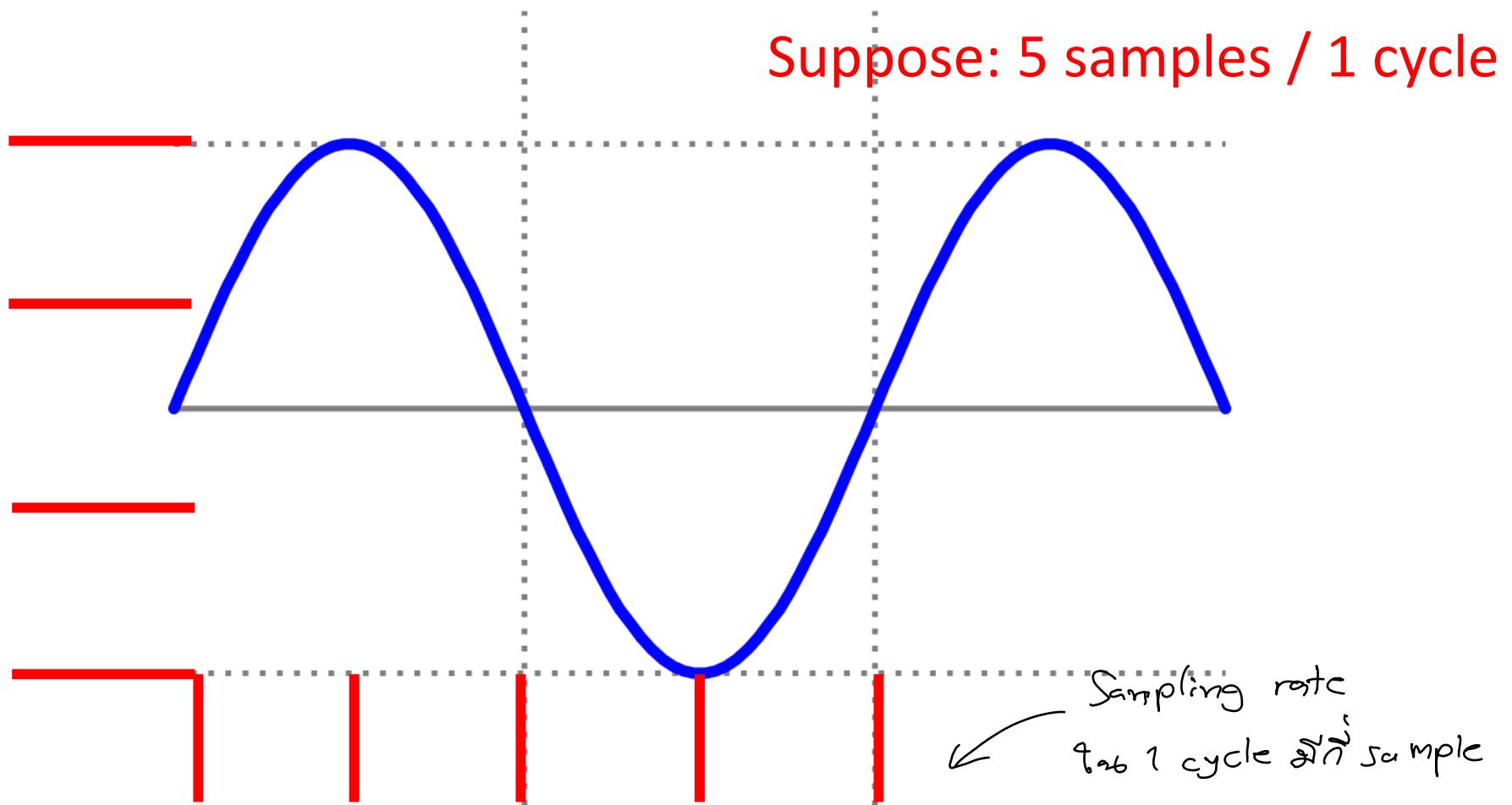
Convert Analog Signal to Digital Signal

- Step2: Define the number of levels (bits)



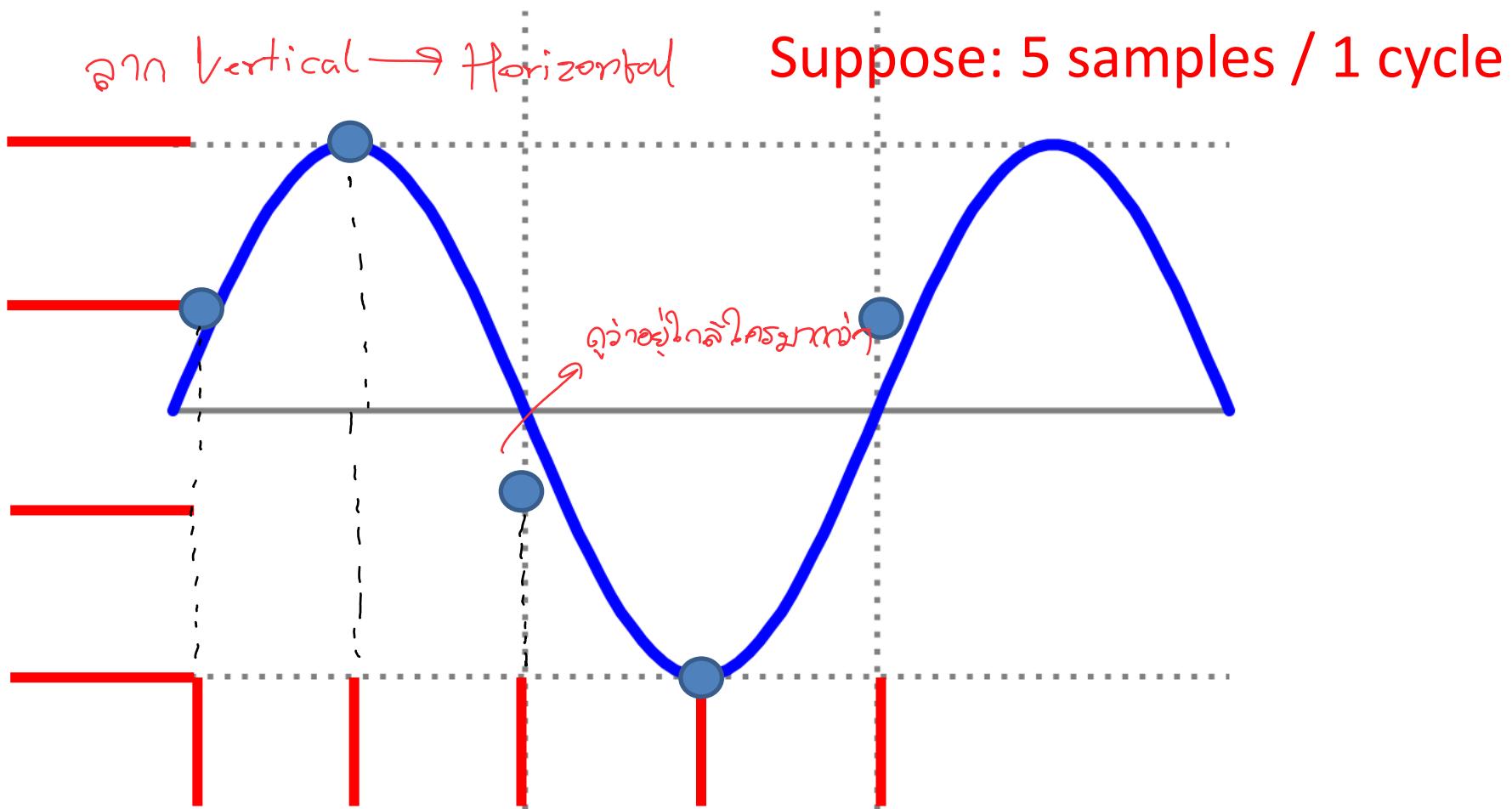
Convert Analog Signal to Digital Signal

- Step3: Define the number of sampling



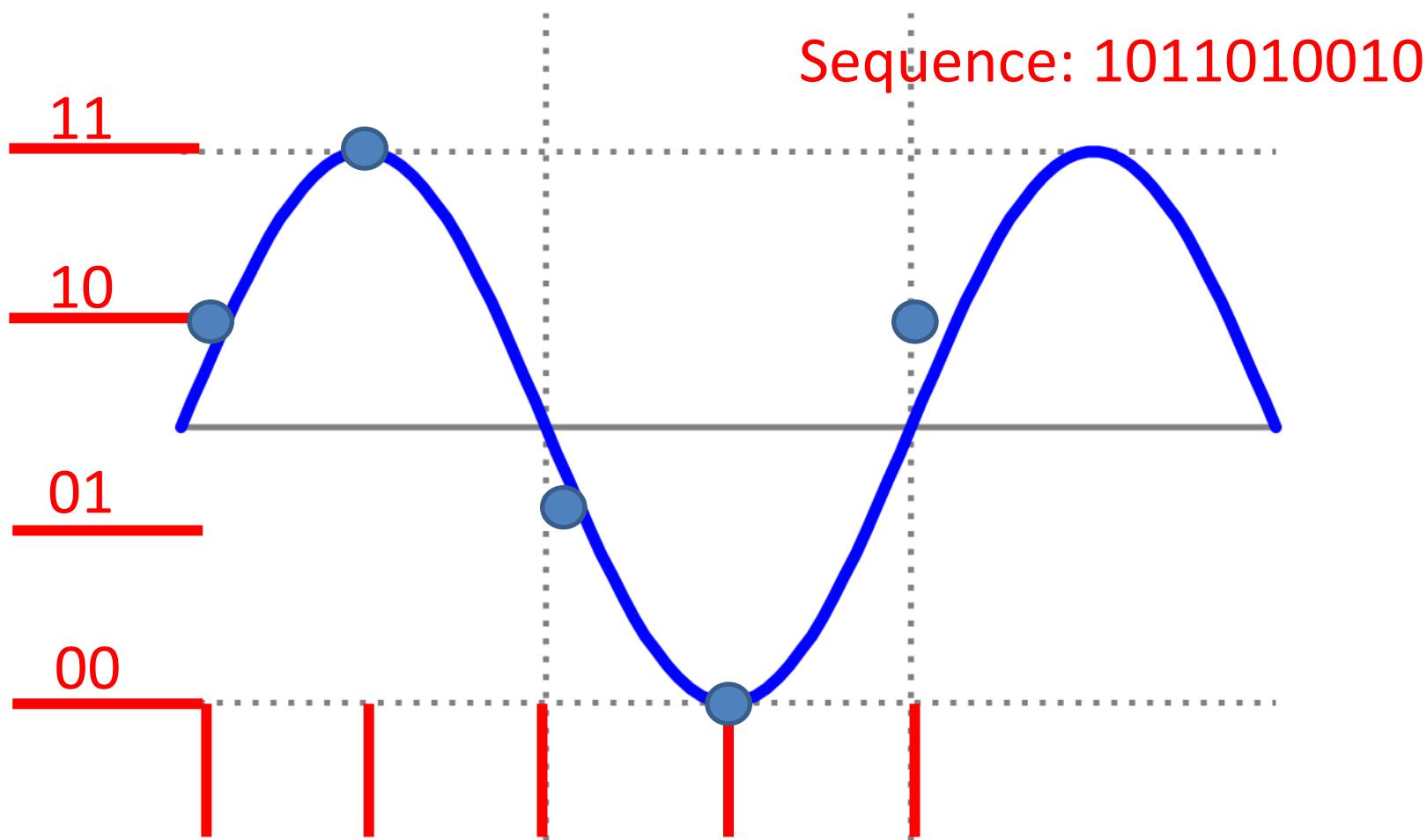
Convert Analog Signal to Digital Signal

- Step4: Map the level and sampling to the signal

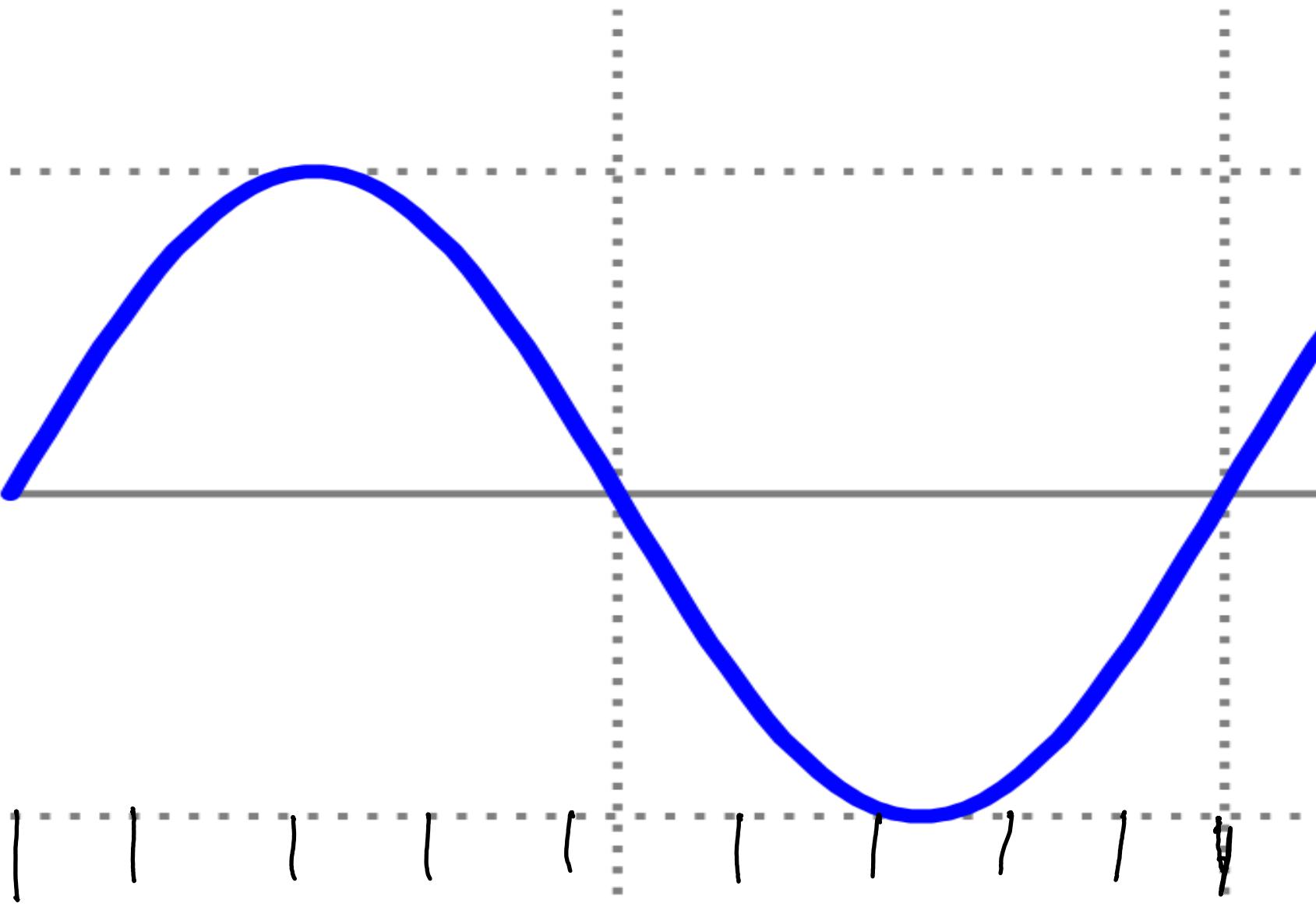


Convert Analog Signal to Digital Signal

- Step5: Reading digital signal



Activity 4.4 Drawing 8 levels and 10 sampling



Reference

- <https://www.quora.com/What-is-an-application-of-an-RS-flip-flop>
- <https://electronics.stackexchange.com/questions/jk-flip-flop-toggle>