Design Rules Verification Report

Filename : C:\Users\mmeagher\Documents\Projects\RomeoZe

Warnings
Total

Rule Violations
Clearance Constraint (Gap=10mil) (InNamedPolygon('GND_L02_P002')),(All)
Clearance Constraint (Gap=10mil) (All),(All)
Clearance Constraint (Gap=10mil) (InNamedPolygon('P3V_L03_P005')),(All)
Short-Circuit Constraint (Allowed=No) (All),(All)
Un-Routed Net Constraint ((All))
Width Constraint (Min=6mil) (Max=10mil) (Preferred=6mil) (All)
Width Constraint (Min=8mil) (Max=10mil) (Preferred=10mil) (InNet('P3V'))
Width Constraint (Min=8mil) (Max=30mil) (Preferred=10mil) (InNet('GND'))
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width
Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole To Hole Clearance (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver (Gap=3mil) (HasFootprint('VQFN-20 (3MMX3MM)'))
Silk to Silk (Clearance=10mil) (All),(All)
Component Clearance Constraint (Horizontal Gap = 10mil, Vertical Gap = 10mil)
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)
Total