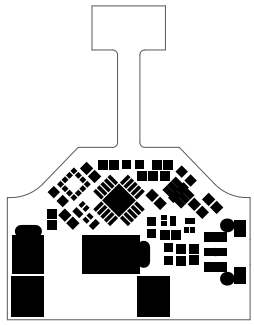


LED Top Overlay

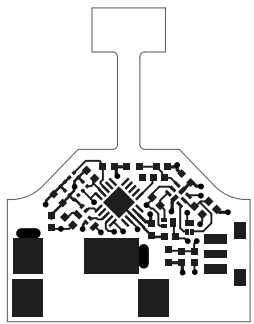
Board Outline

SIGSAUER



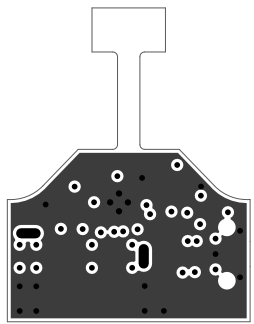
Top Coverlay

Board Outline



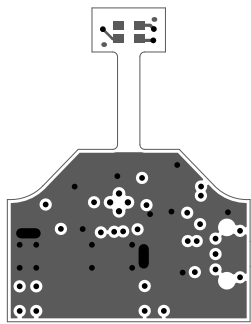
Top Layer 1

Board Outline



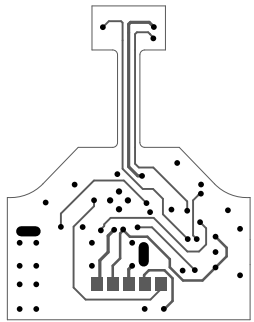
Layer 2

Board Outline



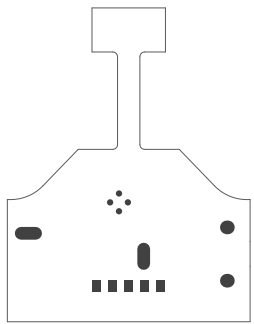
Layer 3/Top LED

Board Outline



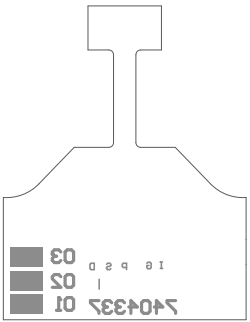
Bottom Layer

Board Outline



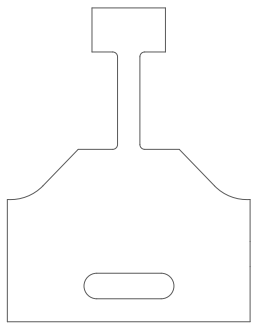
Bottom Coverlay

Board Outline



Bottom Overlay

Board Outline



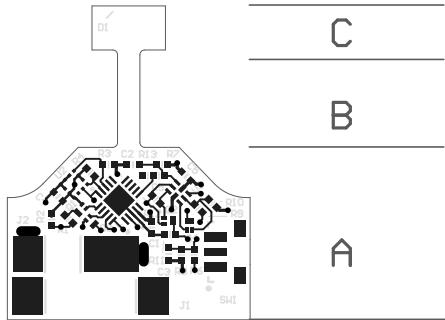
Cutout in Stiffener

Board Outline

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Top Layer 1

LED Top Overlay

Fab Notes

Board Outline

- PCB Fab Notes (dimensions in mm)---
1. Refer to 7404337 drawing pdf for additional requirements.
 2. For PCB stackup ('A', 'B', 'C'), refer to stackup file in Project Outputs > FAB folder.
 3. Finish: Exposed conductive pads and traces plated with ENIG per IPC-4552.
 4. Soldermask: CM is allowed to alter soldermask expansion as required.
 5. Layer-to-layer registration <0.152.
 6. PCB to be lead free and RoHS compliant, and compatible with RoHS assembly methods.
 7. Inner layer copper pullback from board edge allowed.
 8. Silkscreen: white, permanent, non-conductive ink. Keep clear of solder pads.
 9. No controlled impedance requirements.
 10. Hole tolerance: +/-0.076 (drill position); diameter +/-0.076 (PTH).
 11. Coverlay may be added over black in the C section of stackup to create smaller solder dams to prevent solder bridges.
 12. There are two additional files for top paste and solder for the layer 3 top.
 13. Stiffener on the bottom side of section A needs a mechanical cutout for 5-pin, see drawing.
 14. Mounting slots for J2 show plating through the stiffener that shouldn't be there the plating should not extend to stiffener.
 15. Bottom Coverlay Print should be printed on the bottom of the stiffener, not the bottom of the flex circuit.



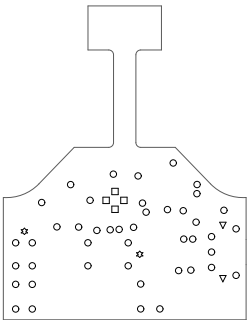
18 Industrial Drive Exeter, NH 03833

Title			CIRCUIT BOARD, ROMEO ZERO, GEN2 BOARD	
Size	Number		Revision	
A	7404337		00	
Date:	3/30/23		Sheet	1 of 1
File:			Drawn By:	MM

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DrillDrawing

Board Outline

Hole tolerance: +/- .076 (drill position): diameter +/- .076 (PTH).

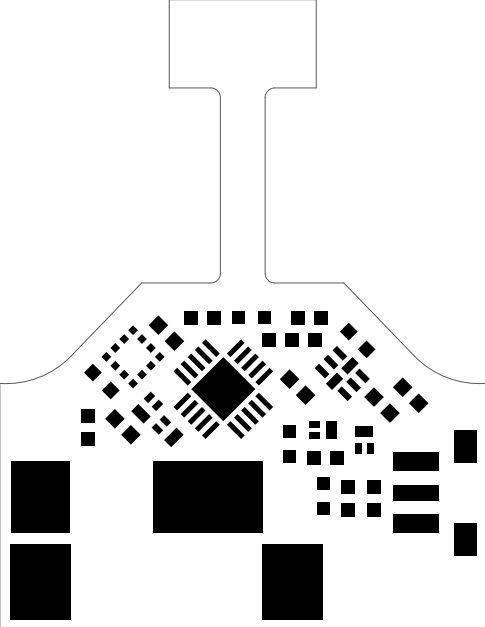
Symbol	Count	Hole Size	Hole Length	Routed Path Length	Plated	Hole Type
☆	2	17.00mil (0.432mm)	62.00mil (1.575mm)	45.00mil (1.143mm)	PTH	Slot
▽	2	35.00mil (0.889mm)	-	-	NPTH	Round
□	4	11.81mil (0.300mm)	-	-	PTH	Round
○	44	8.00mil (0.203mm)	-	-	PTH	Round
52 Total						

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



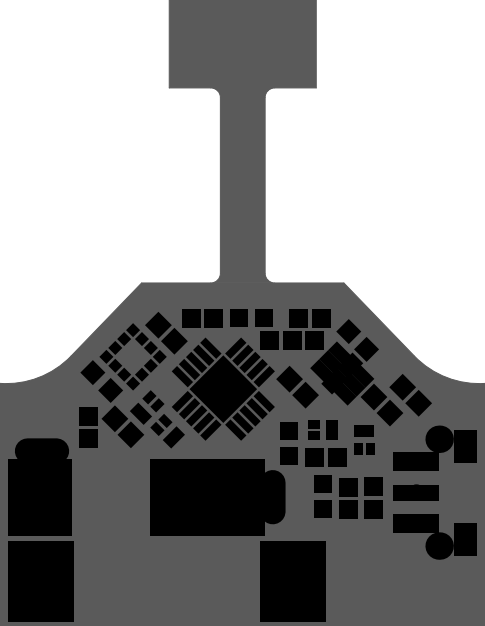
18 Industrial Drive Exeter, NH 03833

Title			CIRCUIT BOARD, ROMEO ZERO, GEN2 BOARD		
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A	7404337			00	
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File:				Drawn By: MM	



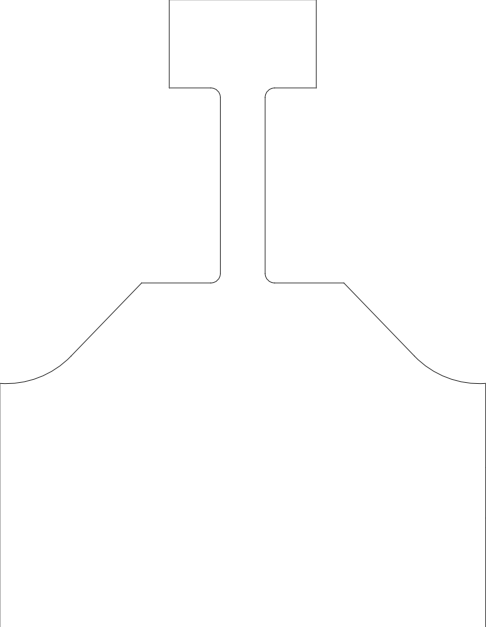
TopPaste

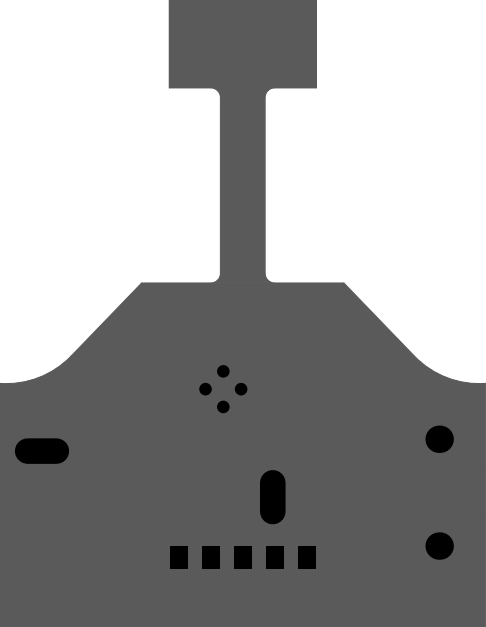
Board Outline



Top Coverlay

Board Outline





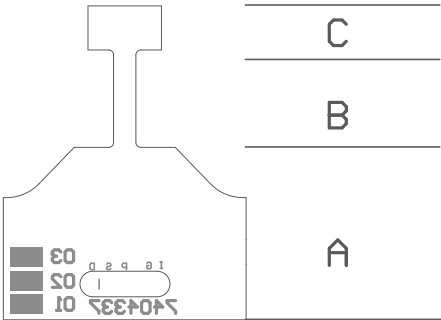
Bottom Coverlay

Board Outline

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Bottom Overlay

- Fab Notes
- Assembly Notes
- Cutout in Stiffener
- Board Outline

- PCA Assembly Notes--
- 1. Assemble per IPC-A-610, Class 2. Double sided assembly.
 - 2. Lead free, No Wash, RoHS compliant assembly.
 - 4. ESD sensitive assembly. Package and handle in accordance with ESD procedures.
 - 5. Optical components at D1. Keep D1 lens clear of debris and contaminants.
 - 6. No component at J3, programming pads. Keep pads clear of contaminants.
 - 7. Refer to 7404337 dwg pdf for additional requirements.
 - 8. The 7404337 board will be used for three different BOMS



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