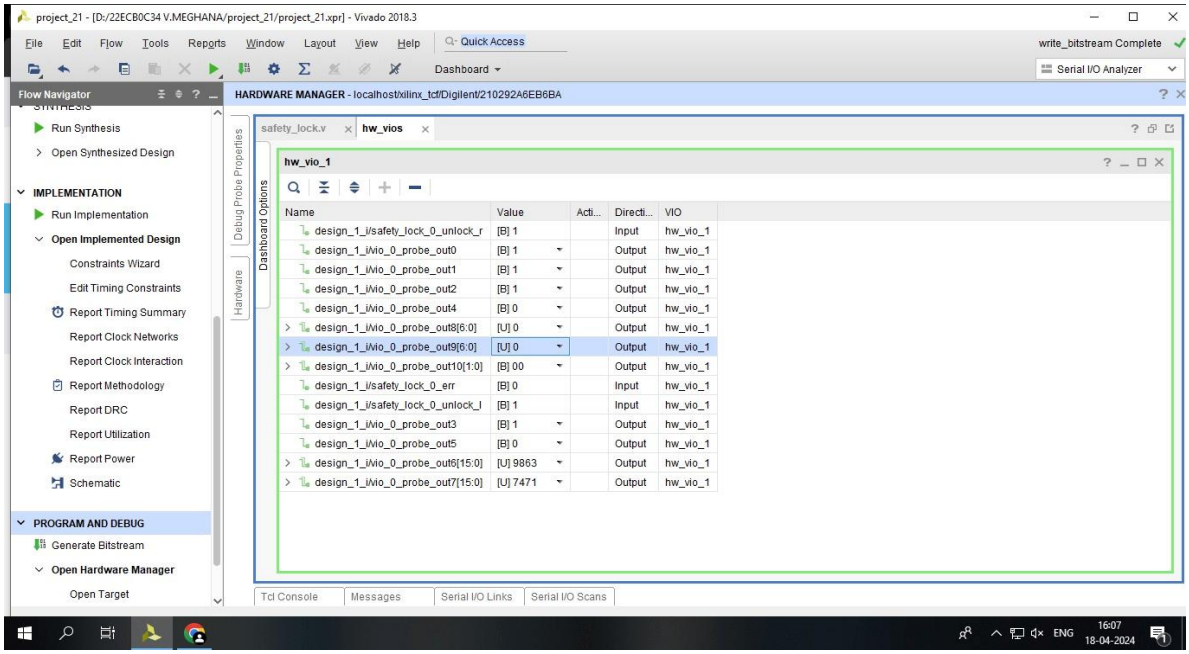
project_21 - [D:/22ECB0C34 V.MEGHANA/project_21/project_21.xpr] - Vivado 2018.3
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Dashboard
Serial I/O Analyzer
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HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210292A6EB6BA
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Open Target
safety_lock.v
hw_vios
hw_vio_1
Debug Probe Properties
Dashboard Options
Hardware
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Acti...
Directi...
VIO
design_1_i/safety_lock_0_unlock_r [B] 1 Input hw_vio_1
design_1_i/vio_0_probe_out0 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out1 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out2 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out4 [B] 0 Output hw_vio_1
design_1_i/vio_0_probe_out8[6:0] [U] 0 Output hw_vio_1
design_1_i/vio_0_probe_out9[6:0] [U] 0 Output hw_vio_1
design_1_i/vio_0_probe_out10[1:0] [B] 00 Output hw_vio_1
design_1_i/safety_lock_0_err [B] 0 Input hw_vio_1
design_1_i/safety_lock_0_unlock_l [B] 1 Input hw_vio_1
design_1_i/vio_0_probe_out3 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out5 [B] 0 Output hw_vio_1
design_1_i/vio_0_probe_out6[15:0] [U] 9863 Output hw_vio_1
design_1_i/vio_0_probe_out7[15:0] [U] 7471 Output hw_vio_1
Tcl Console
Messages
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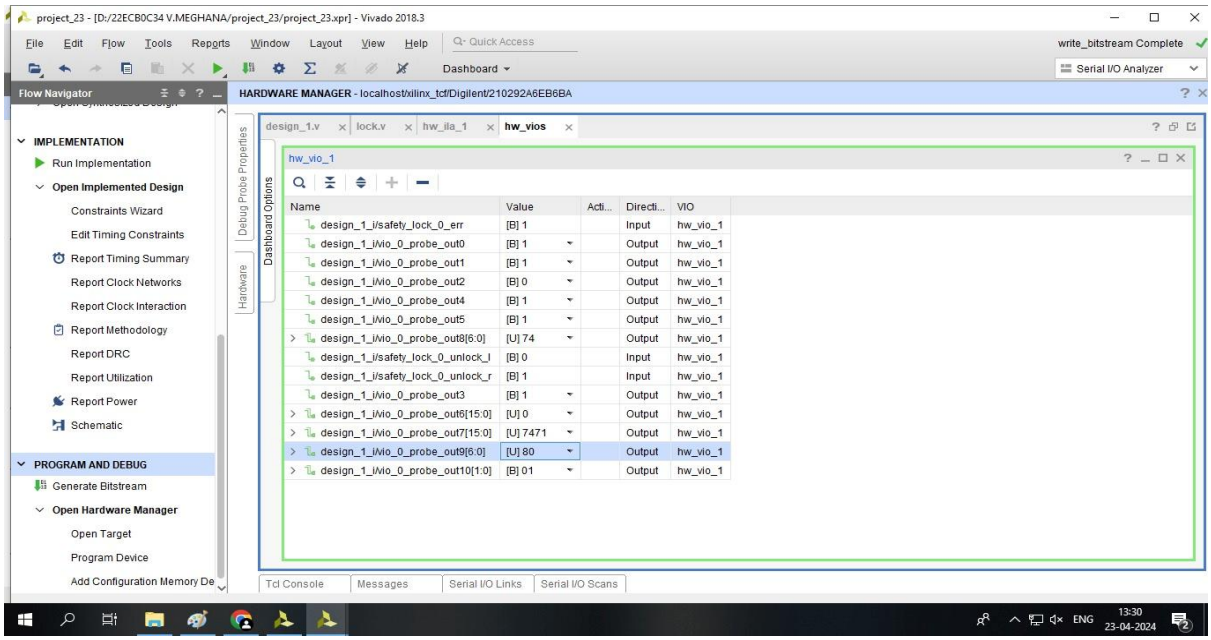
16:07
18-04-2024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Dashboard Options
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VIO
design_1_i/safety_lock_0_err [B] 1 Input hw_vio_1
design_1_i/vio_0_probe_out0 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out1 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out2 [B] 0 Output hw_vio_1
design_1_i/vio_0_probe_out4 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out5 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out8[6:0] [U] 74 Output hw_vio_1
design_1_i/safety_lock_0_unlock_l [B] 0 Input hw_vio_1
design_1_i/safety_lock_0_unlock_r [B] 1 Input hw_vio_1
design_1_i/vio_0_probe_out3 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out6[15:0] [U] 0 Output hw_vio_1
design_1_i/vio_0_probe_out7[15:0] [U] 7471 Output hw_vio_1
design_1_i/vio_0_probe_out9[6:0] [U] 80 Output hw_vio_1
design_1_i/vio_0_probe_out10[1:0] [B] 01 Output hw_vio_1
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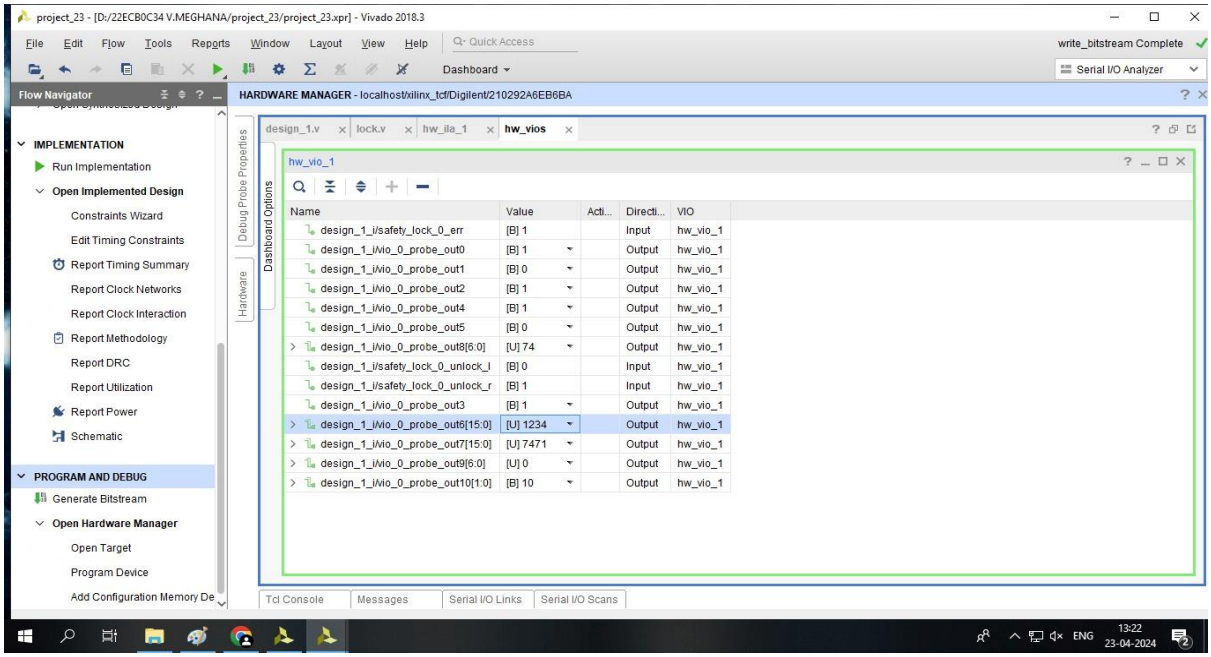
23-04-2024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VIO
design_1_i/safety_lock_0_err [B] 1 Input hw_vio_1
design_1_i/vio_0_probe_out0 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out1 [B] 0 Output hw_vio_1
design_1_i/vio_0_probe_out2 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out4 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out5 [B] 0 Output hw_vio_1
design_1_i/vio_0_probe_out8[6:0] [U] 74 Output hw_vio_1
design_1_i/safety_lock_0_unlock_l [B] 0 Input hw_vio_1
design_1_i/safety_lock_0_unlock_r [B] 1 Input hw_vio_1
design_1_i/vio_0_probe_out3 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out6[15:0] [U] 1234 Output hw_vio_1
design_1_i/vio_0_probe_out7[15:0] [U] 7471 Output hw_vio_1
design_1_i/vio_0_probe_out9[6:0] [U] 0 Output hw_vio_1
design_1_i/vio_0_probe_out10[1:0] [B] 10 Output hw_vio_1
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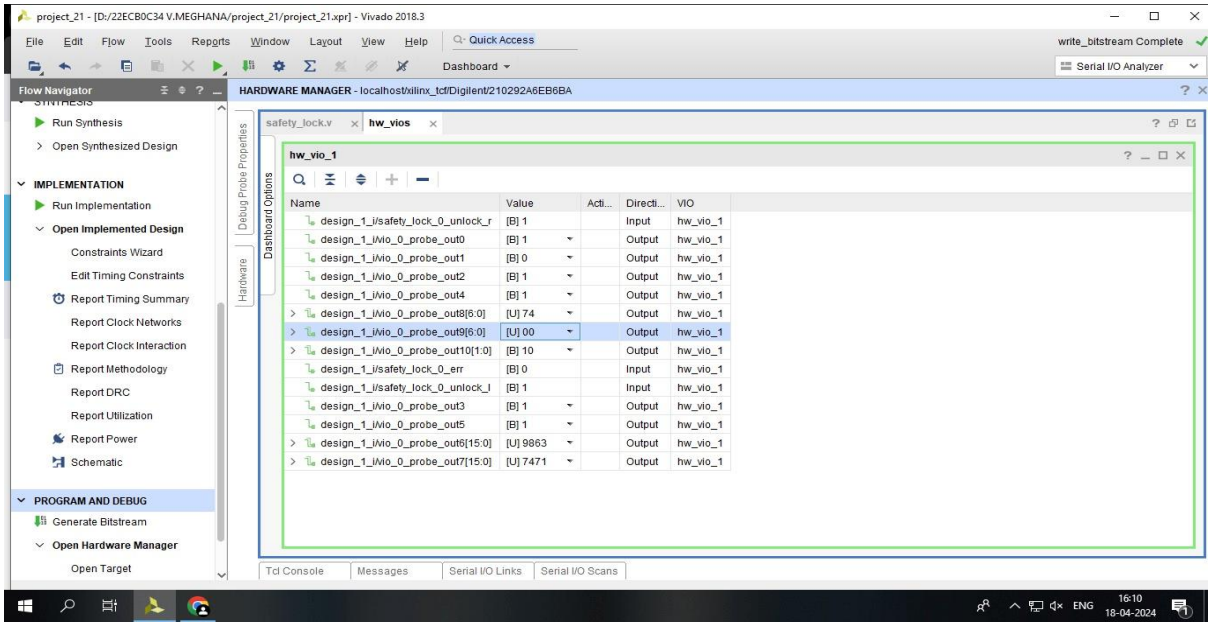
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design_1_i/safety_lock_0_unlock_r [B] 1 Input hw_vio_1
design_1_i/vio_0_probe_out0 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out1 [B] 0 Output hw_vio_1
design_1_i/vio_0_probe_out2 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out4 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out8[6:0] [U] 74 Output hw_vio_1
design_1_i/vio_0_probe_out9[6:0] [U] 00 Output hw_vio_1
design_1_i/vio_0_probe_out10[1:0] [B] 10 Output hw_vio_1
design_1_i/safety_lock_0_err [B] 0 Input hw_vio_1
design_1_i/safety_lock_0_unlock_l [B] 1 Input hw_vio_1
design_1_i/vio_0_probe_out3 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out5 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out6[15:0] [U] 9863 Output hw_vio_1
design_1_i/vio_0_probe_out7[15:0] [U] 7471 Output hw_vio_1
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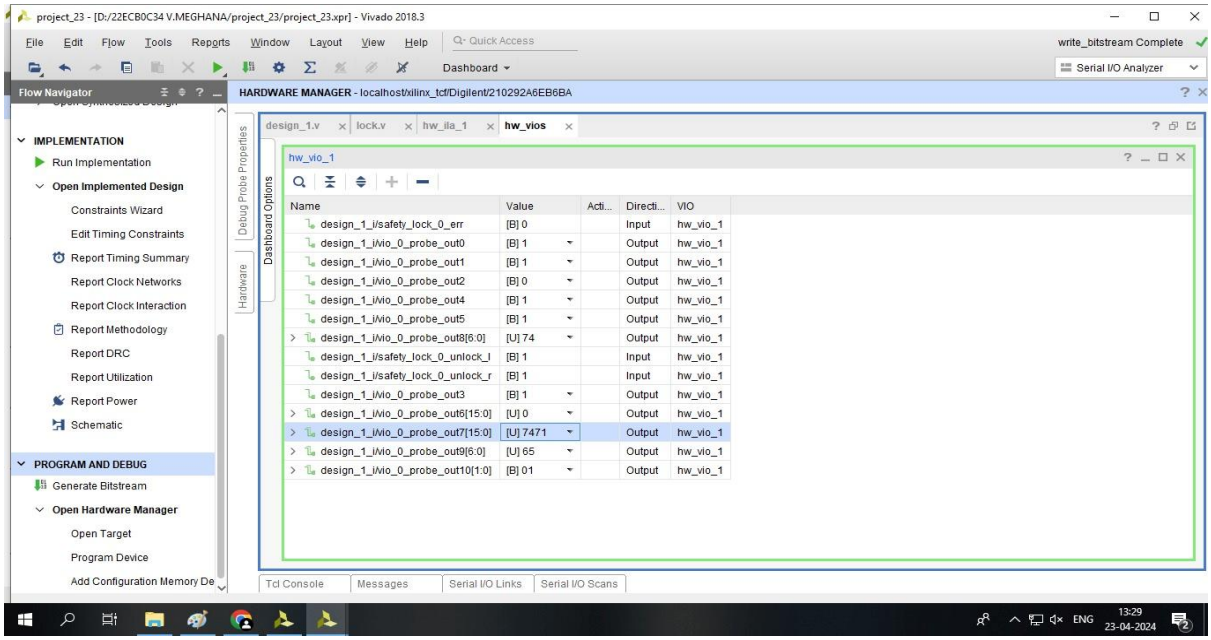
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VIO
design_1_i/safety_lock_0_err [B] 0 Input hw_vio_1
design_1_i/vio_0_probe_out0 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out1 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out2 [B] 0 Output hw_vio_1
design_1_i/vio_0_probe_out4 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out5 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out8[6:0] [U] 74 Output hw_vio_1
design_1_i/safety_lock_0_unlock_l [B] 1 Input hw_vio_1
design_1_i/safety_lock_0_unlock_r [B] 1 Input hw_vio_1
design_1_i/vio_0_probe_out3 [B] 1 Output hw_vio_1
design_1_i/vio_0_probe_out6[15:0] [U] 0 Output hw_vio_1
design_1_i/vio_0_probe_out7[15:0] [U] 7471 Output hw_vio_1
design_1_i/vio_0_probe_out9[6:0] [U] 65 Output hw_vio_1
design_1_i/vio_0_probe_out10[1:0] [B] 01 Output hw_vio_1
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
ENG
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23-04-2024