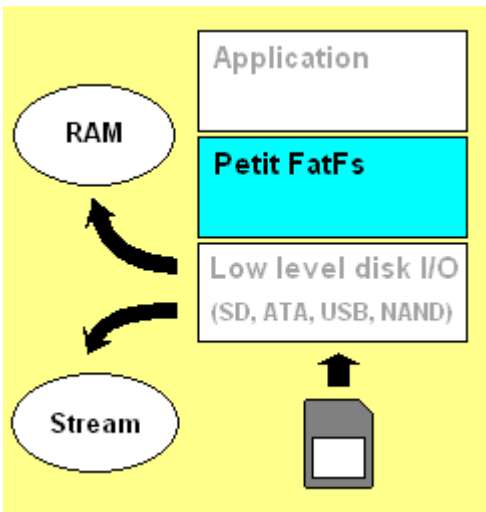## 6. Software Details:

6.1 *FAT File System*

We have used [Petit FatFs](#) *module which is a free software and is opened for education, research and development.*

Petit FatFs is a sub-set of FatFs module for tiny 8-bit microcontrollers. It is written in compliance with ANSI C and completely separated from the disk I/O layer. It can be incorporated into the tiny microcontrollers with a small memory even if the RAM size is less than sector size.
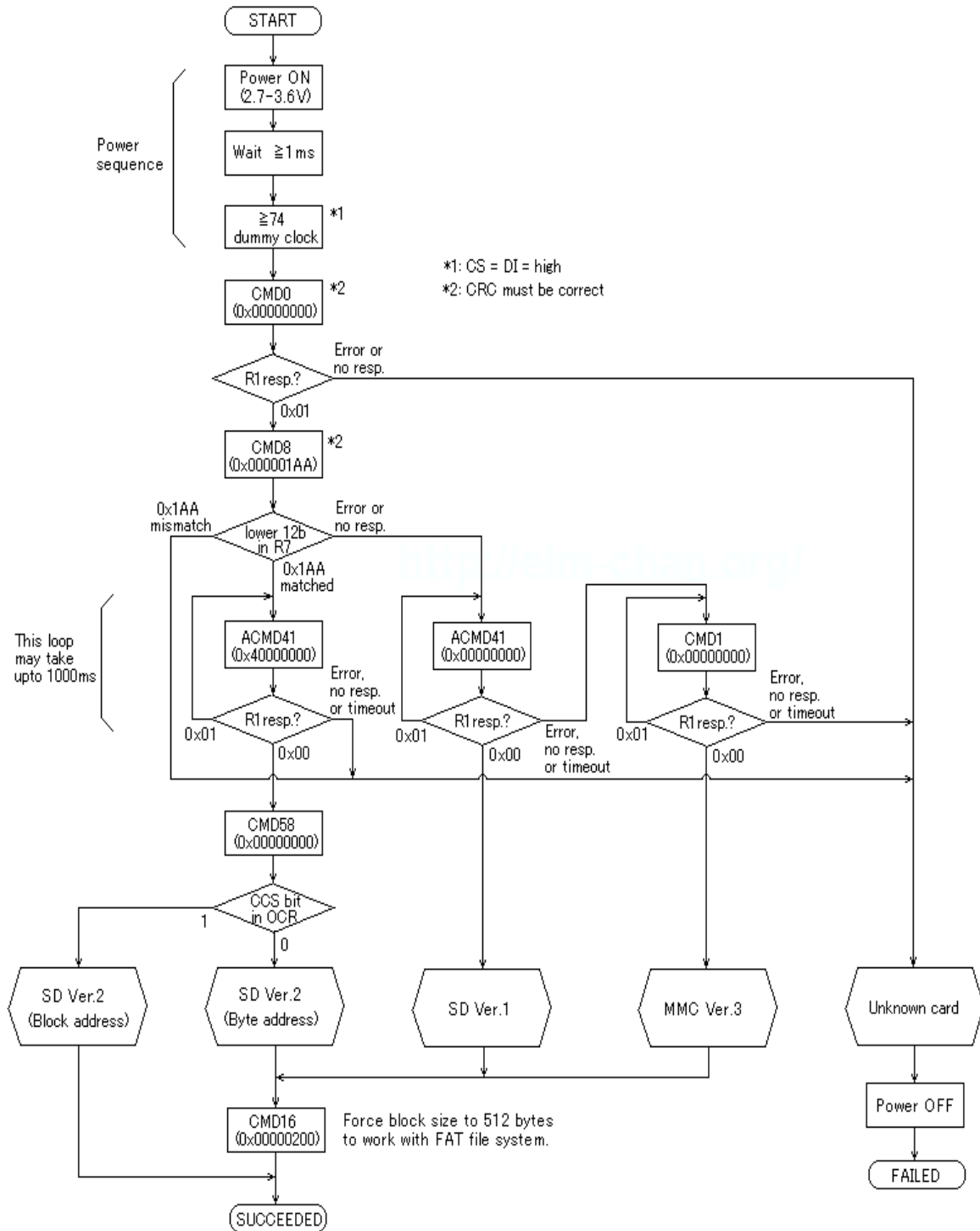
Features:

- Very small RAM consumption (44 bytes work area + certain stack).
- Very small code size (2K-4K bytes).
- Supports FAT32.
- Single volume and Single file.
- File write function with some restrictions.

6.2 *SD card initialization*

Following Flow chart describes the Initialization steps require for SD card initialization.

SDC/MMC initialization flow

START

Power ON
(2.7-3.6V)

Wait ≧1ms

≧74
dummy clock   *1

CMD0
(0x00000000)   *2

*1: CS = DI = high
*2: CRC must be correct

R1 resp.?

Error or
no resp.

0x01

CMD8
(0x000001AA)   *2

0x1AA
mismatch

lower 12b
in R7

Error or
no resp.

0x1AA
matched

This loop
may take
upto 1000ms

ACMD41
(0x40000000)

ACMD41
(0x00000000)

CMD1
(0x00000000)

Error,
no resp.
or timeout

R1 resp.?

0x01   0x00

Error,
no resp.
or timeout

R1 resp.?

0x01   0x00

Error,
no resp.
or timeout

R1 resp.?

0x01   0x00

Error,
no resp.
or timeout

CMD58
(0x00000000)

CCS bit
in OCR

1   0

SD Ver.2
(Block address)

SD Ver.2
(Byte address)

SD Ver.1

MMC Ver.3

Unknown card

Power OFF

CMD16
(0x00000200)

Force block size to 512 bytes
to work with FAT file system.

SUCCEEDED

FAILED

6.3 *SPI Details*

SPI (Serial Peripheral Interface) is one of the on-board inter-IC communication interfaces. The number of signals of SPI, three or four wires.

SPI Structure:

The basic structure of the SPI is shown in right image. The master IC and the slave IC are tied with three signal lines, *SCLK* (Serial Clock), *MISO* (Master-In Slave-Out) and *MOSI* (Master-Out Slave-In), and contents of both 8-bit shift registers are exchanged with the shift clock driven by master IC. Additionally an *SS* (Slave Select) signal other than above three is used to synchronize start of packet or byte boundary, and for realize multi-slave configuration simultaneously. Most slave ICs assign different pin names, such as DI, DO and CS, to the SPI interface. For one-way transfer device, such as DAC and single channel ADC, either of data lines may be omitted. The data bits are shifted in *MSB first*.