Digital Logic Circuit Simulator

Group Members:
Meghanad Shingate (09307608)
Nirbhay Rane (09307905)
Bharat Kumar (09307904)

Group : 13
AE663 Intermediate Presentation

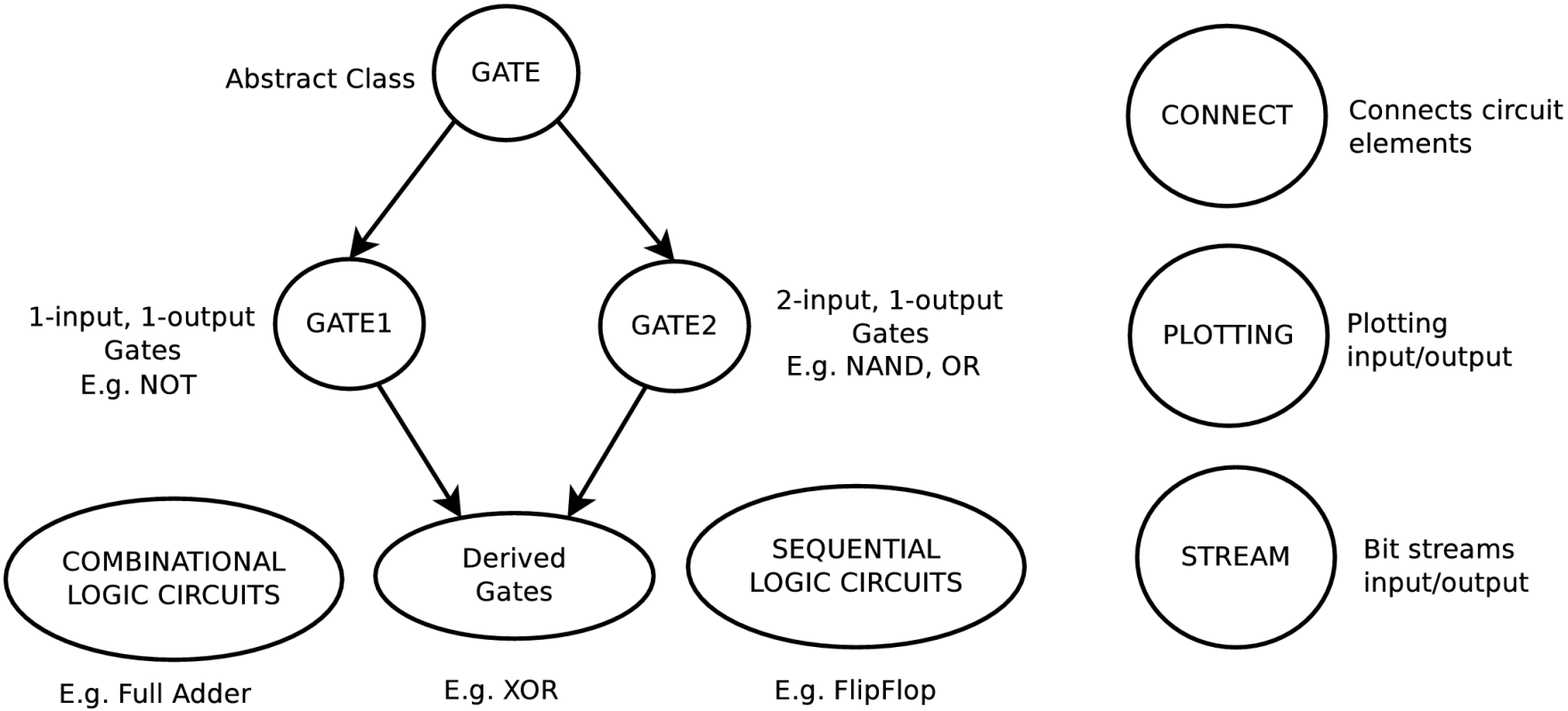
November 3, 2011

Problem Statement

Implementation of Logic Circuit Simulator using Python

- Basic logic gates (e.g. AND, OR, NOR, etc.)
- Combinational Logic circuits (e.g. Half adder, Full adder, Mux/Demux etc.)
- Sequential Logic circuits (e.g Flip-Flop, Counters, Shift registers etc.)
- Digital signal sources (e.g. clock source)

Implementation Details



Issues and Status

Issues/Difficulties

- Textual representation of circuit schematic
- Tracking the signal propagation - event driven, multi-tier circuit
- Managing connection between combinational and sequential circuit elements
- Detection of floating pins

Issues and Status

Issues/Difficulties

- Textual representation of circuit schematic
- Tracking the signal propagation - event driven, multi-tier circuit
- Managing connection between combinational and sequential circuit elements
- Detection of floating pins

Project Status

- Approximately 20% work is done
- Number of hours put : 3 hours per person