1. Introduce Your Self?
2. Tell me about your rescent Project?
3. What is setup/hold timing?
4. If your block got cleaned in HM level, But when ran into top level the internal timing Path getting violation ? What might be the reason?
5. How many Violations are got in you desisgn after constaints are fixed?
6. Which Timing violations are important to clean first? Either setup or hold?
7. What it menat by MPW? How to fix it?
8. For example you have require pulse width is 290ps and rise delay is 30 ps and Fall delay is 40ps, and Frequency 2GHz, and 50% Duty Cycle , in your Path have 20 buffers in Your design. What is MPW violation in this design?
9. What are the things have to do to fix the MPW violations? Why You are using the inverter pairs instead of Buffers.?
10. For Example you have file with Hold violations with Endpoint and respected slack for those endpoint, Write PrimeTIme Script for to grep the Endpoints and To get the Setup slack for those Endpoints , and then Print those Endpoints and With Respect to Setup Slack?

11. For Example in your design take one D Pins, (Endpoint). For That Endpoint you Got different Startpoints, For those startpoint you got the some SetupSlacks , write a scripts for Those paths have the only Negetive Setupslack, and the count the how many paths are violated?
12. For Example Your one Design is have 2GHz frequncy and second Design is 1GHz which is more Difficult to Met the timining.
13. For Example you design got Cleared all the timing vilations, but Still you some DRV vilations, Is that need to fix that timing DRVs or not? IF Yes why?
14. What are the SDC Constraints Please write it down? What is the main Constraint? After Writing the Create clock and Create Generate clock?
15. Did you get the any PTE-075 Errors? What it Mean by PTE-075 Error? How will fix those Errors?
16. For Exmple
    We have
    Create_clock -name CLK1 -period 10 -waveform {0 5}
    Creat_clock -name CLK2 -period 10 -waveform {2 7}
    Those two clocks are going to two flops in a path? What is the Where we check the setup And Hold Check?
17. What will Happened if you are not fixing the Hold Violations?
18. What is the difference between the -nowrst and -max paths?
19. For Example you did report timing like a
    Report_timing -delay_type min -max_paths 10 -nworst 10000 from this how many paths will report?
20. What it meant by PBA and GBA ? which on is better? Why we use PBA Exhaustive Mode in report_timing?
21. What are the Sanity Checks are done your full Chip timing?
22. What it meant by X-talk Violations How do you fix the X-talk Violations?
23. How to overcome the Dynamic Power Consumption?
24. Can you Please tell me about OCV Concepts.
25. For Example in POCV We have # buffers in a paths Each Cell have mean = 15 ps and Delay Variation = 12 ps what is the Over all Delay of the Path?
26. How many Scenarios in Your Design?
27. For example you have a setup path violations ? but that path in lower metal layer, we did all the techniques to overcome the setup violation, but still get the violation how do fix those set up viloation?
28. What is the Difference between the Set_fase_path and set_disable timing? Which one you prefer mostly?
29. What it meant by Tweaker tool? Why it needed?
30. Tell abut DMSA?
31. What are the Clock groups ? Why we need to define the Clock Groups in Our design? Like why we need to define the logically exclusive groups or those clocks are Physcially Excusive Groups?

32. How to verify these are real clocks and these are virtual clocks, how do differentiate the real clock and Virtual clock in constraint way?
33. Did You know about the Timing Budget Concept?
34. How to fix the Cross talk Violations? What it men by Shielding?
35. After extracting the SPEF file how you decide , the extracted spef is correct or not?
36. What it mean by clock pushing and pulling, which one you prefer most?
37. You have all positive skew margin for all path ? but in one perticular path you have huge clock latncy , is that necessary to reduce the that clock latency?
38. Is that cross talk effect in the physically exclusive clocks?
39. When you we using the mutli cylce paths.
40. How we write the ECOS?

AMD Questions:

1. Tell me about STA Flow?
2. Calculation on Cross Talk delay on launch and Capture Path?
3.