MEGHANA JAJAM

STA Engineer

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STA Engineer with 3+ years of experience in timing ECOs, timing analysis, and managing complex designs at advanced nodes. Proficient in Prime Time, TCL and UNIX. Seeking to contribute expertise to innovative semiconductor solutions.

SUMMARY

- 3+ years of experience as STA Engineer. Trained in PD as well.
- Worked on Full chip coverage and Full chip sign off.
- Experience in DRV, Noise, Timing & Annotation analysis on Prime Time.
- Have knowledge of Floor Planning, Power Planning, IR Drop Analysis, Place and Opt,CTS, Routing, Extraction and Signal Integrity.
- Experience in lower technology nodes such as TSMC 7nm, 28nm, 65nm, 90nm and able tohandle complex designs with multimillion gates.
- Good at debugging and analyzing critical paths beforehand and take care of those paths withappropriate design methodologies.
- Proficient in writing the timing ECO's.
- Executed the block from Netlist to GDSII and performed block-level sign-off checks.
- Knowledge in physical verification skills like DRC, LVS, ERC etc.
- Familiarity with TCL and UNIX work history.
- Have experience on Hyperscale and DMSA.

SKILLS

- Synthesis : GENUS
- Floorplan, Place & Route : INNOVUS
- Timing Analysis/SI : PRIME TIME / TEMPUS
- Physical Verification : CALIBRE (on Std. Cell Layouts)
- Scripting language : TCL

WORK EXPERIENCE

- Working as a STA Engineer at AMD Xilinx from April 2021.

EDUCATION

- Pursued B. Tech in ECE from Anurag Group of Institutions in 2019 with 9.2 CGPA.
- Pursued Intermediate from CRS Junior College in 2015 with an aggregate of 97.5%.
- Completed SSC from Haliya Public School, Haliya 2013 with 9.5 CGPA.

PROJECTS

Project #1:

Project Name	:	KSB
Full chip Name	:	HNICX_MSOC
Node	:	7nm
Instance Count	:	42M
No. of Clocks	:	1287
Frequency	:	1.04 GHz
Tools	:	Prime Time

Responsibilities:

- Performed DRV, Timing, Noise & Annotation (Both Full & Partial) analysis at Full Chip level.
- Linking the design and checking Full & Partial Annotation for complete MSoC. The design is mixed with analog as well as digital blocks, due to this complexity, I have seen more annotation issues (PARA-124, PARA-004, PARA-006).
- Identified false timing arcs in timing .lib. Due to which there were false timing paths & false min clockpulse width violations.
- Timing violated for interface paths due to active aggressors in top level. Provided eco's to respectiveblock owners.
- Correlation between MSOC and Block level time.

Project #2:

Project Name	:	Everest
Full chip Name	:	HMID Full chip
Node	:	7nm
Instance Count	:	6.6M
No. of Clocks	:	1068
Frequency	:	300 MHz
Tools	:	Prime Time

Responsibilities:

- Linking the design in Full chip level and identify the interface timing paths.
- Checking Global clocks distribution at full chip level and making sure that the clocks go to all the respected blocks/cores without any breaking.
- Sanity checks on the Timing Logs and reports.
- Defining Interface & Internal path groups at full chip level.
- Worked on DRV and Min Pulse Width violations.
- Worked on Black Box analysis on few cores as part of full chip coverage.

Project #3:

Project Name	:	Everest
Full chip Name	:	HBM2E
Node	:	7nm
Tools	:	Prime Time

Responsibilities:

- Linking the design and checking Full & Partial Annotation for complete MSoC. The design is mixed with analog as well as digital blocks, due to this complexity, I have seen more annotation issues (PARA-124, PARA-004, PARA-006).
- Sanity checks on the Timing Logs and reports.
- Worked on DRV and Min Pulse Width violations.
- Validated Library correctness (gtm_octal_core) for Full Chip Timing.
- Performed Constraint validation - Linting & Equivalency checks at Full Chip Level.

Project #4:

Project Name	:	Everest
Full chip Name	:	SV60
Node	:	7nm
Tools	:	Prime Time

Responsibilities:

- Linking the design and checking Full & Partial Annotation for complete Full chip.
- Performed an In-depth analysis on STA log files.
- Performed DRV, Timing, Noise & Annotation (Both Full & Partial) analysis at Full Chip level.
- Validated Library correctness (gtm_octal_core) for Full Chip Timing.
- Provided Budgets for Interface timing paths at Full Chip Level, for NOC to NPI and vice versa.
- Performed Constraint validation - Linting & Equivalency checks at Full Chip Level.

DECLARATION

I hereby declare the above provided details are correct to the best of my knowledge.

Meghana Jajam

Place: Hyderabad