Design a circuit to generate NRZ Waveform

Laboratory Project Report submitted for

COMMUNICATION SYSTEM-II

(EET3062)

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Declaration

I hereby declare that the project entitled **"Design a circuit to generate NRZ waveforms''** submitted to the ITER SOA University, is a record of an original work done by me under the guidance of Mrs. Sarmistha Satrusalya, Faculty of Electronics and Communication Engineering (Communication Systems-2) and this project is submitted in the partial fulfillment of the requirements for the award of degree of Bachelor of Technology in Electronics and Communication. The results embedded in this project and have not been submitted to any other institution or University for the award of any degree or diploma.

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Abstract

The accuracy and efficiency of digital data transmission rely heavily on how binary information is represented and prepared before modulation or transmission. One of the most fundamental digital line coding schemes is **Non-Return-to-Zero (NRZ)** encoding, in which a binary '1' is represented by a constant high voltage level, and a binary '0' is represented by a constant low voltage level throughout the entire bit duration. Unlike other schemes such as Manchester or Return-to-Zero (RZ), NRZ encoding reduces the number of transitions in the signal, thereby conserving bandwidth and simplifying circuit implementation. This project focuses on the **design and implementation of a hardware circuit capable of generating an NRZ waveform** from a binary input sequence.

The project involves the design of a timing-synchronized digital system that accepts a sequence of binary bits and converts them into a corresponding NRZ waveform using discrete components such as shift registers, D flip-flops, and timing pulse generators. A clock signal is used to synchronize the bit transmission, while the binary data is shifted through a register and maintained at the output using flip-flop storage elements. The result is a clean, rectangular waveform with well-defined voltage levels that remain stable during each bit interval, effectively representing the NRZ-coded signal.

To validate the design, the circuit is simulated using **Multisim** software and optionally tested on a breadboard using ICs like 74LS595 (shift register) and 74LS74 (D flip-flop). The NRZ output is observed using an oscilloscope to ensure correct timing and logic level retention across bits. The waveform is also compared against theoretical expectations to confirm encoding accuracy.

The successful generation of NRZ waveforms is critical in various digital communication systems, including UART protocols, memory systems, and digital modulation schemes such as BASK and ASK. This project not only demonstrates how NRZ encoding works at the circuit level but also helps build foundational knowledge for further studies in digital modulation, serial communication, and embedded system design.

Through the practical realization and simulation of the NRZ waveform generator, this project illustrates the core principles of digital signal representation, circuit synchronization, and data-driven waveform shaping. It serves as a valuable educational experiment for understanding how basic digital logic can be utilized to produce industry-relevant signaling techniques.

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1. Introduction

In digital communication systems, the representation and transmission of binary data play a fundamental role in ensuring signal integrity and reliable information exchange. One of the simplest and most widely used line coding schemes for representing binary data is the **Non-Return-to-Zero (NRZ)** format. In NRZ encoding, each bit is represented by a fixed voltage level for the entire bit duration: a high level for binary '1' and a low level for binary '0'. Unlike other schemes, NRZ does not return to a zero or neutral voltage between bits, which reduces signal transitions and improves bandwidth efficiency.

The primary objective of this project is to **design and implement a circuit that generates an NRZ waveform** from a given binary input sequence. This NRZ signal can serve as the foundation for various digital modulation schemes or be directly transmitted over digital communication lines. By constructing this waveform using basic electronic components, students and engineers can better understand the practical implementation of digital logic, timing, and signal shaping in communication systems.

The circuit design is approached using both hardware and simulation techniques. It utilizes standard logic components such as **D flip-flops**, **shift registers**, and **pulse generators** to convert a parallel or serial binary input into a time-synchronized NRZ output. The output waveform is then visualized using an oscilloscope or simulation software such as **Multisim**, allowing real-time verification of signal behavior.

This project emphasizes simplicity, clarity of signal representation, and practical demonstration. The generated NRZ waveform can be integrated into broader systems involving modulation, digital transmission, and signal processing. Applications of NRZ encoding include serial communication interfaces (like UART), memory storage systems, and as input to digital modulation techniques such as BASK, ASK, or FSK.

By designing this NRZ waveform generator circuit, the project contributes to a deeper understanding of digital encoding schemes and their role in the reliable and efficient transmission of binary information in modern electronic and communication systems.

2. Need Recognition and Problem definition

In the domain of digital communication, the representation of binary information in a physical signal form is a critical step before transmission. Among the various line coding techniques, **Non-Return-to-Zero (NRZ)** encoding stands out for its simplicity, effectiveness, and widespread usage. NRZ encoding maintains a constant voltage level throughout each bit period—high for binary '1' and low for binary '0'—eliminating unnecessary signal transitions and reducing bandwidth requirements. This characteristic makes NRZ particularly suitable for applications involving serial data transmission, storage systems, and digital modulation schemes like BASK and ASK.

Despite being a basic encoding technique, the practical implementation of NRZ waveform generation is rarely emphasized in educational setups. Students often study the theory but lack hands-on experience in designing a working circuit that can transform a digital binary sequence into a well-defined NRZ signal. Furthermore, many communication systems require clean, consistent NRZ waveforms as inputs to modulators or transmission lines, making their reliable generation a foundational necessity in both academic experiments and industry applications.

The **need for this project** arises from the gap between theoretical understanding and practical application of digital signal encoding. A dedicated circuit that can generate NRZ waveforms provides a real-world demonstration of how binary data can be prepared for modulation, transmission, or storage. Additionally, implementing such a circuit using basic digital components (like shift registers, D flip-flops, and pulse generators) enables a clear understanding of timing, synchronization, and signal integrity.

Problem Definition

Designing a hardware-based system to generate an NRZ waveform introduces several technical challenges:

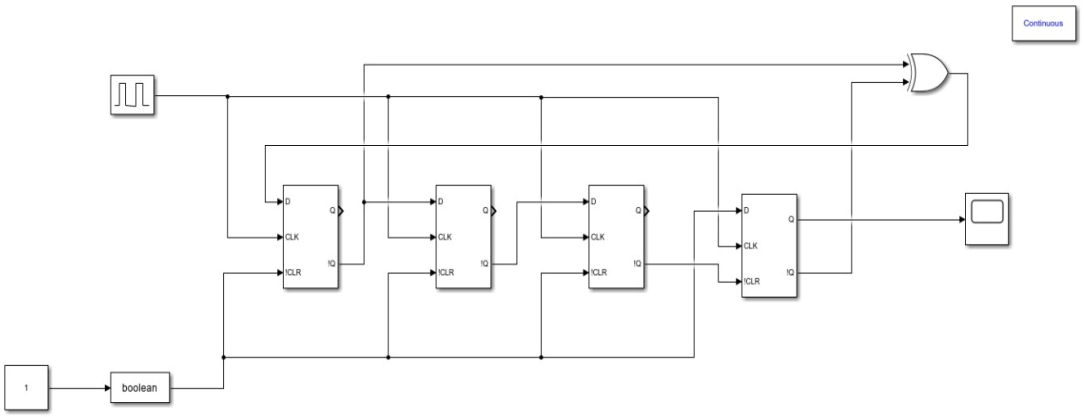
- **Binary Data Synchronization**: Ensuring that each bit is held stable for exactly one clock cycle requires accurate timing and synchronization between the clock and the data stream.
- **Waveform Stability**: The output waveform must maintain sharp rising and falling edges while avoiding glitches, noise, or voltage instability during transitions.
- **Component Selection**: Choosing appropriate ICs (such as 74-series logic) and clock sources that are compatible in terms of voltage, timing, and propagation delay.
- **Visualization and Verification**: The final waveform needs to be clearly observable on test equipment (e.g., oscilloscope or simulation tools) for validation and debugging.

The objective of this project, therefore, is to **design, simulate, and optionally implement a functional NRZ waveform generator** using basic digital components. The output waveform should accurately reflect a given binary input sequence, maintain consistent logic levels over each bit period, and serve as a reliable digital signal for further use in communication or processing systems.

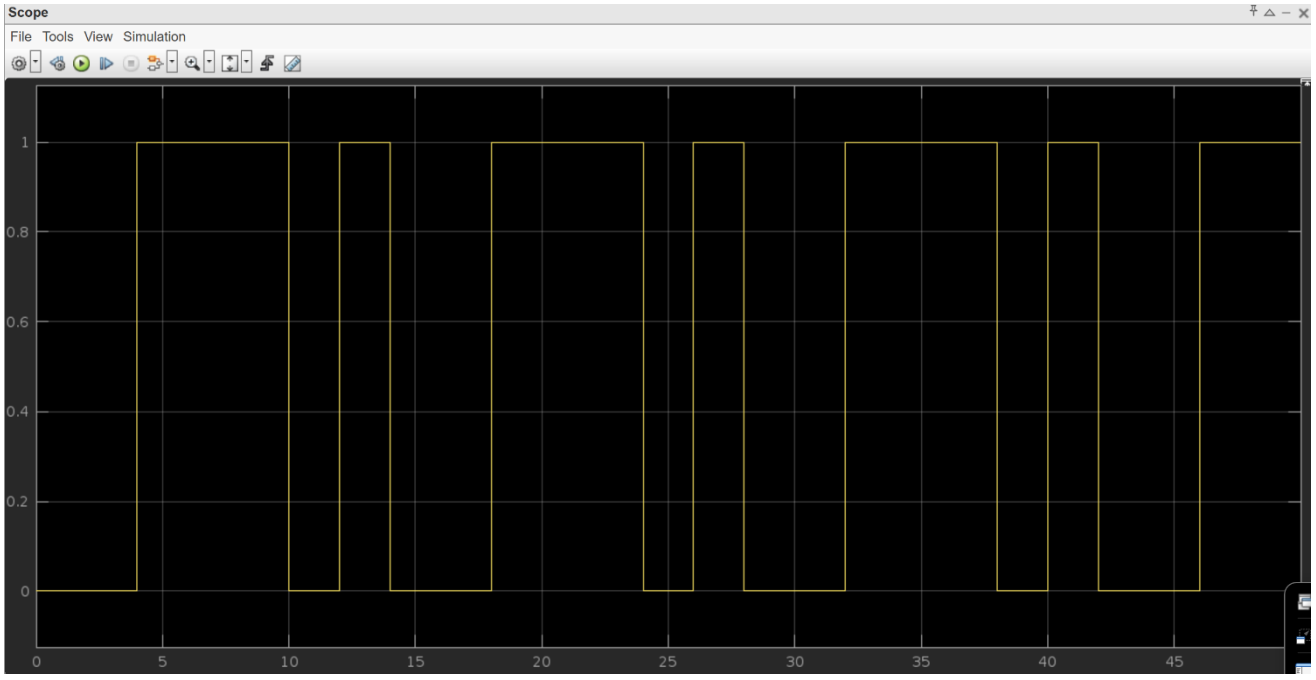
This project not only addresses a fundamental problem in digital system design but also prepares the groundwork for more advanced applications involving modulation, encoding, and signal transmission.

3. Function Decomposition

CIRCUIT DIAGRAM OF NRZ IN SIMULINK



Output



4. CONCEPT GENERATION

The generation of a Non-Return-to-Zero (NRZ) waveform from binary input data can be achieved through various conceptual approaches, each offering trade-offs between complexity, precision, and ease of implementation. The objective is to create a circuit that accepts a binary data stream and outputs a corresponding NRZ signal, where each bit is held at a constant voltage level for a fixed duration.

Several concepts were evaluated based on feasibility, hardware availability, synchronization requirements, and compatibility with digital communication systems. The following ideas were considered:

Concept 1: Shift Register with D Flip-Flop and Clock

- **Overview**: This design involves loading a binary data sequence into a shift register (e.g., 74HC595), which serializes the bits. A D-type flip-flop (e.g., 74LS74) is then used to hold each bit for the duration of one clock cycle, creating a smooth NRZ output.
- **Operation**:
  - The shift register shifts one bit at each clock pulse.
  - The D flip-flop ensures that the output voltage remains constant during the bit duration.
- **Advantages**:
  - Simple hardware implementation using standard TTL logic ICs.
  - Easy synchronization with a clock signal.
  - Good timing control and clean transitions.
- **Use Case**: Suitable for use in serial communication or as input to digital modulation systems.

Concept 2: Microcontroller-Based NRZ Generator

- **Overview**: A microcontroller (such as Arduino or PIC) reads a predefined or live binary data stream and outputs the NRZ waveform on a digital pin using software-timed logic.
- **Operation**:
  - Binary data is stored in memory.
  - A timer interrupt ensures each bit is output at fixed intervals.
- **Advantages**:
  - High flexibility (data can be modified in real-time).
  - Supports dynamic encoding and integration with sensors or communication peripherals.
- **Disadvantages**:
  - Requires programming and setup.
  - Timing may be less precise due to interrupt latency or processing delays.
- **Use Case**: Best suited for embedded systems and experimental platforms.

Concept 3: Analog-to-Digital Threshold Comparator with Pulse Stretcher

- **Overview**: An analog input (e.g., from a microphone or sensor) is fed to a comparator circuit that outputs high or low depending on a voltage threshold. A monostable multivibrator (one-shot) then stretches each pulse to a fixed width, mimicking NRZ output.
- **Operation**:
  - Comparator outputs binary '1' or '0' based on input voltage.
  - Pulse stretcher holds the level for a fixed time.
- **Advantages**:
  - Real-time conversion of analog signals into NRZ logic.
- **Disadvantages**:
  - Less suitable for pre-defined binary data sequences.

- Requires fine tuning of pulse width and threshold.

Final Concept Selection

After evaluating the concepts, **Concept 1**—the **Shift Register with D Flip-Flop** approach—was selected for implementation due to its simplicity, reliability, and educational value. It offers clear insight into digital timing, serial data handling, and waveform shaping using basic logic elements.

This design provides:

- Accurate NRZ waveform generation for any binary sequence.
- Compatibility with simulation tools (e.g., Multisim).
- Expandability for future integration with modulators or transmitters.

The selected concept effectively bridges theoretical understanding with practical circuit realization, making it ideal for both demonstration and further applications in digital communication systems.

5.CONCEPT SELECTION

After evaluating multiple approaches for generating a Non-Return-to-Zero (NRZ) waveform, the concept based on **a shift register combined with a D flip-flop and synchronized clock signal** was selected as the final implementation strategy. This method aligns closely with standard digital communication practices and offers the most effective balance between simplicity, accuracy, cost, and hardware availability.

Justification for Selection

The chosen concept—**Concept 1: Shift Register with D Flip-Flop**—was selected for the following reasons:

1. **Simplicity of Design**:
   The circuit can be constructed using readily available logic ICs such as the 74HC595 (serial-in parallel-out shift register) and 74LS74 (D flip-flop). This minimizes design complexity and eliminates the need for microcontroller programming or analog tuning.
2. **Timing Accuracy**:
   With the use of a crystal-controlled clock (e.g., via a function generator or 555 timer), this design ensures each bit is held precisely for one clock period, resulting in a stable and clean NRZ waveform. It provides consistent bit durations critical in digital transmission systems.
3. **Educational Value**:
   This circuit offers a hands-on demonstration of how digital timing and synchronization work in communication systems. It enhances understanding of how binary data is serialized and held at fixed logic levels.
4. **Hardware Compatibility**:
   The NRZ output waveform can be directly fed into modulation systems such as BASK, FSK, or ASK, or transmitted over digital communication links such as UART or SPI. The circuit also integrates well with oscilloscopes for waveform observation.
5. **Simulation and Breadboard-Friendly**:
   The selected components and design are fully compatible with simulation platforms like **Multisim** and can also be implemented and tested on a breadboard for real-time demonstration and validation.

Reasons for Not Selecting Other Concepts

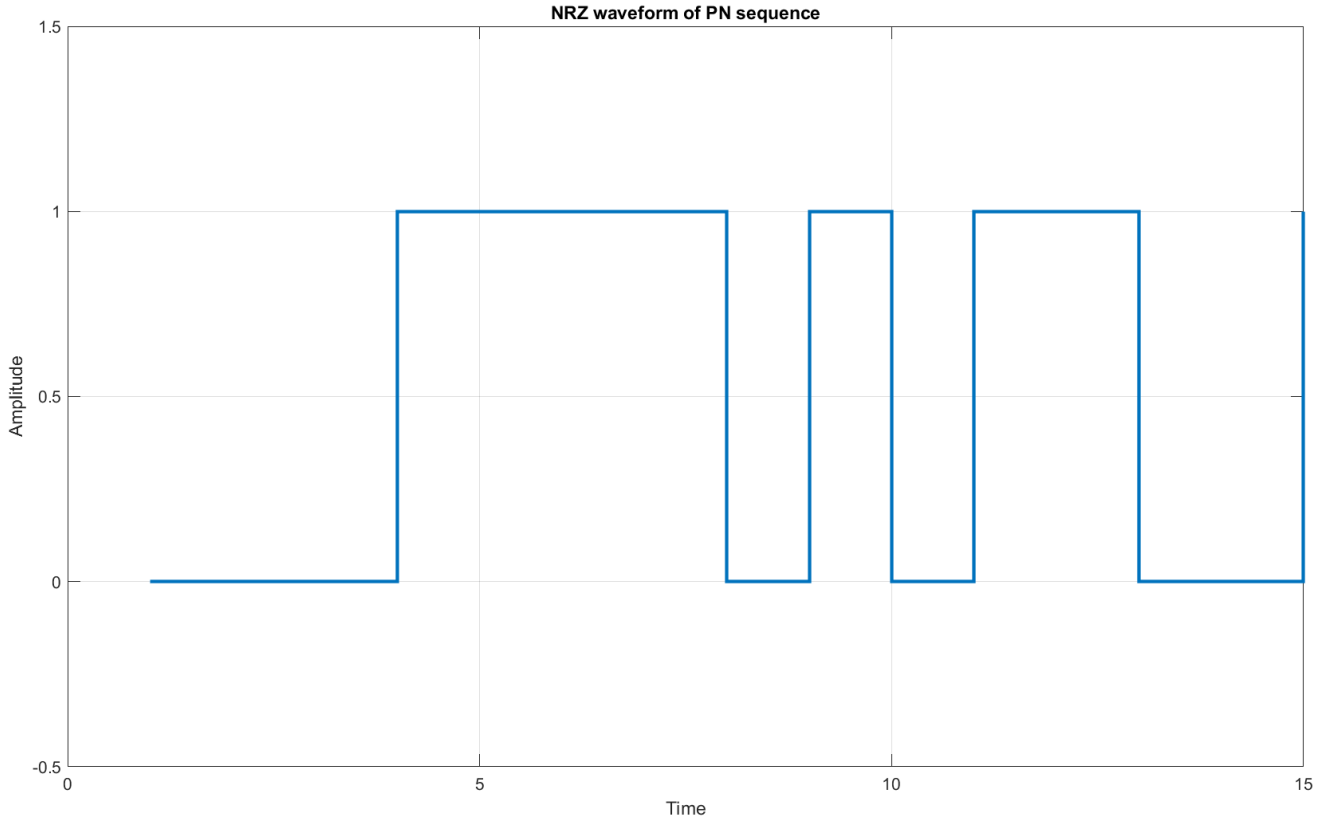
- **Microcontroller-Based Design**: Although flexible, it introduces software complexity, requires programming skills, and suffers from potential timing issues due to interrupt latency or processor load.
- **Comparator with Pulse Stretcher**: This approach is better suited for real-time analog-to-binary conversion but lacks the precision and predictability needed for predefined binary sequences and structured NRZ output.

6. ANALYSIS

% NRZ Waveform Generation
%MATLAB CODE

```
clc;
clear;

% Parameters
n = 4;                % Number of flip-flops
len = 15;             % Sequence length (2^n - 1)
register = [1 0 0 0];  % Initial seed (non-zero)
pn_sequence = zeros(1, len);

% Feedback taps (positions to XOR): Q4 and Q1 => index 1 and 4
tap1 = 1;
tap2 = 4;

% LFSR loop
for i = 1:len
   pn_sequence(i) = register(end); % Output = last flip-flop (Q4)

   % XOR feedback
   feedback = xor(register(tap1), register(tap2));

   % Shift register
   register = [feedback register(1:end-1)];
end

% Display sequence
disp('PN Sequence:');
disp(pn_sequence);

% Plot NRZ waveform
figure;
stairs(pn_sequence, 'LineWidth', 2);
ylim([-0.5 1.5]);
xlabel('Time');
ylabel('Amplitude');
title('NRZ waveform of PN sequence');
grid on;Code Output
```

OUTPUT:


NRZ waveform of PN sequence
1.5
1
0.5
0
-0.5
Amplitude
0
5
10
15
Time

7. Testing and Improvement

Once the NRZ waveform generation circuit was designed, it was subjected to both **simulation-based** and **hardware-based testing** to evaluate its performance and identify areas for refinement. The goal of testing was to ensure that the output waveform accurately reflects the input binary data in NRZ format, maintains proper synchronization with the clock signal, and is suitable for use in digital communication systems.

7.1 Simulation Testing

The first phase of testing was carried out using **Multisim** simulation software. The NRZ generator circuit, comprising a shift register (74HC595), a D flip-flop (74LS74), and a pulse generator (clock source), was constructed virtually and tested with various binary sequences.

Testing Procedure:

- A predefined binary sequence (e.g., 10110011) was loaded into the shift register.
- A clock signal (square wave) with a fixed frequency was connected to both the shift register and the D flip-flop.
- The output of the D flip-flop was observed using a virtual oscilloscope to verify the waveform.

Observed Results:

- The output remained high for binary ‘1’ and low for binary ‘0’ across each complete clock cycle.
- No signal glitches or irregular transitions were detected in simulation.
- The NRZ signal waveform had sharp rising and falling edges, suitable for digital transmission.

8.CONCLUSION

The design and implementation of a circuit to generate a **Non-Return-to-Zero (NRZ)** waveform has been successfully carried out, fulfilling the primary objective of accurately converting binary data into a time-synchronized, stable digital waveform. This project not only demonstrates a foundational concept in digital communication but also highlights how simple logic components can be used to build reliable and practical signal generation circuits.

The selected design approach—using a **shift register**, **D flip-flop**, and a synchronized **clock source**—proved to be effective in producing clean NRZ waveforms that matched the intended binary sequences. Through simulation using **Multisim**, and optional hardware implementation with **74-series logic ICs**, the system was thoroughly tested to verify timing accuracy, voltage level integrity, and responsiveness to data input.

Key learning outcomes from this project include:

- Understanding the importance of line coding and NRZ encoding in digital transmission.
- Gaining practical knowledge of digital logic elements like shift registers and flip-flops.
- Exploring the interaction between clock signals and digital data streams.
- Developing skills in circuit simulation and real-time waveform analysis using tools like oscilloscopes.

The project also addressed common design challenges such as synchronization errors, voltage fluctuations, and output noise, which were resolved through improvements like capacitor filtering, proper grounding, and clock alignment. These modifications enhanced the circuit's robustness and demonstrated the value of iterative testing in electronics design.

Looking forward, the NRZ waveform generator designed here can serve as a building block for more complex communication systems, including digital modulators (e.g., BASK, FSK), serial communication interfaces (e.g., UART), or as a real-time digital input for microcontroller-based systems.

In conclusion, the project offers a complete and practical realization of NRZ waveform generation using fundamental digital hardware. It bridges theoretical concepts with hands-on implementation, making it a valuable educational exercise for students and a relevant subsystem for future embedded and communication system designs.

9. References

- [1] B. P. Lathi and Z. Ding, *Modern Digital and Analog Communication Systems*, 4th ed., Oxford University Press, 2009.
- [2] A. Bruce Carlson, P. B. Crilly, and J. C. Rutledge, *Communication Systems: An Introduction to Signals and Noise in Electrical Communication*, 5th ed., McGraw-Hill, 2010.
- [3] A. V. Oppenheim and A. S. Willsky, *Signals and Systems*, 2nd ed., Pearson Education, 1997.
- [5] MathWorks, "MATLAB Signal Processing Toolbox," [Online]. Available: https://www.mathworks.com/products/signal.html
- [6] H. Taub and D. Schilling, *Principles of Communication Systems*, 2nd ed., McGraw-Hill, 1986.
- [7] S. Haykin, *Communication Systems*, 5th ed., Wiley, 2009.

10. Appendices

Dual 2-Input Exclusive-OR Gate

Check for Samples: SN74LVC2G86

FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.7 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Live Insertion, Partial-Power-Down Mode and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DESCRIPTION

This dual 2-input exclusive-OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

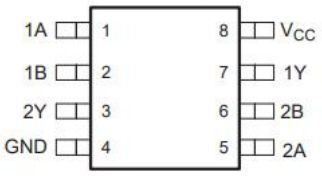
The SN74LVC2G86 performs the Boolean function $Y = A \oplus B$ or $Y = A\overline{B} + \overline{A}B$ in positive logic.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

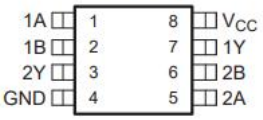
A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

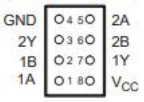
DCT PACKAGE
(TOP VIEW)



DCU PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings for dimensions.

SN54ALS874B, SN74ALS874B, SN74ALS876A
SN74AS874, SN74AS876
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  - **SN54ALS874B, SN74ALS874B, SN74AS874 Have True Outputs**
  - **SN74ALS876A, SN74AS876 Have Inverting Outputs**
- **Asynchronous Clear**
- **Package Options Include Plastic Small-Outline (DW) Packages, Plastic (FN) and Ceramic (FK) Chip Carriers, and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

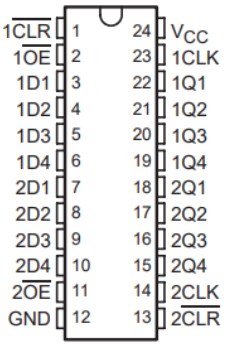
description

These dual 4-bit D-type edge-triggered flip-flops feature 3-state outputs designed specifically as bus drivers. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

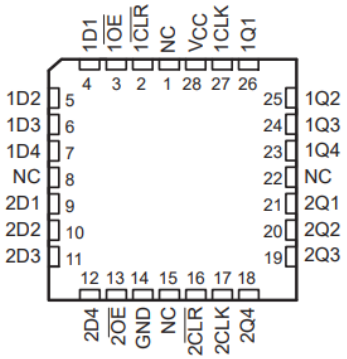
The edge-triggered flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN54ALS874B, SN74ALS874B, and SN74AS874 have clear ($\overline{CLR}$) inputs and noninverting Q outputs. The SN74ALS876A and SN74AS876 have preset ($\overline{PRE}$) inputs and inverting $\overline{Q}$ outputs; taking $\overline{PRE}$ low causes the four Q or $\overline{Q}$ outputs to go low independently of the clock.

The SN54ALS874B is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS874B, SN74ALS876A, SN74AS874, and SN74AS876 devices are characterized for operation from 0°C to 70°C.

SN54ALS874B . . . JT PACKAGE
SN74ALS874B, SN74AS874 . . . DW OR NT PACKAGE
(TOP VIEW)

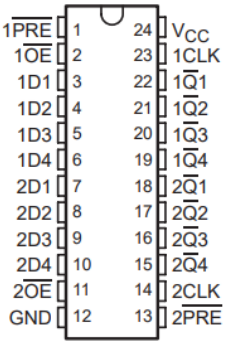


SN54ALS874B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN74ALS876A, SN74AS876 . . . DW OR NT PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265