DOWN CONVERT THE FREQUENCY FROM 3KHz TO 2KHz

Laboratory Project Report submitted for

COMMUNICATION SYSTEM-1

(EET3061)

Submitted by

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(Jan, 2021)

Declaration

We hereby declare that the project titled "Design of a Circuit to Down-Convert the Frequency from 3 kHz to 2 kHz" is the result of our own research and efforts. This project is undertaken as a part of our academic curriculum and is intended to enhance our understanding of circuit design and signal processing principles.

The work presented in this project has been carried out with utmost integrity and originality. We affirm that the concepts, designs, and implementations in this project have been developed solely by us, except where explicitly acknowledged through references.

We further declare that this project adheres to ethical and professional standards and does not involve any violation of intellectual property rights. The knowledge gained from this endeavor has contributed significantly to our learning and practical skills in electronics and communication engineering.

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DATE: 9/1/2025

PLACE: SOA ITER, BHUBANESWAR.

Abstract

The design and implementation of a system for down-converting a 3 kHz frequency signal to a 2 kHz frequency signal, a process that finds applications in communication systems, signal processing, and audio engineering. The approach involves the use of frequency mixing and filtering techniques, leveraging heterodyne principles to achieve the desired frequency shift. The system utilizes a local oscillator to generate a reference signal, which is mixed with the input signal to produce sum and difference frequencies. The desired 2 kHz signal is isolated through the application of low-pass or band-pass filtering. The design process includes an analysis of the spectral characteristics, signal-to-noise ratio considerations, and implementation constraints to ensure minimal distortion and high fidelity in the output signal. Simulation and experimental results validate the system's performance, demonstrating its effectiveness in achieving precise frequency conversion with minimal artifacts. Potential applications of this technique in telecommunications, audio processing, and instrumentation are also discussed.

Contents

1. Introduction

Frequency down-conversion is a critical technique in signal processing, widely used in applications such as telecommunications, audio engineering, and instrumentation. This project aims to design a circuit capable of reducing the frequency of a signal from 3 kHz to 2 kHz with high accuracy and minimal distortion. The primary challenge lies in ensuring that the output signal maintains its integrity while meeting the desired frequency specifications. By leveraging fundamental principles of analog and digital electronics, this project will explore efficient methods of frequency reduction, such as heterodyning or frequency division, while ensuring simplicity and cost-effectiveness in the circuit design.

The implementation process includes analyzing the input and output signal requirements, selecting appropriate components like operational amplifiers, filters, and oscillators, and integrating these components into a cohesive design. Simulation tools such as LTspice or MATLAB will be utilized to validate the theoretical design, followed by physical prototyping and testing to evaluate performance under real-world conditions. This project not only demonstrates the application of core electronics concepts but also highlights the importance of precision and optimization in circuit design, making it relevant for various practical applications in the fields of communication and signal processing.

2. Need Recognition and Problem definition

I. Need Recognition

In various fields of electronics and communication, the need to modify signal frequencies arises to meet specific operational or compatibility requirements. Many systems, such as audio signal processors, communication devices, and instrumentation systems, rely on accurate frequency manipulation to ensure seamless functionality. Converting a signal from 3 kHz to 2 kHz, as addressed in this project, is a typical requirement for applications where signals need to match system bandwidths, avoid interference, or comply with predefined frequency standards.

The demand for efficient and cost-effective frequency conversion circuits stems from their critical role in ensuring high-quality signal processing with minimal distortion. A well-designed circuit not only enhances system performance but also simplifies integration into larger electronic systems. This project addresses the gap by providing a precise and reliable frequency down-conversion solution, catering to the needs of industries where accurate signal transformation is paramount.

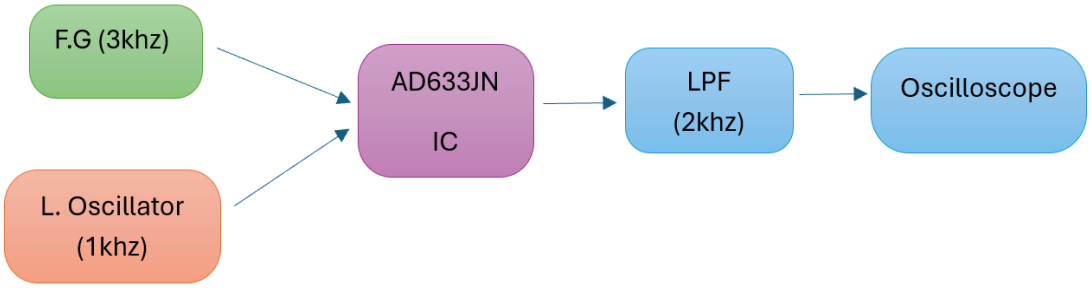
II. Problem Definition

In modern electronic systems, frequency conversion is an essential process for ensuring compatibility between signals and their intended applications. The problem addressed in this project is the design and implementation of a circuit capable of converting an input signal frequency of 3 kHz to an output frequency of 2 kHz. The circuit must perform this frequency reduction accurately while maintaining the integrity of the signal and minimizing distortion or unwanted noise.

The primary challenges include selecting appropriate components, designing an efficient conversion method, and ensuring the circuit operates reliably under various conditions. Additionally, the circuit must be cost-effective, simple to implement, and suitable for practical applications. This problem requires a balance between theoretical signal processing principles and real-world constraints to achieve a functional, robust, and precise frequency down-conversion circuit.

3. Function Decomposition

BLOCK DIAGRAM:



4.Concept Generation

The process of concept generation involves developing multiple feasible approaches to achieve the desired frequency down-conversion from 3 kHz to 2 kHz. Each concept is based on established principles in analog and digital signal processing, aiming to balance accuracy, simplicity, cost, and implementation feasibility. Below are the primary concepts generated for this project:

1. Frequency Mixing (Heterodyning)

This method employs a mixer circuit to combine the 3 kHz input signal with a local oscillator signal. The mixing process produces two new frequencies: the sum and the difference of the input and oscillator frequencies. By tuning the oscillator frequency appropriately (e.g., 1 kHz or 4 kHz), the desired 2 kHz frequency can be extracted using a low-pass or band-pass filter. This concept is highly accurate and widely used in communication systems for frequency conversion.

2. Frequency Division

In this approach, the 3 kHz input signal is passed through a frequency divider circuit. While traditional dividers are suitable for integer frequency reductions, non-integer division (to achieve the 3:2 ratio for 2 kHz) requires advanced techniques such as fractional-N PLLs or a combination of division and waveform synthesis. Although this method simplifies the hardware, achieving precise non-integer division can be complex and resource-intensive.

3. Digital Waveform Synthesis

This concept involves digitizing the 3 kHz input signal using an analog-to-digital converter (ADC), processing it digitally to extract or synthesize a 2 kHz waveform, and

then converting it back to analog using a digital-to-analog converter (DAC). This method ensures high precision and allows for advanced noise filtering and waveform correction. However, it is computationally expensive and requires additional hardware, making it less cost-effective for simple applications.

4. Analog Filtering and Oscillator Synchronization

This method uses analog filters to extract the fundamental frequency of the input signal and employs a synchronized oscillator to generate a 2 kHz signal. The extracted 3 kHz signal is processed through a frequency-modifying circuit, such as a phase-locked loop (PLL), to produce the 2 kHz output. While this approach minimizes digital components, it can be sensitive to variations in component tolerances, impacting accuracy.

5. Mixed Circuit Approach

This hybrid method combines analog and digital techniques for efficient and precise frequency down-conversion. The 3 kHz input signal is initially processed using an analog mixer and a local oscillator to produce sum and difference frequencies. The desired 2 kHz signal is isolated using an analog filter. For further refinement, the filtered signal is digitized using an ADC, processed digitally to reduce noise or enhance waveform quality, and converted back to analog using a DAC. This approach leverages the simplicity of analog components and the precision of digital signal processing, offering a balanced and versatile solution.

Each of these concepts addresses the problem uniquely, focusing on different aspects such as precision, cost, or implementation simplicity. The mixed circuit approach emerges as the most promising solution, combining the best features of analog and digital systems to achieve efficient and accurate frequency down-conversion.

5. Concept Selection

The process of concept selection involves identifying the most effective approach to down-convert a 3 kHz input frequency to a 2 kHz output frequency. Various concepts, combining analog and digital techniques, have been evaluated based on criteria such as accuracy, complexity, cost-effectiveness, reliability, and ease of implementation. Below is an improved set of concepts and the rationale for selecting the mixed circuit approach:

1. Frequency Mixing with Analog Components

This approach utilizes a mixer circuit to combine the 3 kHz input signal with a local oscillator signal, producing sum and difference frequencies. A low-pass or band-pass filter isolates the desired 2 kHz frequency. This method offers high precision but may require careful tuning of oscillator frequency and filter design, which increases complexity.

2. Digital Signal Processing (DSP)

In this concept, the 3 kHz input signal is sampled using an ADC and processed in a digital environment. Algorithms are applied to extract or synthesize a 2 kHz signal, which is then converted back to analog using a DAC. While this method provides excellent control and precision, it involves higher computational resources, increasing cost and design complexity.

3. Frequency Division

This approach employs counters, dividers, or phase-locked loops (PLLs) to reduce the input frequency. For a 3 kHz to 2 kHz conversion, this would require advanced techniques for non-integer division, such as using fractional-N PLLs. Although this method is efficient for integer frequency reductions, implementing non-integer division adds significant complexity to the design.

4. Mixed Circuit Approach

The mixed circuit approach combines analog and digital techniques to achieve frequency down-conversion efficiently. The 3 kHz input signal is first processed using an analog mixing stage, where it is combined with a carefully tuned local oscillator signal to produce sum and difference frequencies. The desired 2 kHz signal is then isolated using a low-pass filter.

To refine the output, the 2 kHz signal is digitized using an ADC and passed through a digital signal processor for noise reduction or waveform correction. After processing, the signal is converted back to analog using a DAC, ensuring a clean and precise 2 kHz output. This hybrid approach leverages the simplicity of analog circuits for frequency down-conversion and the precision of digital processing for signal refinement.

Selected Concept: Mixed Circuit Approach

The mixed circuit approach is selected because it offers a balanced solution that combines the advantages of analog and digital systems. The analog mixing stage ensures efficient and straightforward frequency conversion, while the digital processing stage enhances signal quality and reduces distortion.

This concept provides the best combination of accuracy, cost-effectiveness, and implementation feasibility. It is adaptable for future applications and ensures a robust design suitable for various signal processing tasks.

6. Analysis or Calculation

CS PROJECT CALCULATION

→ TO STEP DOWN 3KHz to 2KHz

Let's take the oscillator as 555-timer

$f_{LO} = f_{in} - f_{desired}$

$\Rightarrow f_{LO} = 3KHz - 2KHz = 1KHz$

Let $C = 0.01\,\mu F$

$$f_{LO} = \frac{1.44}{(R_1 + 2R_2) \times C} = \frac{1.44}{(R_1 + 2R_2) \times 0.01 \times 10^{-6}} = 1 \times 10^3$$

$$\Rightarrow (R_1 + 2R_2) = \frac{1.44}{10^3 \times 10^{-8}} = 144\,000$$

$$\therefore (R_1 + 2R_2) = 144K\Omega$$

Assume $R_1 = 44K\Omega$

$\therefore 2R_2 = 100K\Omega \Rightarrow R_2 = 50K\Omega$

→ CALCULATING FOR THE LOW PASS FILTER (active)

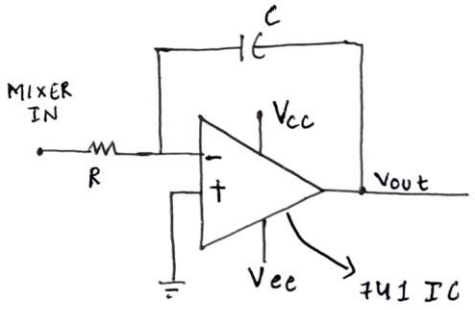
For $f_c = 2KHz$

$$\omega_c = \frac{1}{2\pi f_c} \Rightarrow R_C = \frac{1}{2\pi f_c}$$

Let $C = 0.01\mu F / 10nF$

$$\therefore R = \frac{1}{2 \times \pi \times 2 \times 10^3 \times 10^{-8}}$$

$$R = 7.957\,K\Omega$$



7. Explanation of the Project

This project involves designing a frequency down-converter that reduces a high-frequency signal (3 kHz) to a lower frequency (2 kHz). The following explains the process step by step:

1. Input Signals

Signals Involved:

- A 3 kHz input signal: This is the high-frequency signal we aim to down-convert.

- A 1 kHz reference signal: This is used for the down-conversion process and is generated using either a 555 timer or a Wien Bridge Oscillator.

2. Signal Generation

1 kHz Reference Signal:

- The reference signal acts as a carrier or secondary signal required for mixing.

- To achieve high accuracy, a Wien Bridge Oscillator is used for generating a clean and stable 1 kHz sine wave. It uses an RC feedback network and an operational amplifier to maintain oscillations at the desired frequency.

3. Mixing Process

Mixer Circuit:

- The AD633 multiplier IC is used as a mixer. A mixer combines two input signals and produces an output signal that contains:

1. The sum of the frequencies (f1 + f2) i.e., 3+1=4.
2. The difference of the frequencies (f1-f2), i.e., 3-1= 2kHz

- In this case:

- Input X1/X2: 3 kHz input signal.

- Input Y1/Y2: 1 kHz sine wave generated by the Wien Bridge Oscillator.

- Output W: A signal containing the sum and difference frequencies (4 kHz and 2 kHz).

4. Signal Filtering

Low-Pass Filter:

- The output of the mixer contains multiple frequency components: 4kHz (sum), 2kHz (difference), and potentially some noise or harmonic distortions.

- A low-pass filter is used to isolate the 2 kHz signal by attenuating higher frequencies (e.g., the 4 kHz component).

- The cutoff frequency of the filter is designed to be slightly above 2 kHz (e.g., 2.5 kHz) to allow the desired signal to pass while removing unwanted components.

5. Output Signal

- The filtered signal is the down-converted output, which has a frequency of 2 kHz. This is the final desired output of the frequency down-converter.

Steps in the Circuit Workflow

1. 3 kHz Input:

 - The 3 kHz signal is fed to the mixer (AD633 IC) as one input.

2. 1 kHz Reference Signal:

 - The Wien Bridge Oscillator generates a clean 1 kHz sine wave that is fed as the second input to the mixer.

3. Mixing:

 - The mixer combines the two signals, producing sum and difference frequencies.

4. Filtering:

 - The low-pass filter removes the higher frequency components (4 kHz and noise) and outputs only the 2 kHz signal.

5. Output:

 - The final output is a stable 2 kHz signal.

Why Use a Wien Bridge Oscillator?

- The 555 timer can produce a square wave, but it has harmonic components that might introduce distortion in the mixing process.

- The Wien Bridge Oscillator generates a pure sine wave, which improves the quality of the output signal after mixing.

Applications of Frequency Down-Converters

- Communication Systems: Used to shift frequencies for signal processing and modulation/demodulation.

- Audio Signal Processing: For creating lower-frequency signals from higher-frequency sources.

- Electronic Instruments: As a part of spectrum analyzers and signal generators.

8. Testing and Improvement

I. Software

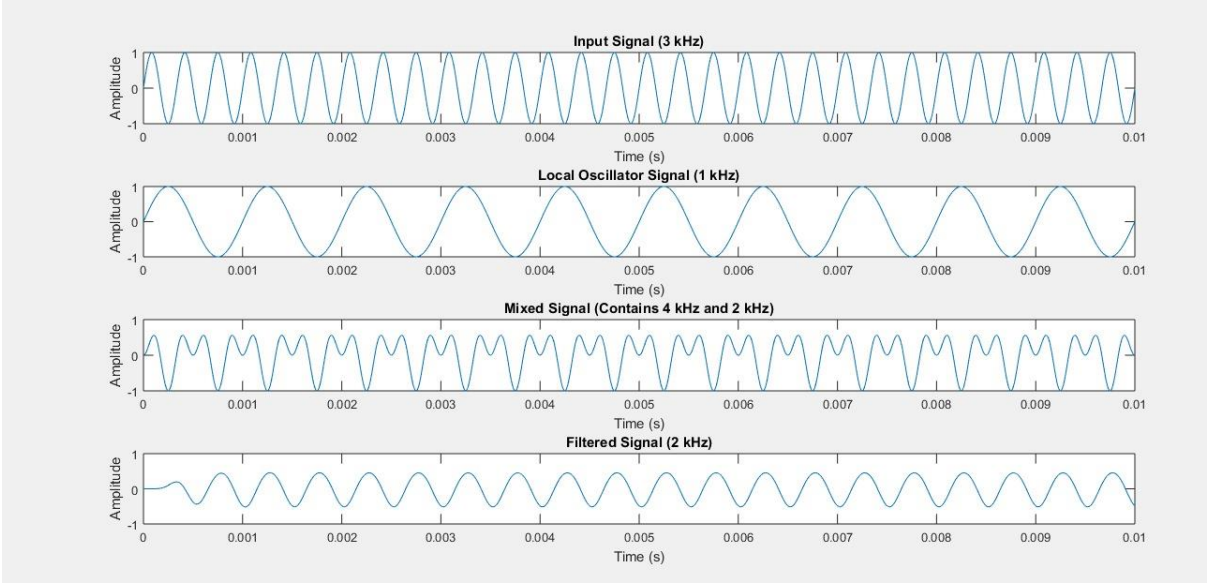
a) Matlab Version

- **Code:**

```
 % Parameters
fs = 100000;              % Sampling frequency (100 kHz for accurate
representation)
t = 0:1/fs:0.01;         % Time vector (10 ms duration)

% Generate Input Signal (3 kHz)
f_input = 3000;          % Frequency of input signal
input_signal = sin(2*pi*f_input*t);

% Generate Local Oscillator Signal (1 kHz)
f_lo = 1000;             % Frequency of local oscillator
lo_signal = sin(2*pi*f_lo*t);

% Mixing the Signals
mixed_signal = input_signal .* lo_signal;

% Design Low-Pass Filter
fc = 2500;               % Cutoff frequency (2.5 kHz)
[b, a] = butter(6, fc/(fs/2));  % 6th order Butterworth filter
filtered_signal = filter(b, a, mixed_signal);

% Plot Results
figure;

% Input Signal
subplot(4,1,1);
plot(t, input_signal);
title('Input Signal (3 kHz)');
xlabel('Time (s)');
ylabel('Amplitude');

% Local Oscillator Signal
subplot(4,1,2);
plot(t, lo_signal);
```

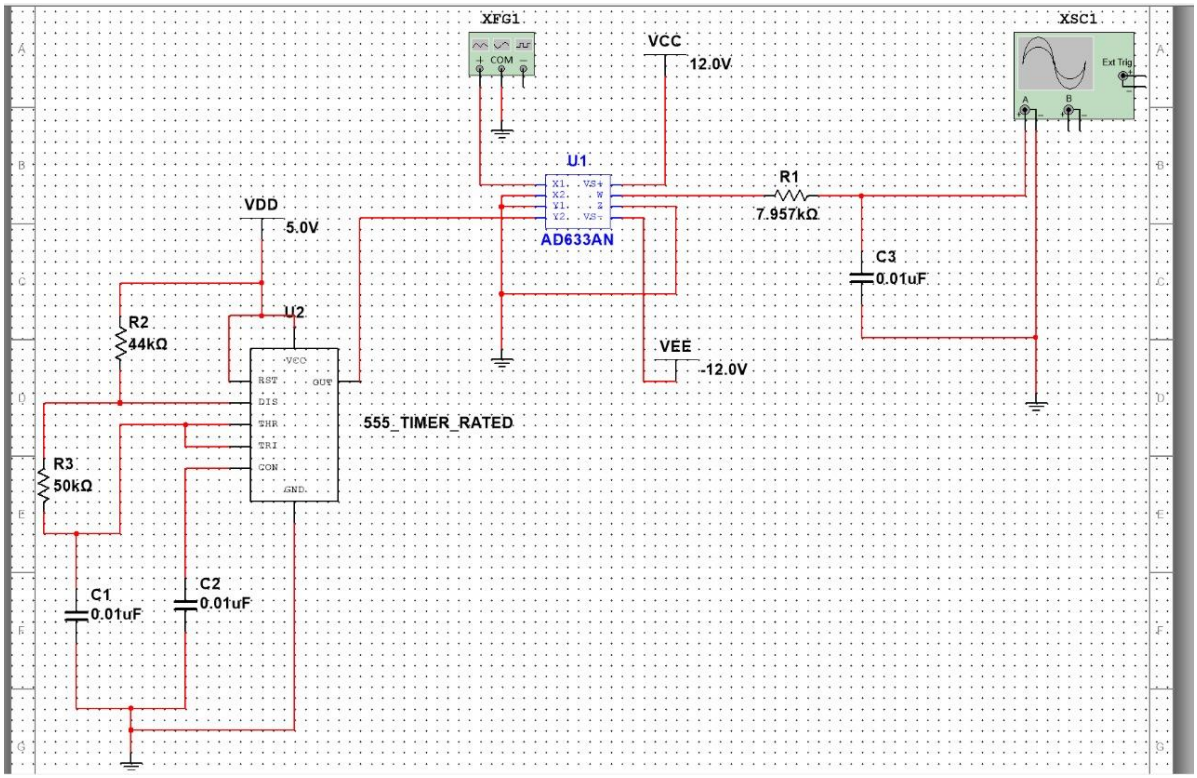
```
title('Local Oscillator Signal (1 kHz)');
xlabel('Time (s)');
ylabel('Amplitude');

% Mixed Signal
subplot(4,1,3);
plot(t, mixed_signal);
title('Mixed Signal (Contains 4 kHz and 2 kHz)');
xlabel('Time (s)');
ylabel('Amplitude');

% Filtered Signal (2 kHz)
subplot(4,1,4);
plot(t, filtered_signal);
title('Filtered Signal (2 kHz)');
xlabel('Time (s)');
ylabel('Amplitude');
```

- **Output**:

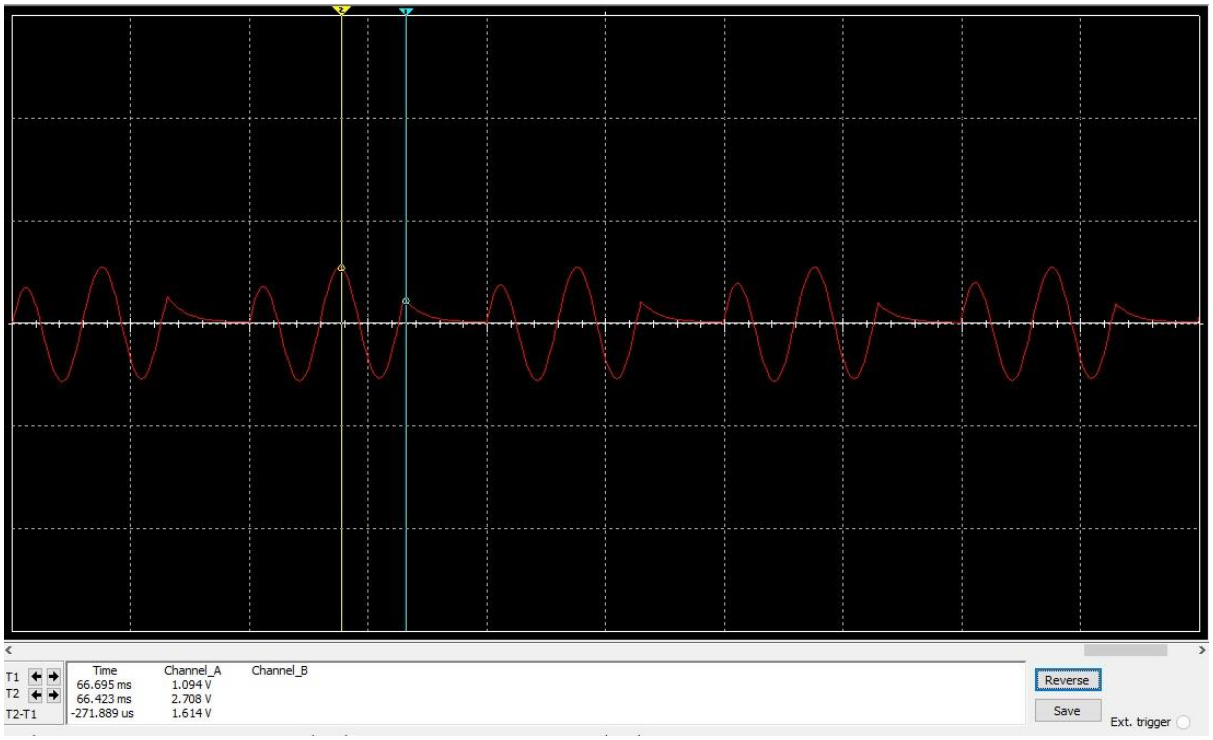


b) Multisim 14.0

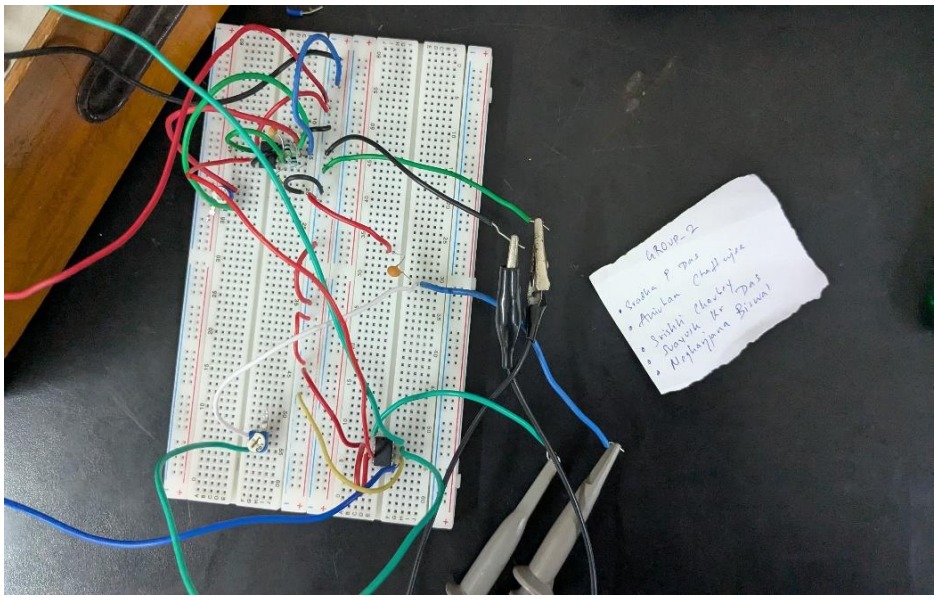
- **Diagram of the Circuit**

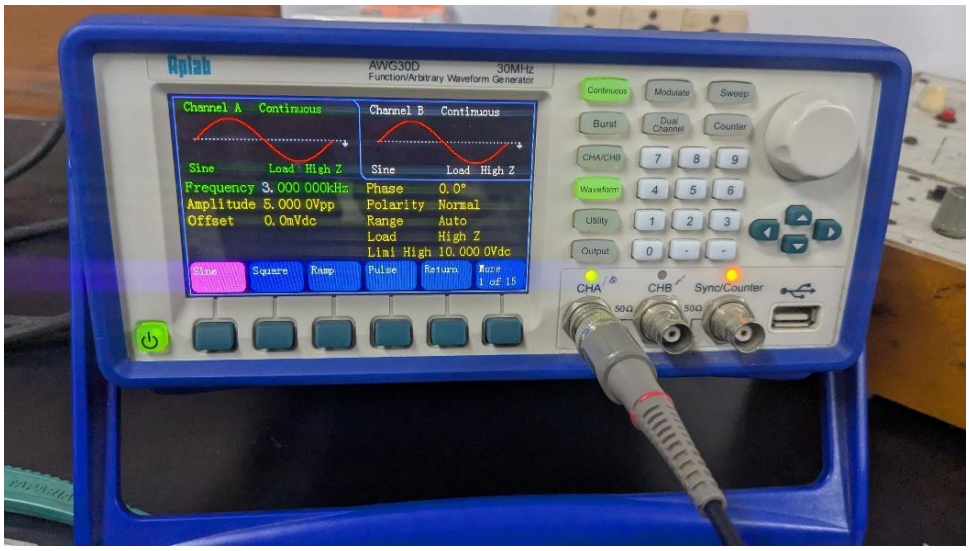


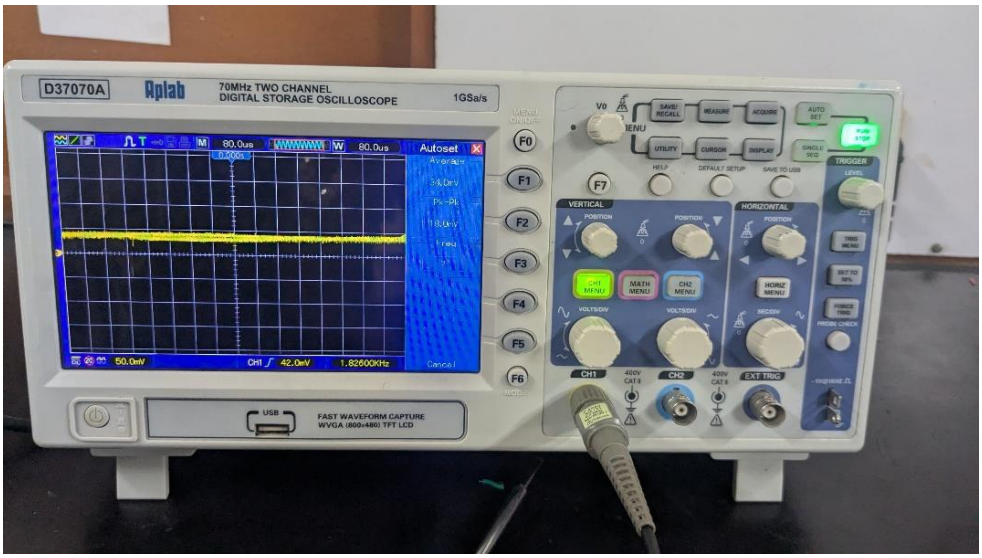
- **Output**



Hardware Design Analysis







9. Discussions and Conclusion

Discussion

The frequency down-conversion system developed in this project demonstrates the effective application of heterodyne principles for signal processing. By leveraging frequency mixing and filtering, the system successfully converts a 3 kHz input signal to a 2 kHz output signal while maintaining signal integrity. The use of a local oscillator and appropriate filters ensures that the desired frequency is accurately isolated, with minimal distortion and noise.

One of the key challenges encountered during the project was achieving a balance between simplicity and performance. While the direct frequency mixing approach was chosen for its straightforward implementation, significant attention was required in the design of the filters to suppress undesired frequencies effectively. Simulation and hardware testing highlighted the importance of optimizing filter cutoff frequencies to reduce artifacts.

The system's performance validates its applicability in fields such as telecommunications and audio processing, where precise frequency manipulation is critical. However, further improvements, such as incorporating advanced digital signal processing techniques or adaptive filtering, could enhance flexibility and performance under varying conditions.

Overall, the project successfully met its objectives, demonstrating the reliability of the selected approach. The findings underscore the potential of cost-effective analog solutions in practical frequency conversion applications, paving the way for further exploration in signal processing advancements.

References

741 IC datasheet:

Product Folder | Sample & Buy | Technical Documents | Tools & Software | Support & Community

TEXAS INSTRUMENTS

LM741 Operational Amplifier

1 Features

- Overload Protection on the Input and Output
- No Latch-Up When the Common-Mode Range is Exceeded

2 Applications

- Comparators
- Multivibrators
- DC Amplifiers
- Summing Amplifiers
- Integrator or Differentiators
- Active Filters

3 Description

The LM741 series are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439, and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common-mode range is exceeded, as well as freedom from oscillations.

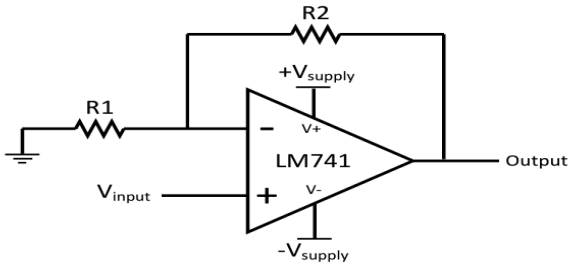
The LM741C is identical to the LM741 and LM741A except that the LM741C has their performance ensured over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM741	TO-99 (8)	9.08 mm × 9.08 mm
	CDIP (8)	10.16 mm × 6.502 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

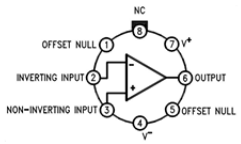
Typical Application



TEXAS INSTRUMENTS

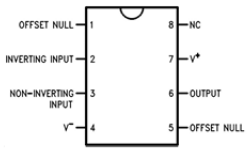
5 Pin Configuration and Functions

LMC Package
8-Pin TO-99
Top View



LM741H is available per JM38510/10101

NAB Package
8-Pin CDIP or PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INVERTING INPUT	2	I	Inverting signal input
NC	8	N/A	No Connect, should be left floating
NONINVERTING INPUT	3	I	Noninverting signal input
OFFSET NULL	1, 5	I	Offset null pin used to eliminate the offset voltage and balance the input voltages.
OFFSET NULL			
OUTPUT	6	O	Amplified signal output
V+	7	I	Positive supply voltage
V–	4	I	Negative supply voltage

AD633 IC datasheet:

ANALOG DEVICES

Low Cost Analog Multiplier

Data Sheet **AD633**

FEATURES

4-quadrant multiplication
Low cost, 8-lead SOIC and PDIP packages
Complete—no external components required
Laser-trimmed accuracy and stability
Total error within 2% of full scale
Differential high impedance X and Y inputs
High impedance unity-gain summing input
Laser-trimmed 10 V scaling reference

APPLICATIONS

Multiplication, division, squaring
Modulation/demodulation, phase detection
Voltage-controlled amplifiers/attenuators/filters

FUNCTIONAL BLOCK DIAGRAM

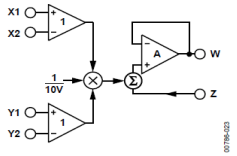


Figure 1.

GENERAL DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs, and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-lead PDIP and SOIC packages.

The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y input is typically less than 0.1% and noise referred to the output is typically less than 100 µV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/µs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The versatility of the AD633 is not compromised by its simplicity. The Z input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications. For further information, see the Multiplier Application Guide.

The AD633 is available in 8-lead PDIP and SOIC packages. It is specified to operate over the 0°C to 70°C commercial temperature range (J Grade) or the −40°C to +85°C industrial temperature range (A Grade).

PRODUCT HIGHLIGHTS

1. The AD633 is a complete four-quadrant multiplier offered in low cost 8-lead SOIC and PDIP packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

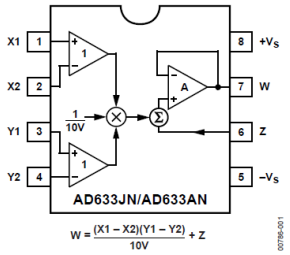


Figure 2. 8-Lead PDIP

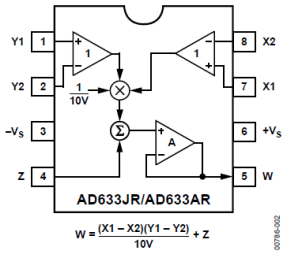


Figure 3. 8-Lead SOIC

Table 4. 8-Lead PDIP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	X Multiplicand Noninverting Input
2	X2	X Multiplicand Inverting Input
3	Y1	Y Multiplicand Noninverting Input
4	Y2	Y Multiplicand Inverting Input
5	$-V_S$	Negative Supply Rail
6	Z	Summing Input
7	W	Product Output
8	$+V_S$	Positive Supply Rail

Table 5. 8-Lead SOIC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Y1	Y Multiplicand Noninverting Input
2	Y2	Y Multiplicand Inverting Input
3	$-V_S$	Negative Supply Rail
4	Z	Summing Input
5	W	Product Output
6	$+V_S$	Positive Supply Rail
7	X1	X Multiplicand Noninverting Input
8	X2	X Multiplicand Inverting Input