EE311 DIGITAL SYSTEM DESIGN - ASSIGNMENT 4

Submission due: 05th June 2020

1. **(a)** Calculate how many full adders, half adders, and AND gates are required for a 8 × 8 array multiplier.

   (b) What is the longest delay in an 8 × 8 array multiplier, assuming an AND gate delay is *t*g = 1 ns, and an adder delay (full adder and half adder) is *t*ad = 2 ns?

   (c) For an 8-bit × 8-bit add-and-shift multiplier, how fast must the clock be in order to complete the multiplication in the same time as in part (b)?

2. **(a)** Estimate how many AND gates and adders will be required for a 16-bit × 16-bit array multiplier.

   (b) What is the longest delay in a 16 × 16 array multiplier, assuming an AND gate delay is *t*g, and an adder delay (full adder and half adder) is *t*ad?

3. **(a)** If gate delays are 5 ns, what is the delay of the fastest 4-bit ripple carry adder? Explain your calculation.

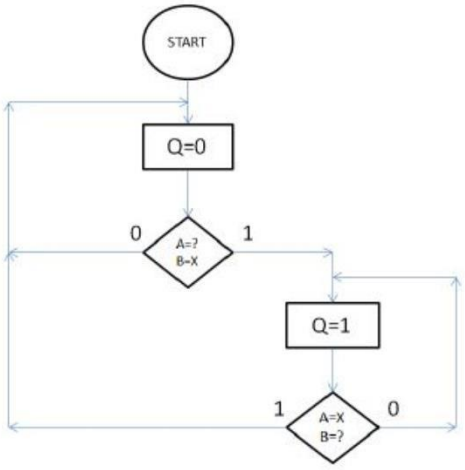
   (b) If gate delays are 5 ns, what is the delay of the fastest 4-bit adder? What kind of adder will it be? Explain your calculation.

4. How many square boxes (state representation) would be required in ASM representation of 1001 detector?

5. Moore machines can always be represented as Mealy machines but Mealy machine cannot always be represented by Moore machine.

   State the above statement is true or false and justify.

6. Deduce the type of flip-flop from the following ASM chart.



7. Consider a Moore machine with 3 flip-flops, 2 inputs and 5 outputs. Determine the maximum number of transition arrows leaving and number of transition arrows entering a state.

8. The number of flip-flops required for the synthesis of a sequential logic circuit with N states is -------.

9. In BCD addition, if the result is less than or equal to 1001 then further addition of 0110 corrects the representation, is this statement true or false, justify.

10. A = $(14)_{10}$ and B = $(7)_{10}$ what is $C_3C_2C_1$ and $C_4S_3S_2S_1S_0$ in binary.