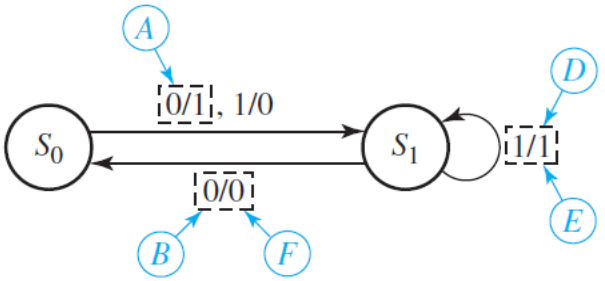
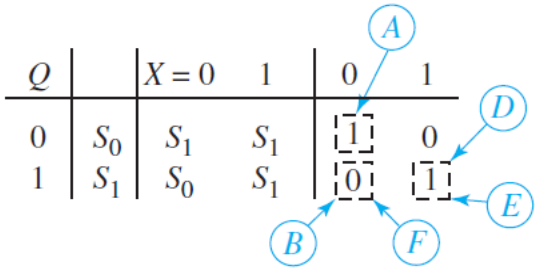
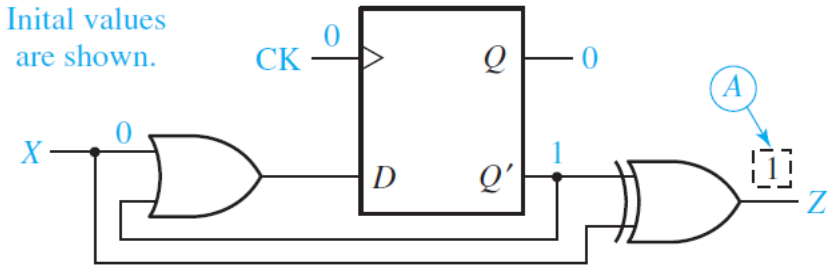
Sequential circuit timing

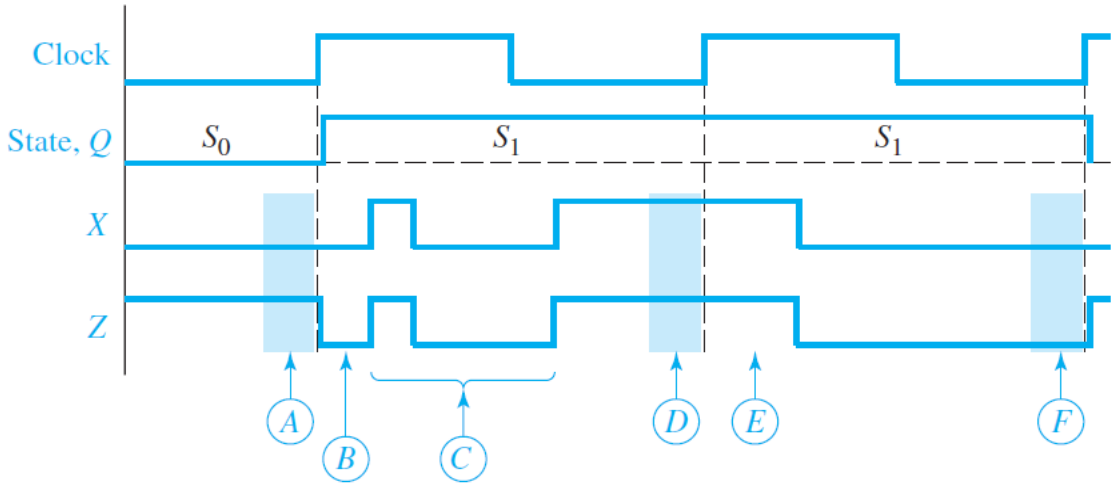
Timing chart – example



Q		$X = 0$	1
0	S_0	S_1	S_1
1	S_1	S_0	S_1







X and Z in shaded area
(before rising edge of clock).

Timing diagrams

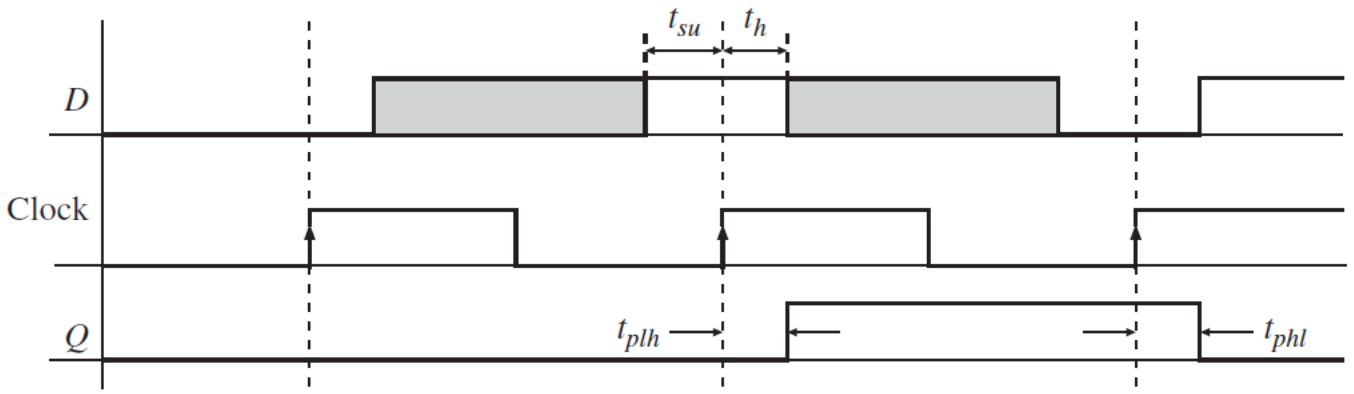
- Sequence of events during one clock period.
- Following the active edge of the clock – flip-flops change state.
- Flip-flop output stable – after propagation delay.
- New value of Q propagate through combinational circuit – D value stable after combinational circuit delay t_c.
- Speed of the sequential circuit and minimum clock period.

Timing diagrams

Important issues in designing sequential circuits:

- Propagation delays of flip-flops, gates and wires.
- Setup times and hold times of flip-flops.
- Clock synchronization.
- Clock skew.

Timing diagrams



Setup and hold times for D flip-flop

- Ideal D flip-flop – D input changed at exactly the same time as the active edge of the clock .

Timing diagrams

Propagation delay or clock-to-Q delay:

- Amount of time that elapses from the time the clock changes to the time the Q output changes.
- Can depend on whether output changing from high to low or vice-versa.

Timing diagrams

- Real flip-flop – D input must be stable for a certain amount of time before the active edge of the clock – time interval – setup time (t_{su})
- D must be stable for a certain amount of time after the active edge of the clock – time interval - hold time (t_h)

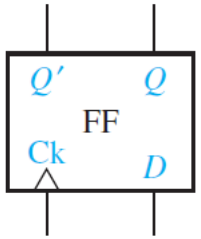
Timing diagrams

- Change in D anytime – during forbidden interval – flip-flop state change cannot be determined.
- Worst case – flip-flop malfunction - output a short pulse, or go into oscillation.
- Set-up, hold times, propagation delay – obtained from manufacturer's data sheets or ASIC libraries accompanying design tools.
- - Create complications in sequential circuit timings.

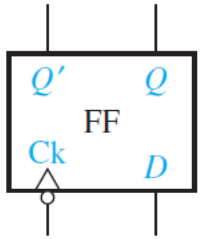
Timing conditions

- Maximum clock frequency for a sequential circuit – influenced by several factors.
- Clock period – must be long enough – all flip-flops and register inputs will have time to stabilize before the next active edge of the clock.
- STA: Static Timing Analysis – method for validating timing performance of a design.
- By checking all possible paths for timing violations under worst case conditions.

Timing diagrams



(a) Rising-edge trigger



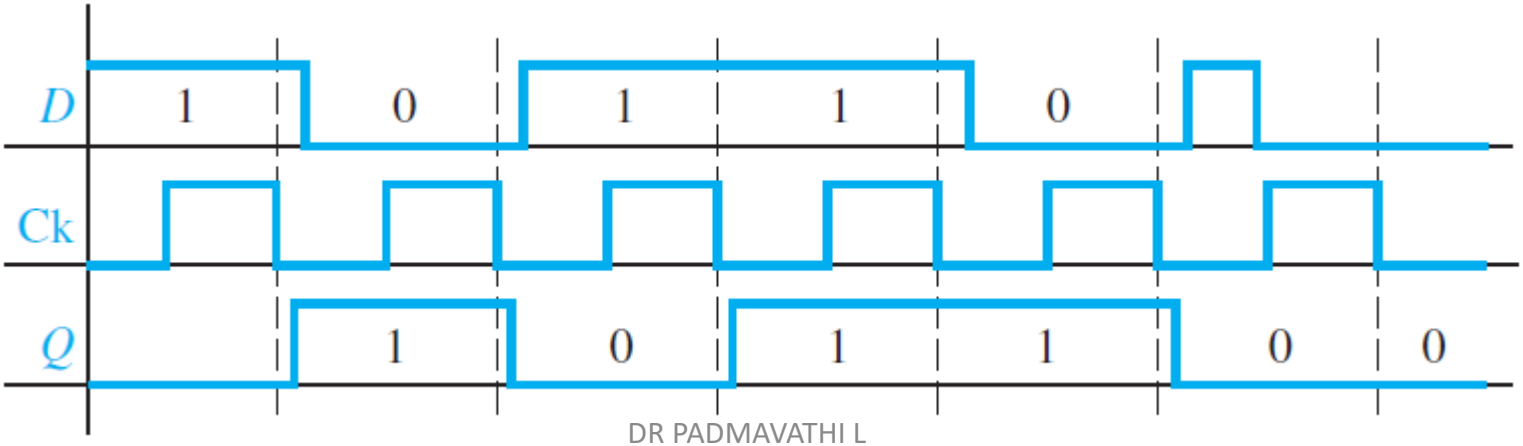
(b) Falling-edge trigger

D Q	Q^+
0 0	0
0 1	0
1 0	1
1 1	1

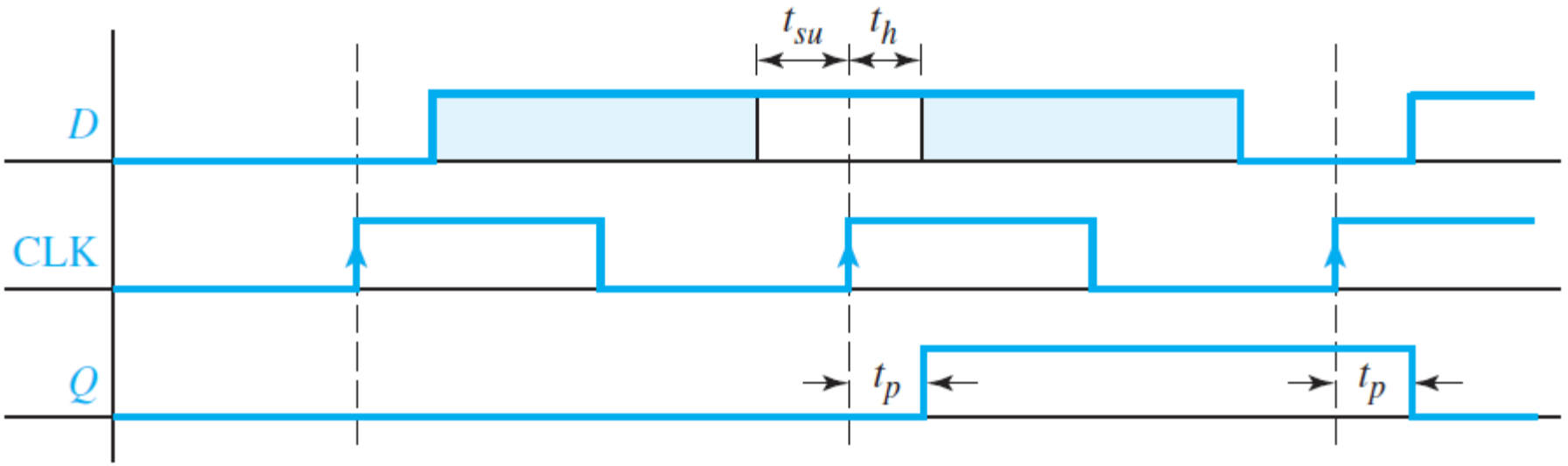
(c) Truth table

$Q^+ = D$

Timing for D Flip-Flop (Falling-Edge Trigger)

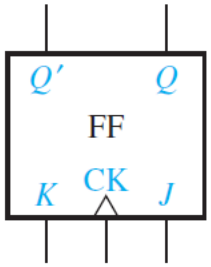


Timing diagrams



Setup and Hold Times for an Edge-Triggered D Flip-Flop

Timing diagrams



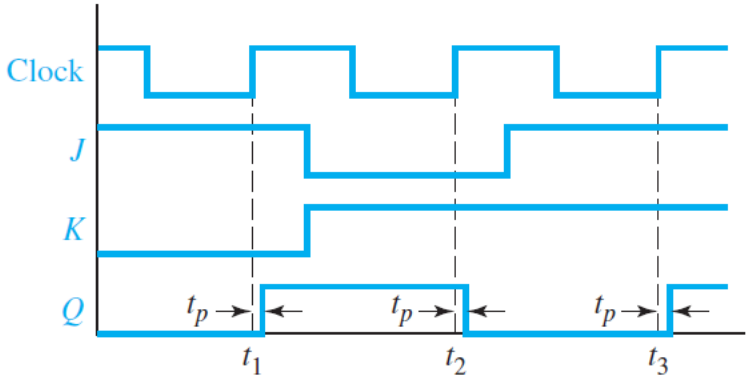
(a) J-K flip-flop

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b) Truth table and characteristic equation

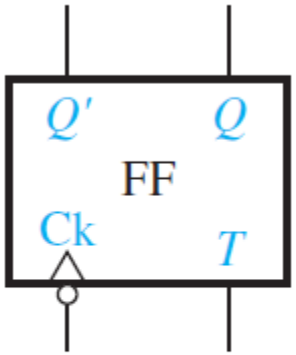
$$Q^+ = JQ' + K'Q$$

J-K Flip-Flop
(*Q* Changes on the Rising Edge)



(c) J-K flip-flop timing

Timing diagrams



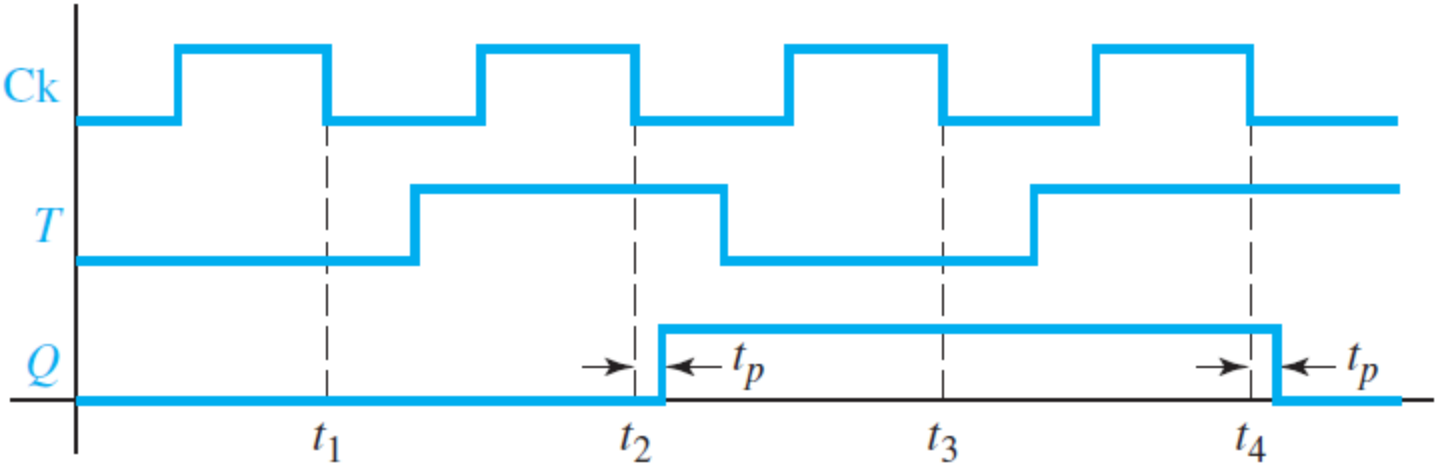
(a)

T Q	Q^+
0 0	0
0 1	1
1 0	1
1 1	0

(b)

$$Q^+ = T'Q + TQ' = T \oplus Q$$

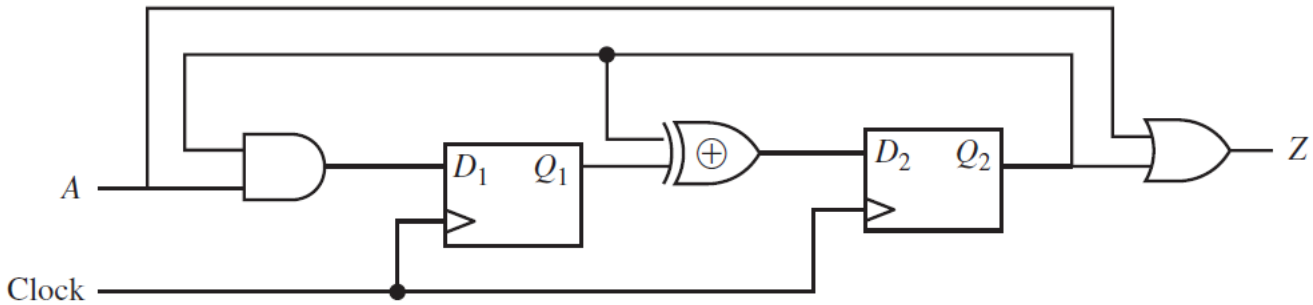
Timing Diagram for T Flip-Flop (Falling-Edge Trigger)



Timing paths in synchronous digital systems

1. Register to register paths.(FF to FF)
2. Primary input to register paths (input to FF)
3. Register to primary output paths(FF to output)
4. Input to output paths (no FF)

Circuit to illustrate timing paths



Circuit to illustrate timing paths

There are six static timing paths in this circuit:

I. From A to D_1 (primary input to flip-flop)
II. From D_1 to D_2 including the XOR (flip-flop to flip-flop)
III. From D_2 via XOR to D_2 (flip-flop to flip-flop)
IV. From D_2 to D_1 via AND (flip-flop to flip-flop)
V. From D_2 to Z via the OR gate (flip-flop to output)
VI. From A to Z via the OR gate (input to output)

Timing conditions

- **Setup time violation** – if the data changes just before the cock – without providing enough setup time for the flip flop.

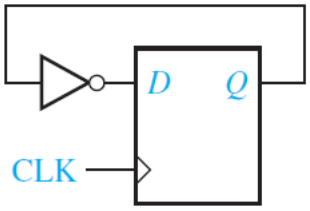
- **Hold-time violation** – data changes just after the clock without providing enough hold time for the flip flop.

- **Paths** – must have zero or positive slack in order to have no violations.

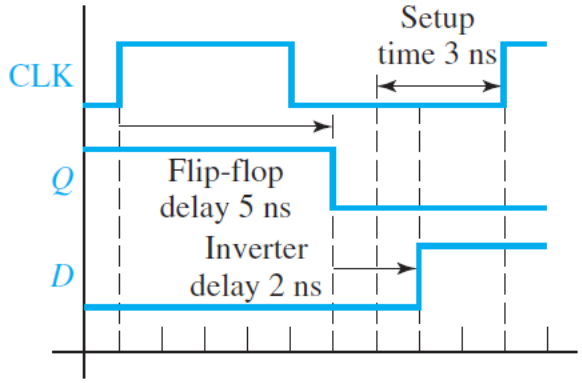
Timing conditions for proper operation

- Paths with zero or very small slack – speed limiting paths in the design.
- Any small changes or gate delays will lead to violations in such circuits.
- Paths with negative slack time – already violated a setup or hold constraint.

Timing diagrams

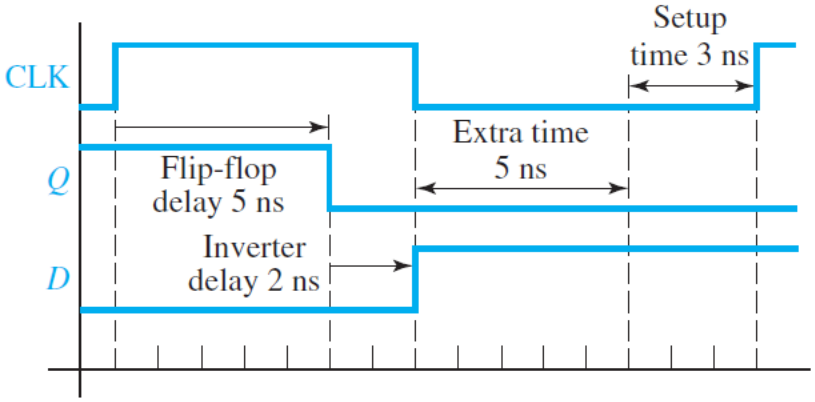


(a) Simple flip-flop circuit

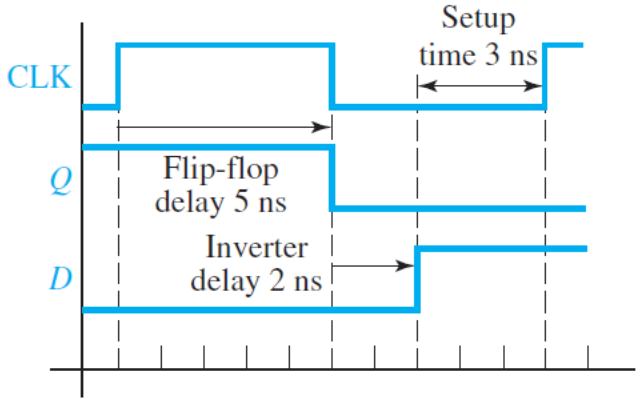


(b) Setup time not satisfied

Clock period 9 ns



(c) Setup time satisfied



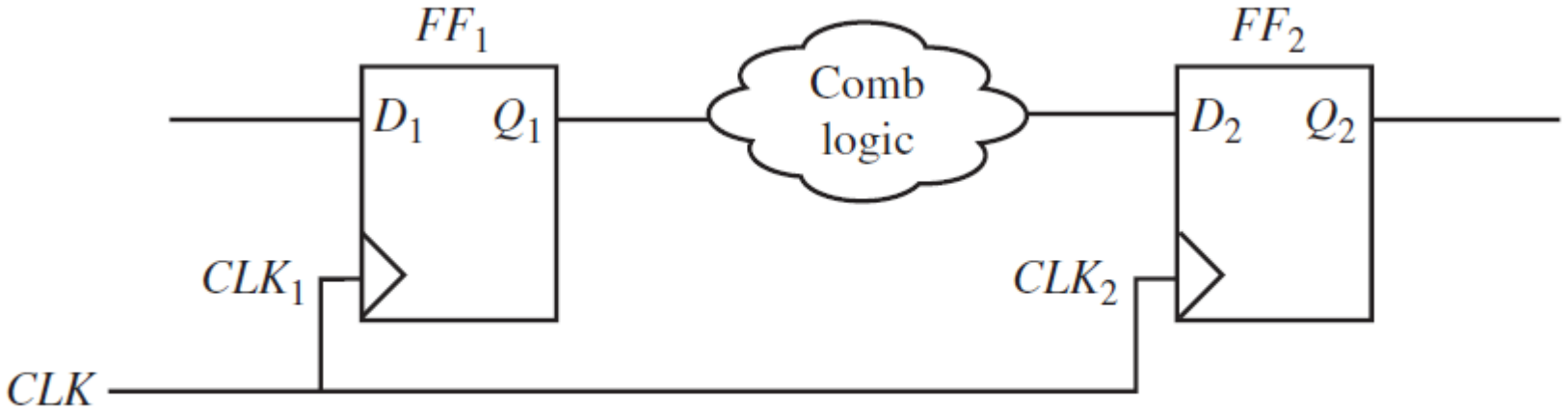
(d) Minimum clock period

Clock period 15 ns

Determination of Minimum Clock Period

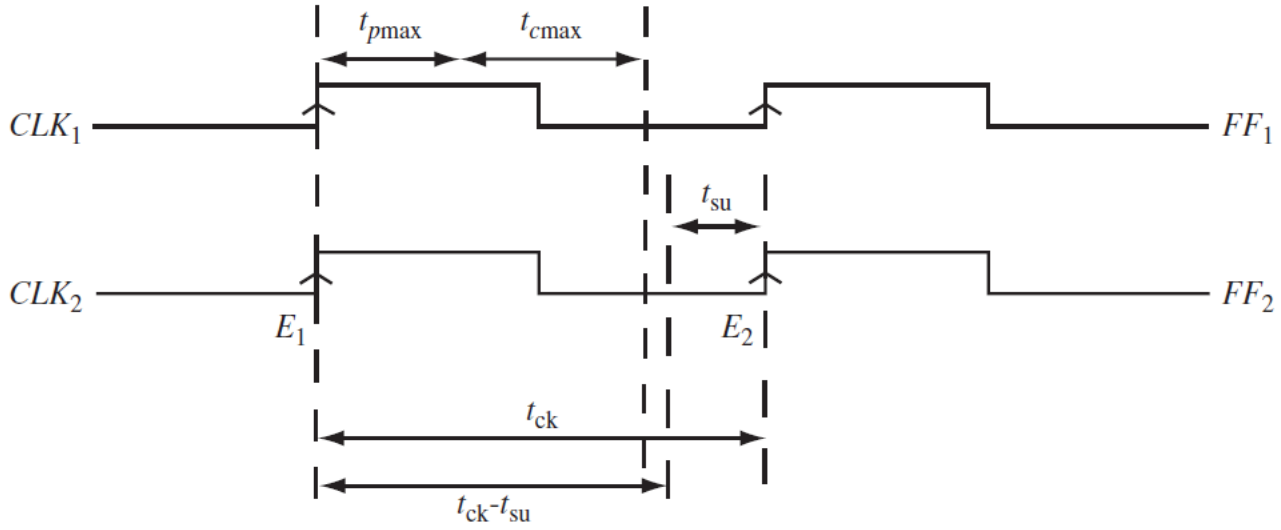
Clock period 10 ns

Timing rules



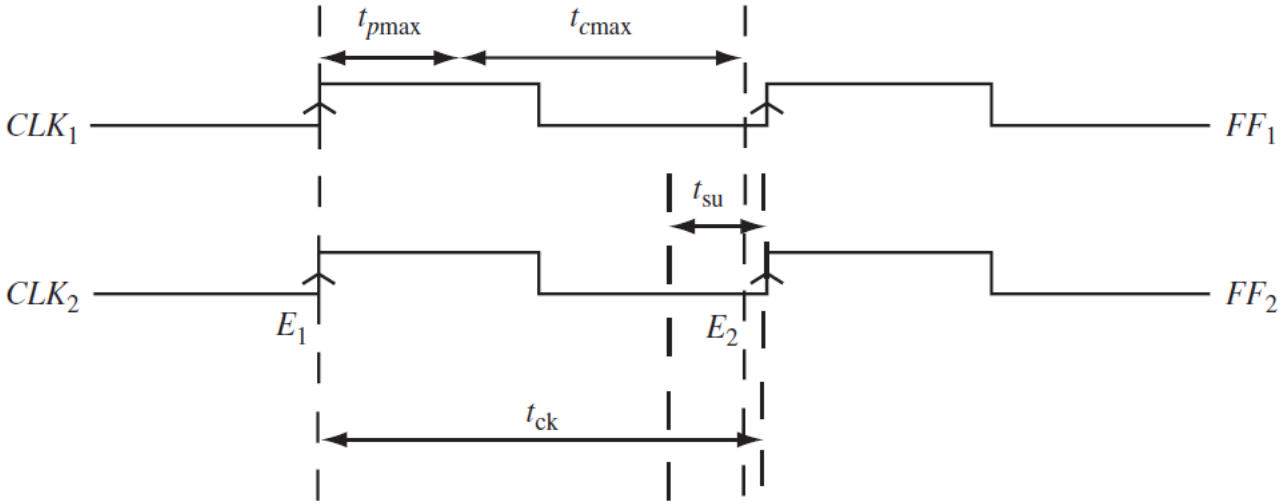
(a) Circiut

FF_1 – launching FF, FF_2 – capturing FF.



(b) Timing diagram when setup time is met

Timing rules



(c) Timing diagram when setup time is violated

Timing rules - FF to FF paths:

- t_{cmax} – maximum propagation delay through the combinational circuit.
- t_{cmin} – minimum propagation delay through the combinational circuit.
- t_{pmax} – maximum clock to Q delay.(propagation delay from the time the clock changes to the time the FF output changes).(maximum of t_{plh} and t_{phl}).
- t_{pmin} – minimum clock to Q delay.

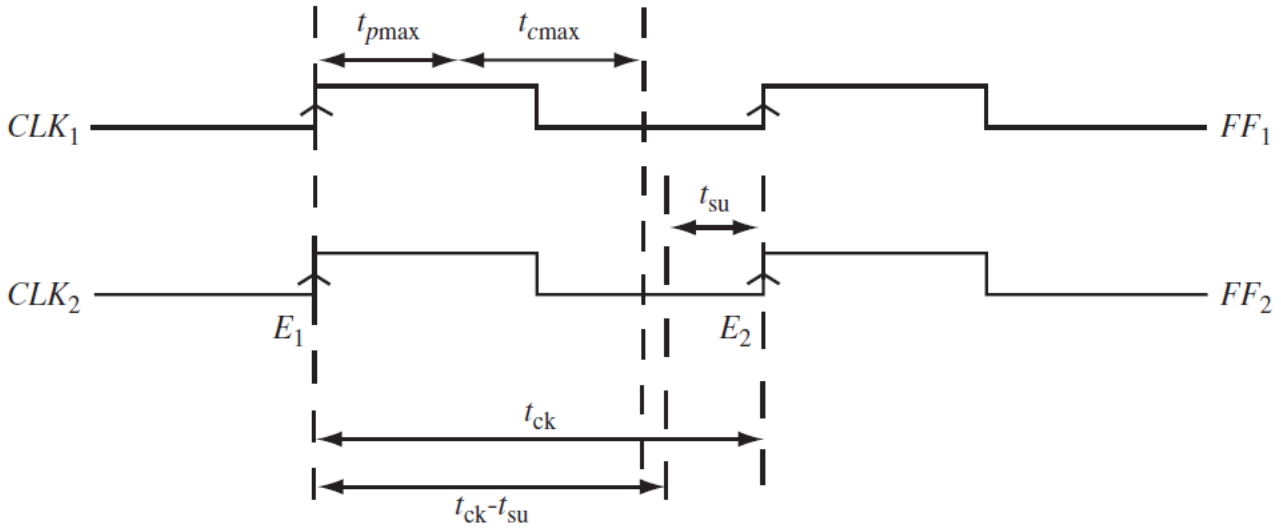
Timing rules

Rule No. 1: Setup time rule for flip-flop to flip-flop path: Clock period should be long enough to satisfy flip-flop setup time.

- Clock period – long enough to allow the FFs output change, combinational circuitry to change – still leaving enough time to satisfy setup time.

Timing rules

- Proper synchronous operation – data launched by FF_1 at edge E_1 of clock CLK_1 – should be captured by FF_2 at edge E_2 of clock CLK_2.



(b) Timing diagram when setup time is met

Timing rules

- Maximum time from the active edge E_1 of the clock CLK_1 to the time the change in Q_1 propagates to the second FF input (D_2) – t_{pmax} + t_{cmax}.

- In order to ensure proper FF operation – combinational circuit output must be stable at least t_{su} before the end of the clock E_2 reaches FF_2.

$$t_{ck} \geq t_{p\max} + t_{c\max} + t_{su}$$

Clock period tck:

Timing rules

- Setup time violations – solved by changing the clock frequency.
- $t_{ck} – t_{pmax} – t_{cmax} – t_{su}$ – setup time margin – zero or positive – in order to have a circuit pass timing checks.
- Check for setup time violations by checking

$$t_{ck} - t_{pmax} - t_{cmax} - t_{su} \geq 0$$

Timing rules

- Design process – FFs and gates are selected from vendors design library – provide fixed t_{pmax} and t_{su}.
- Choice – a different design library with desirable t_{pmax} and t_{su} available to use
- Adjust the clock frequency of the circuit or combinational delay of the logic.
- Clock frequency – comes from customer requirements – meet timing constraints by correct combinational delays.

Timing rules

Rule No. 1: Setup time rule for flip-flop to flip-flop path: Clock period should be long enough to satisfy flip-flop setup time.

Rule No. 2 Hold-time rule for flip-flop to flip-flop path: Minimum circuit delays should be long enough to satisfy flip-flop hold time.

Timing rules

- For proper synchronous operation - data launched by FF_1 on edge E_1 of clock CLK_1 – should not be captured by FF_2 on edge E_1 of clock CLK_1.

- At E_2, FF_2 should capture the data launched by FF_1 on the previous edge E_1 – for this to be satisfied – old data should remain stable at edge E_2 until FF_2s hold time.

- FF_2 capturing old data at edge E_2 – FF_1 started to launch new data on edge E_2 – should be captured by FF_2 only at edge E_3.

Timing rules

- Hold time violation occurs when – if the data launched by FF_1 at E_2 fed through the combinational circuit – causes D_2 to change too soon after the clock edge E_2.

- New data launched by FF_1 takes at least t_{pmin} time – to pass through FF_1, t_{cmin} – to pass through the combinational circuitry

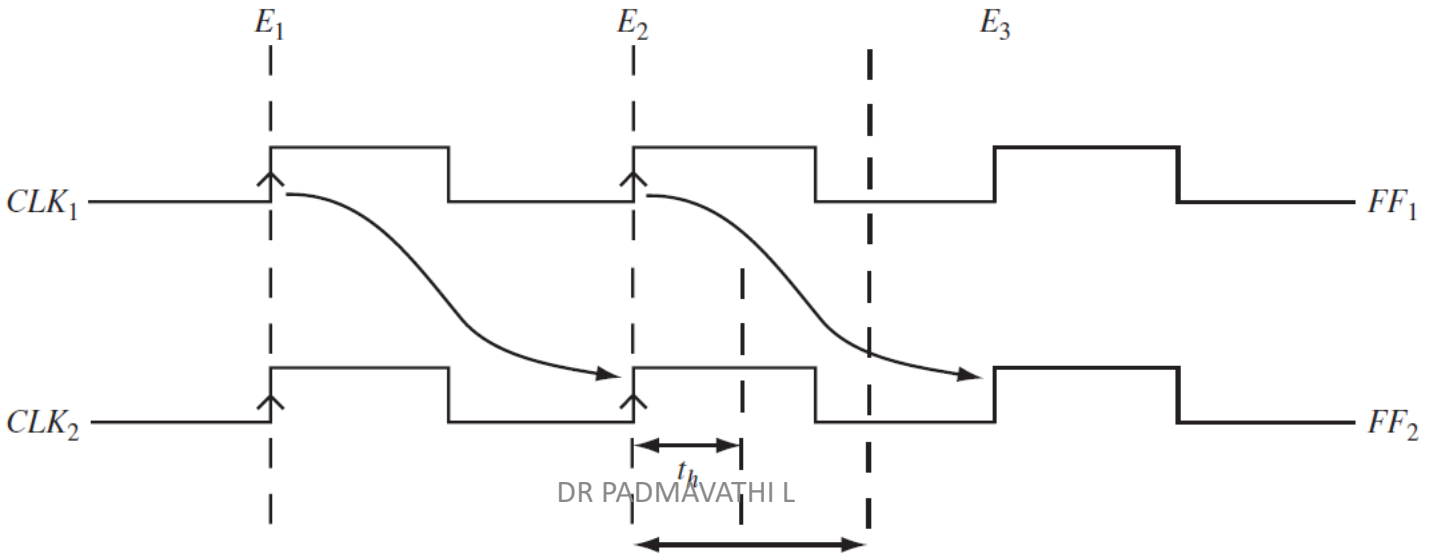
- Hold time condition:

$$t_{pmin} + t_{cmin} \geq t_h$$

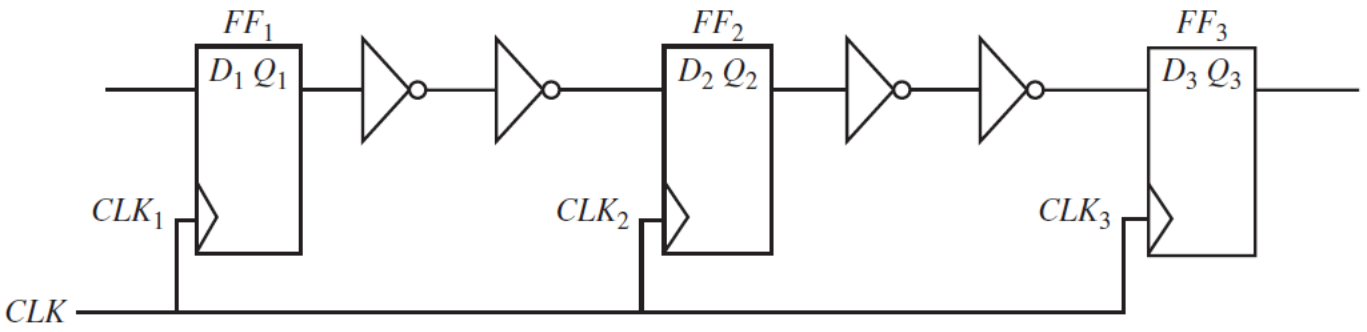
Timing rules

- Usually t_{pmin} for FFs > t_h – hold time violation due to change in Q usually don't occur.

- Hold time violation – can not be corrected by changing the clock frequency of the circuit – circuit need to be redesigned.



Timing rules



Shift registers with buffers for meeting hold tie constraints.

Timing rules

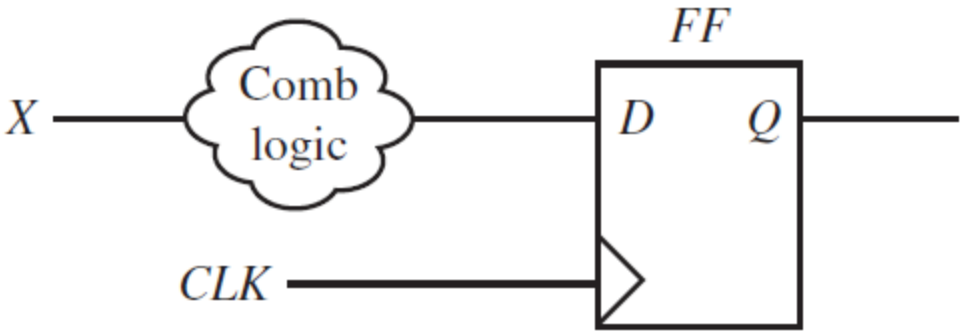
- Design of shift registers and counters – by chaining together FFs – easy from functional perspective.
- Difficult to meet hold time constraints – combinational circuit delay - zero.
- Inserting buffers between FFs – usual way to correct such designs.

Timing rules for input to FF paths:

Rule No. 3 Setup time rule for input to flip-flop path: External input changes to the circuit should satisfy flip-flop setup time.

- Setup time violation could occur - X input to the circuit changes too close to the active edge of the clock.
- X input change – input change propagates to FF input such that setup time is satisfied before the active edge of the clock.

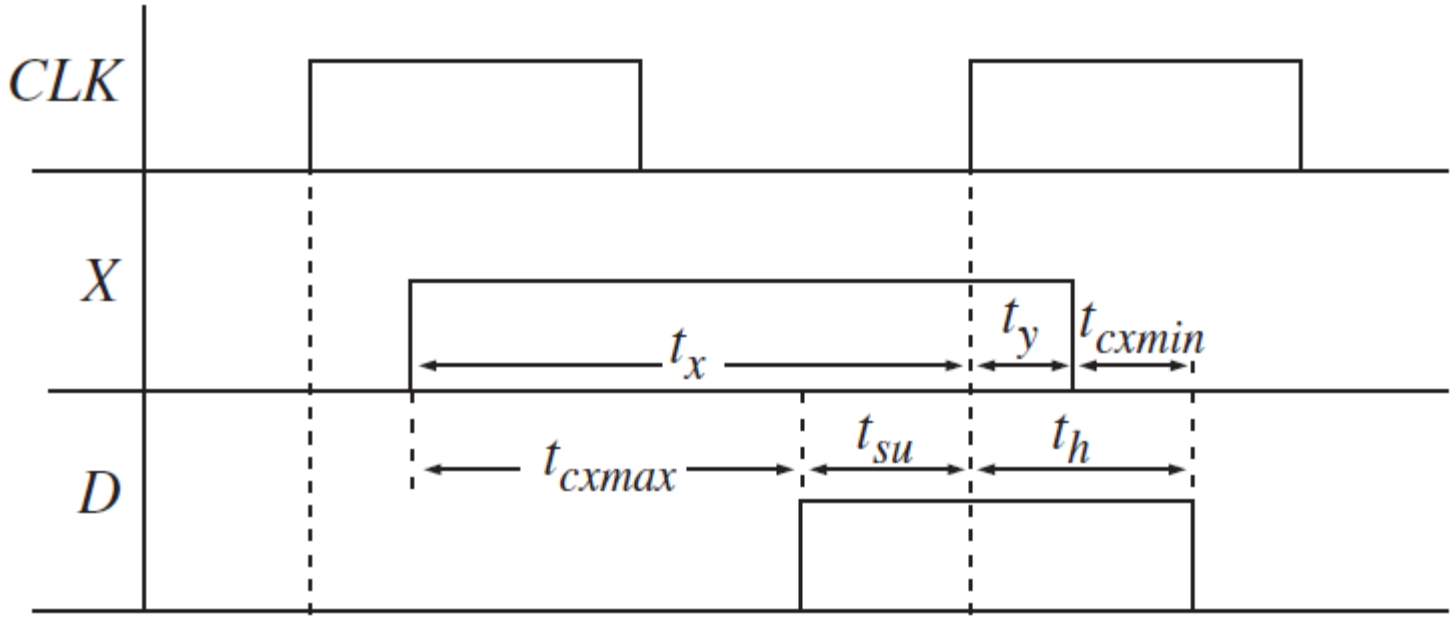
Timing rules for input to FF paths



Input to FF path timing

- Changes in primary input X allowed to happen – input propagates to FF satisfying both setup and hold time constraints.

Timing rules for input to FF paths



$$t_x \geq t_{cxmax} + t_{su} \qquad t_y \geq t_h - t_{cxmin}$$

t_{cxmax} - maximum propagation delay from X to the FF input.

Setup and hold time for changes in X.

Timing rules for input to FF paths:

- If X changes at time t_x before the active edge of the clock – it could take up to the maximum propagation delay of the combinational circuit – before change in X propagates to FF input.

- A margin of t_{su} should be left – before the edge of the clock.

$$t_x \geq t_{cx\max} + t_{su}$$

t_{cxmax} - maximum propagation delay from X to the FF input.

Timing rules for input to FF paths:

Rule No. 3 Setup time rule for input to flip-flop path: External input changes to the circuit should satisfy flip-flop setup time.

Rule No. 4 Hold-time rule for input to flip-flop path: External input changes to the circuit should satisfy flip-flop hold times.

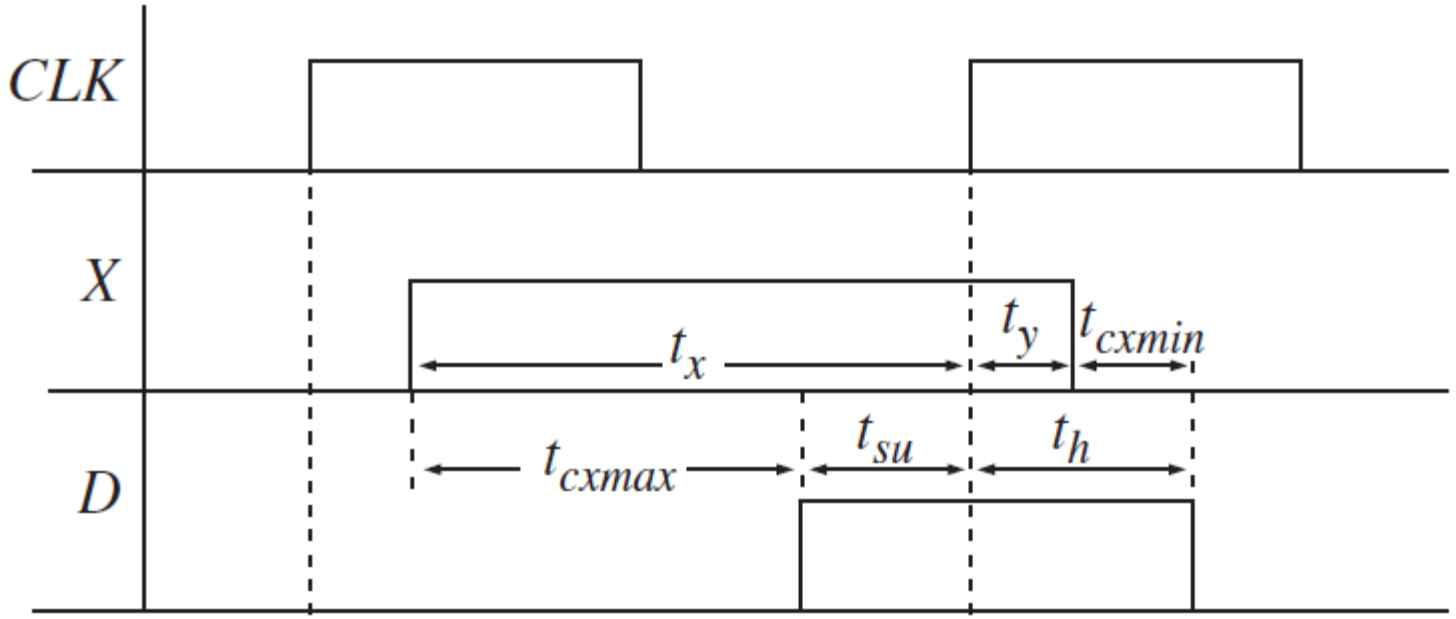
Timing rules for input to FF paths:

- To satisfy hold time constraint – must make sure X does not change too soon after the clock.
- X changes at time t_y after the active edge of the clock,

$$t_y \geq t_h - t_{cx\min}$$

- Condition for hold time

Timing rules for input to FF paths



$$t_x \geq t_{cxmax} + t_{su} \qquad t_y \geq t_h - t_{cxmin}$$

t_{cxmax} - maximum propagation delay from X to the FF input.

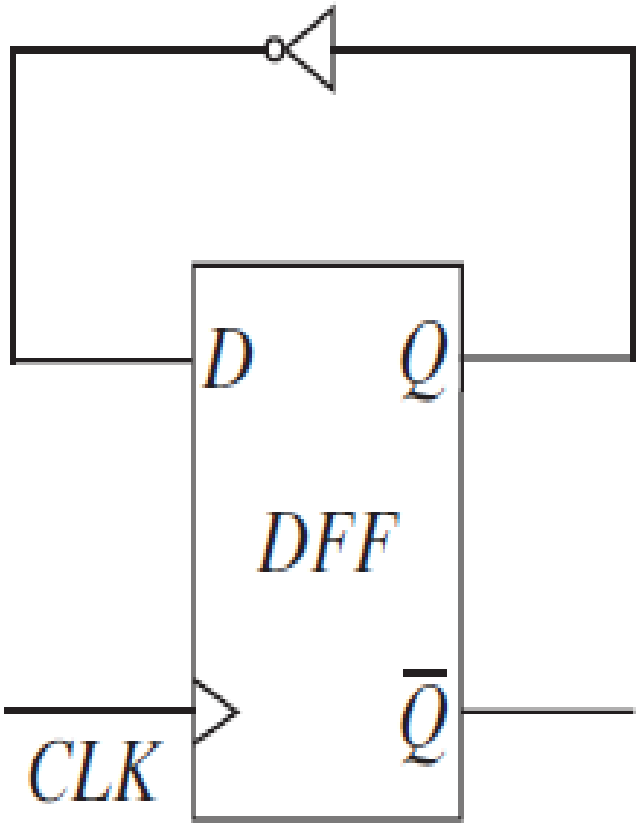
Setup and hold time for changes in X.

Timing rules for input to FF paths:

- Change in X – propagates to the FF input in zero time – X should not change for a duration of t_h after the clock edge.

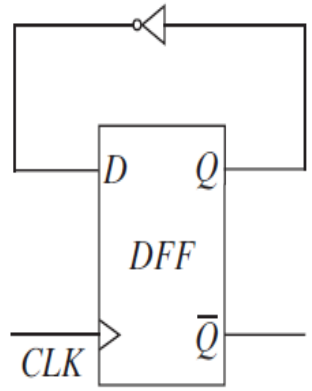
- t_{cxmin} – minimum propagation delay from X to the FF input(changes in X will not reach FF input until at least a time of t_{cxmin} has elapsed after the clock edge)

Timing rules - Simple frequency divider

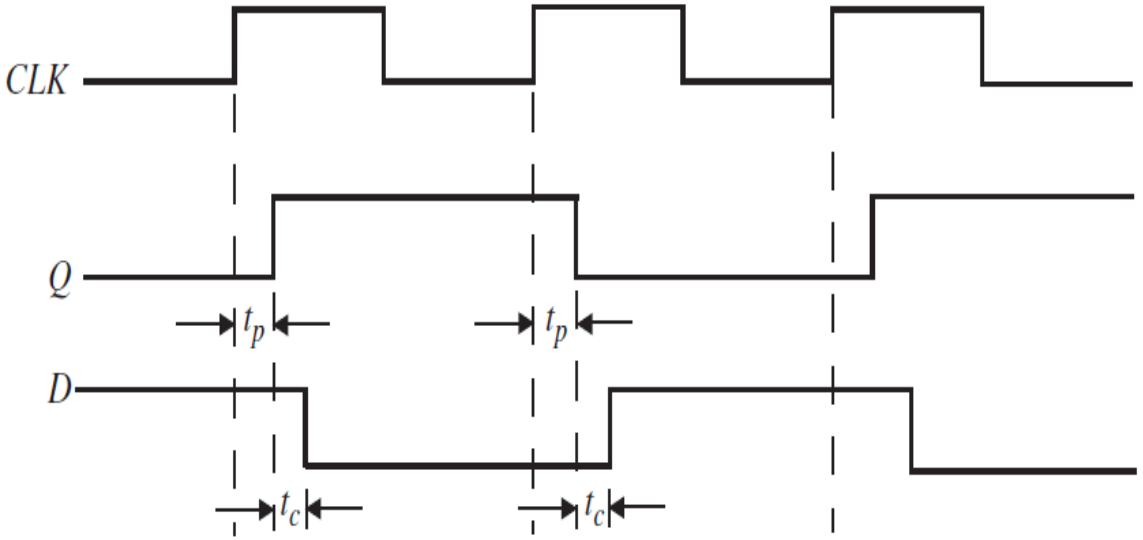


(a) A frequency divider

Timing rules - Simple frequency divider



(a) A frequency divider



(b) Frequency divider timing diagram

Timing rules - Simple frequency divider

- Increase the frequency to be very high – output of the inverter may not have enough time to stabilize – to meet the setup time requirements.
- Choosing a fast inverter – feed the inverter output to the D input extremely quickly – hold time constraints of FF may not be met.
- Variety of ways timing problems could arise from propagation delays, setup and hold time requirements.

Timing rules

- Maximum clock frequency $f_{max} = 1/t_{ckmin}$
- Minimum delay of the inverter = 1 ns, maximum delay = 3 ns
- t_{pmin} and t_{pmax} = 5ns and 8 ns.
- Setup and hold times of the FF = 4ns and 2 ns.

Timing rules

Minimum clock period for the simple frequency divider:

$$t_{ckmin} = t_{p\max} + t_{c\max} + t_{su}$$

Timing rules

- Maximum clock frequency $f_{max} = 1/t_{ckmin}$
- Minimum delay of the inverter = 1 ns, maximum delay = 3 ns
- t_{pmin} and t_{pmax} = 5ns and 8 ns.
- Setup and hold times of the FF = 4ns and 2 ns.
- t_{ck} >= 15ns, maxm clock frequency = 66.67 MHz.

Timing rules

Hold time requirement to be satisfied – D input should not change before 2 ns after the clock edge.

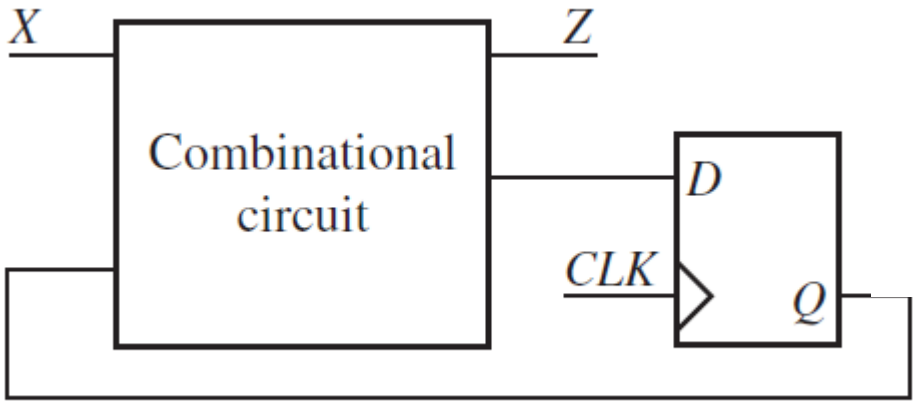
$$t_{p\min} + t_{c\min} \geq t_h$$

Timing rules

- Delay of the combinational circuit – 2 to 4 ns.

- FF propagation delays – 5 to 10 ns.
- Set up time – 8 ns. Hold time – 3 ns.

$$t_{ck} \geq t_{pmax} + t_{cmax} + t_{su}$$

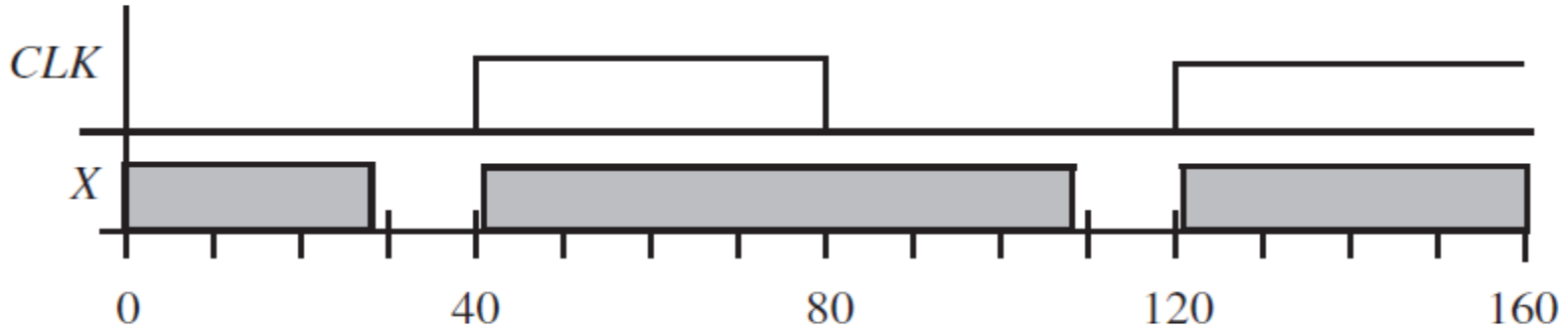


A sequential circuit

$$t_{pmin} + t_{cmin} \geq t_h$$

Timing rules

- External input X
- Identify safe regions where x input can change using rule no. 3 and 4.
- X input – should be stable for a duration 12ns before the clock edge.



(b) Safe regions for changes in X

Timing rules

- X input – should be stable for a duration 12ns before the clock edge.
- X input – should be stable for a duration 1 ns after the clock edge.

$$t_x \geq t_{cx\max} + t_{su}$$

$$t_y \geq t_h - t_{cx\min}$$

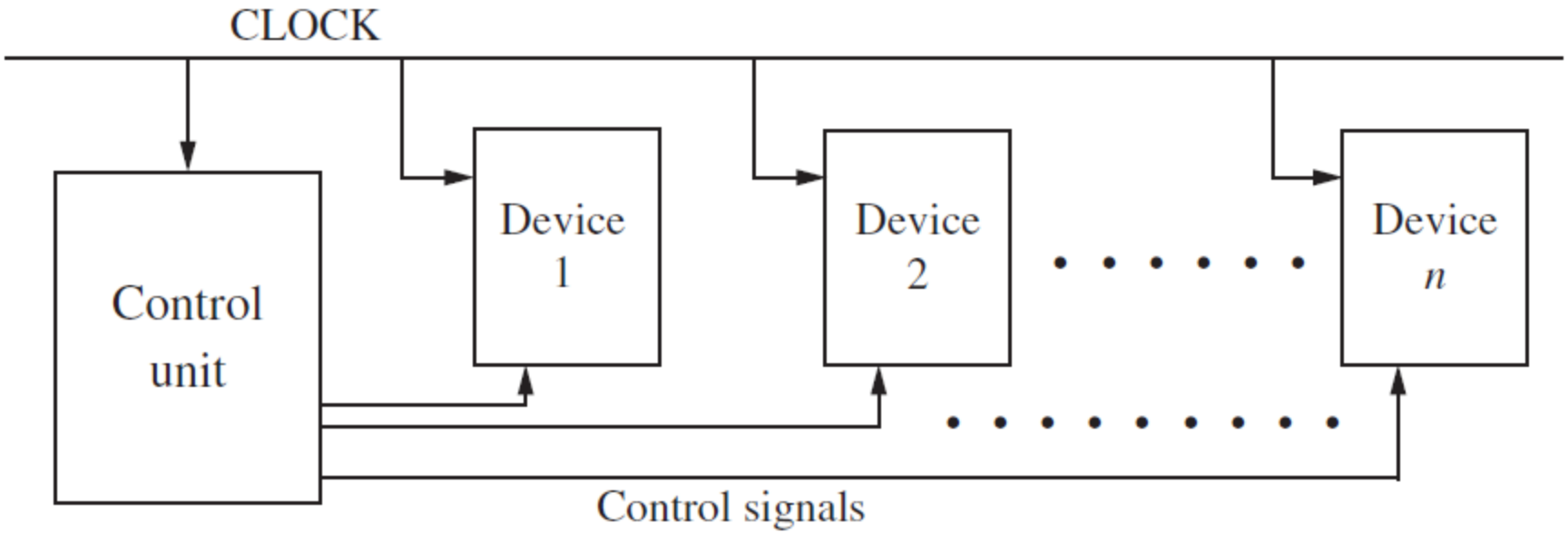
Timing rules

- Typical sequential circuit – millions of timing paths need to be considered – to derive maximum clock frequency.
- Locate the longest path among all timing paths – determine maximum frequency of operation.

Synchronous design

- Commonly used digital design technique.
- Clock – synchronize the operation of all FFs, registers and counters in the system.
- Events occur immediately following the active edge of the clock.

Synchronous design



Synchronous digital systems

All sequential devices – synchronized w.r.t same clock.

Synchronous design

- Digital systems – two sections – data section and a control section.
- Various devices used in the system – part of the data section.
- Control section – a sequential machine that generates control signals to control the operation of the data section.
- Shift Register – data section
- Control section – generate signals that determine when the register to be loaded and when to be shifted.

Synchronous design

- Common clock to synchronize the operation of the control and data sections.
- Data section – generates status signals – affect the control sequence.
- Control section – controller, data section – data path or architecture.

Synchronous design

- Synchronous digital systems – all changes might not happen immediately at the active edge of the clock.
- Significant wire delays compared to the clock period.
- Two FFs connected to same clock – clock edge might arrive at the two FFs at different times – unequal wire delays.
- Unequal wire delays cause – clock reach different devices at slightly different times.

Synchronous design

- Unequal wire delays cause – clock reach different devices at slightly different times – clock skew.

- Clock skew – absolute time difference in clock signal arrival between two points in the clock network.

- Caused by the delays in the interconnect within the clock distribution networks.

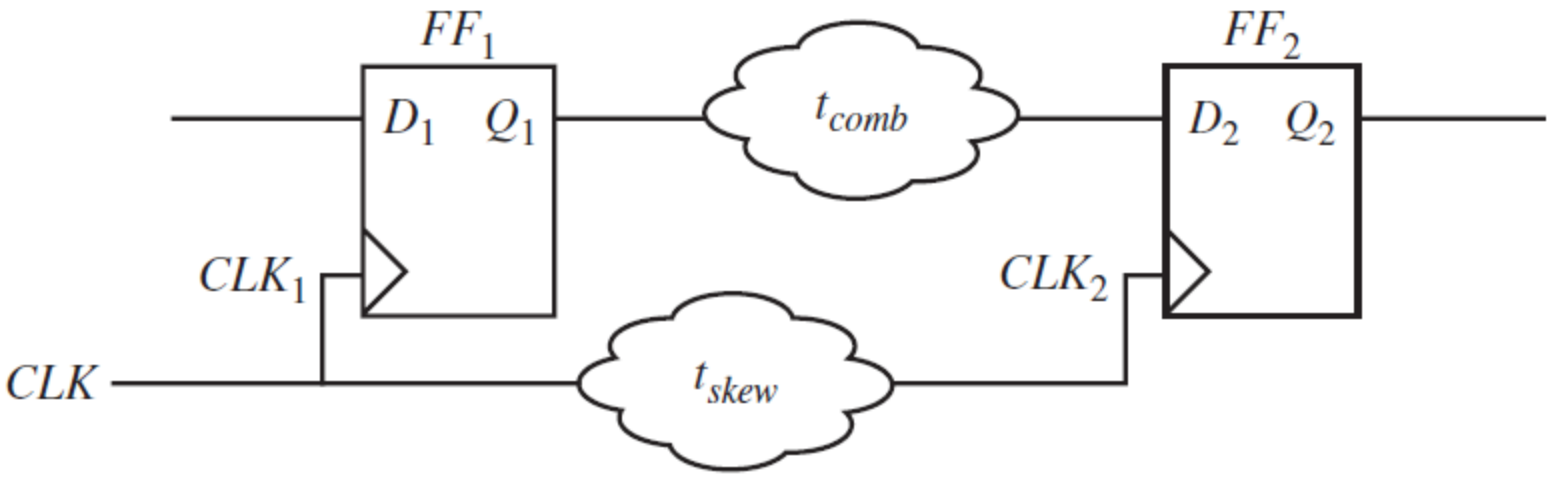
Timing rules for circuits with skew

- Positive skew – capturing FF gets the clock delayed w.r.t the launching FF.

Rule No. 5: $t_{ck} \geq t_{p\max} + t_{c\max} - t_{skew} + t_{su}$

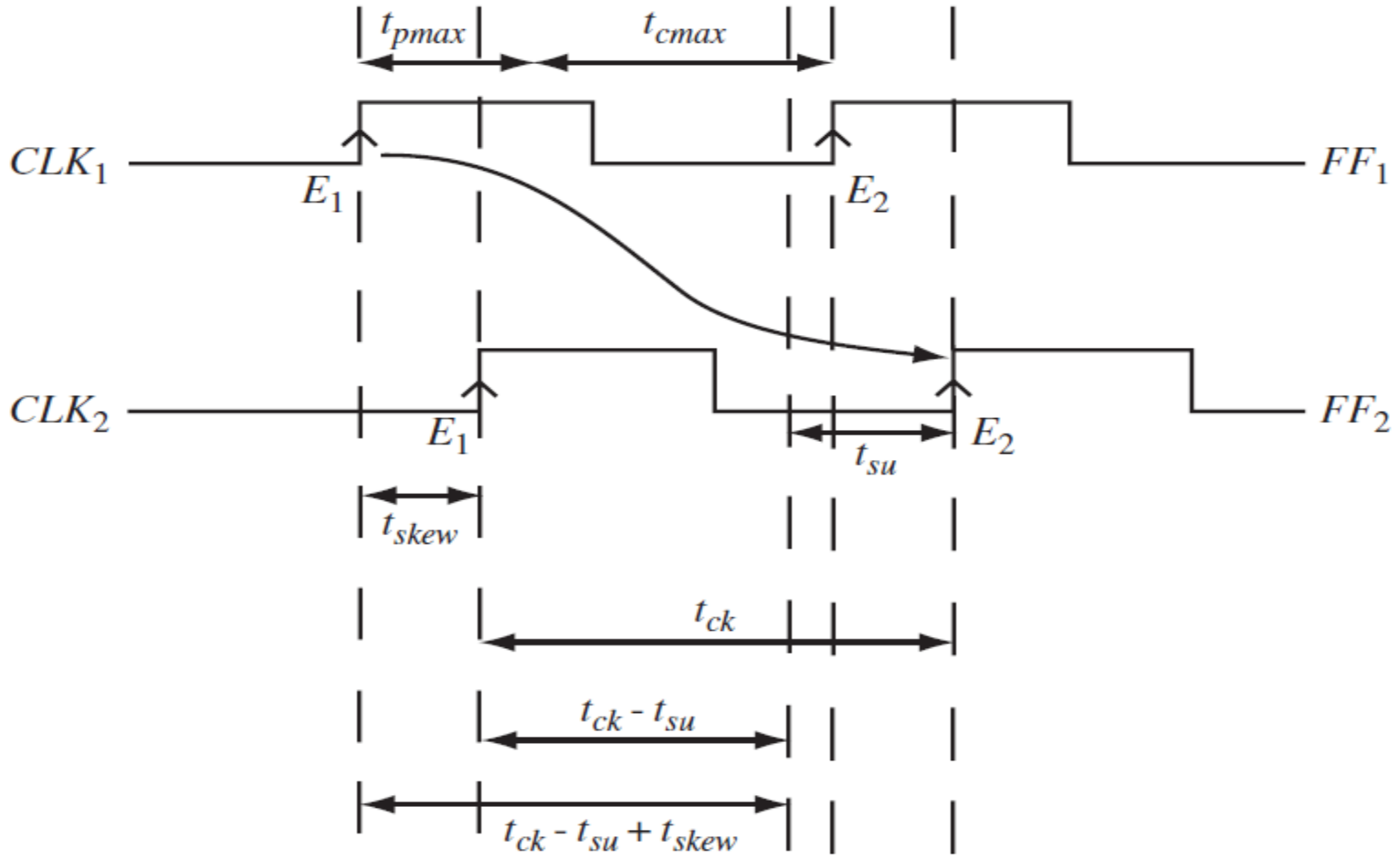
Rule No. 6: $t_{p\min} + t_{c\min} \geq t_h + t_{skew}$

Timing rules for circuits with skew



(a) Positive Skew

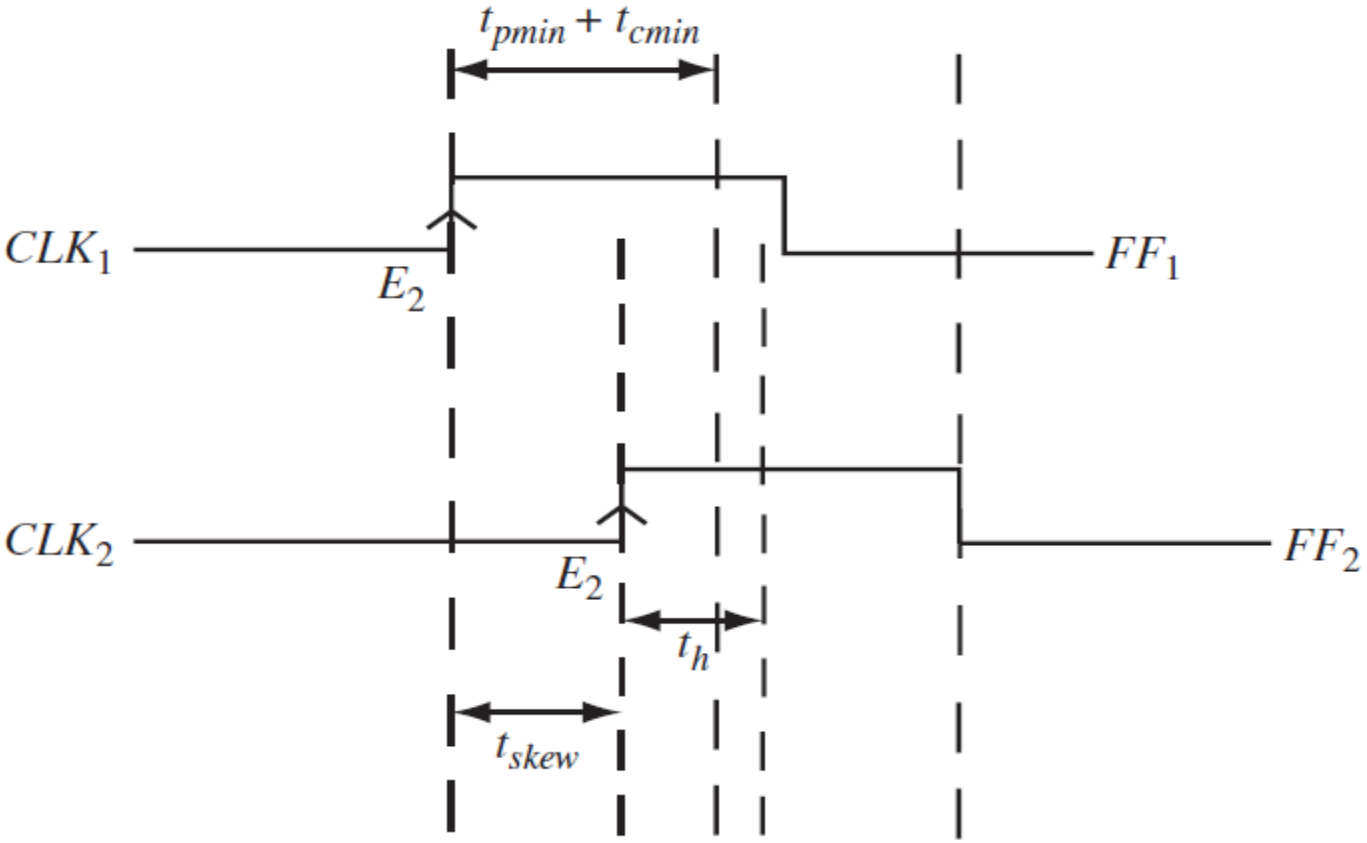
Timing rules for circuits with skew



Condition $t_{pmax} + t_{cmax} \leq t_{ck} - t_{su} + t_{skew}$ not satisfied

(b) Setup Time Violation

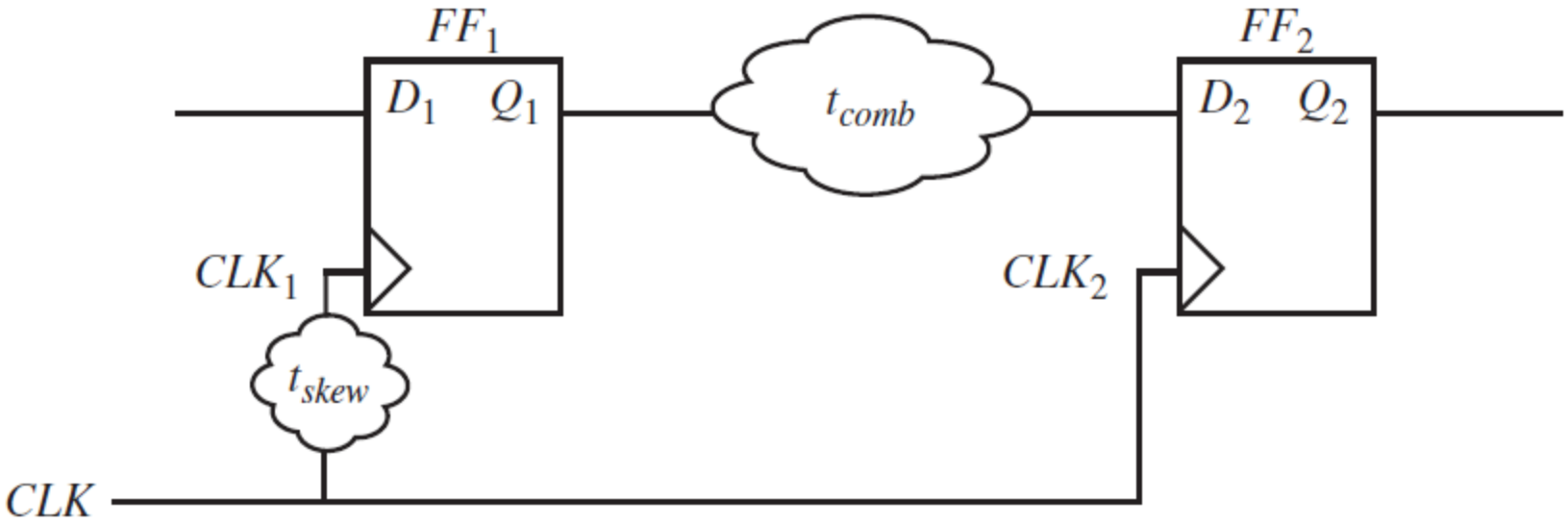
Timing rules for circuits with skew



Condition $t_{pmin} + t_{cmin} \geq t_{skew} + t_{hold}$ not satisfied

(c) Hold-Time Violation

Timing rules for circuits with skew



$$t_{ck} \geq t_{p\max} + t_{c\max} + t_{skew} + t_{su}$$

$$t_{p\min} + t_{c\min} \geq t_h - t_{skew}$$