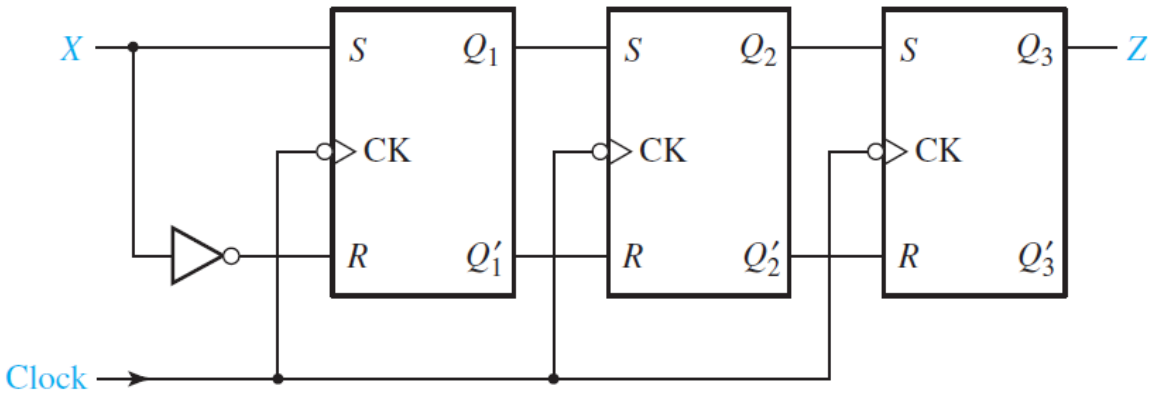
EE311 DIGITAL SYSTEM DESIGN - ASSIGNMENT 1

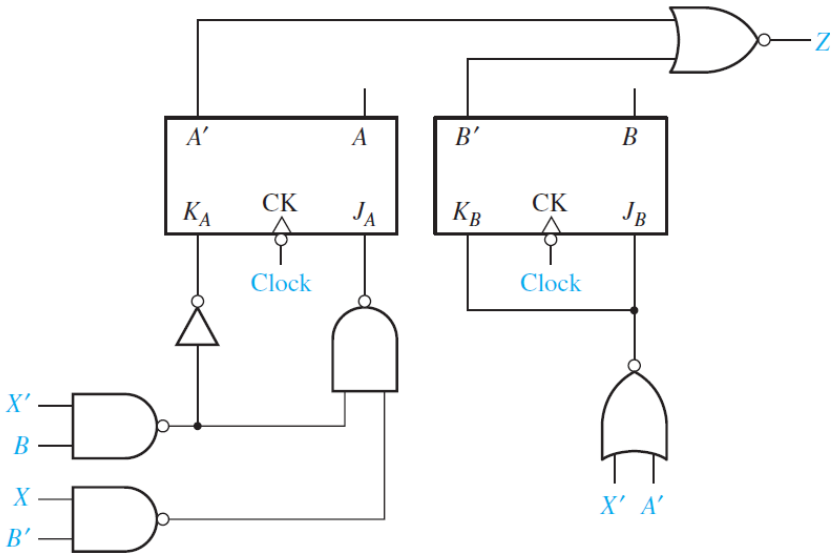
Submission due: 3rd February 2020

1. Construct a state graph for the shift register shown (X is the input, Z is the output).Is this Mealy or Moore machine?

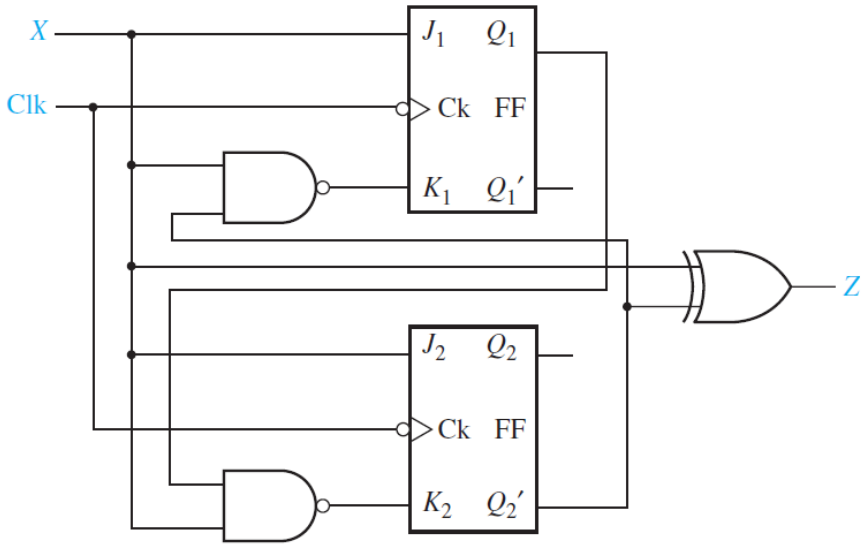


2. i. For the following sequential circuit, find the next state equation or map for each flip-flop. Is this a Mealy or Moore machine? Using these next state equations or maps, construct a state table and graph for the circuit.

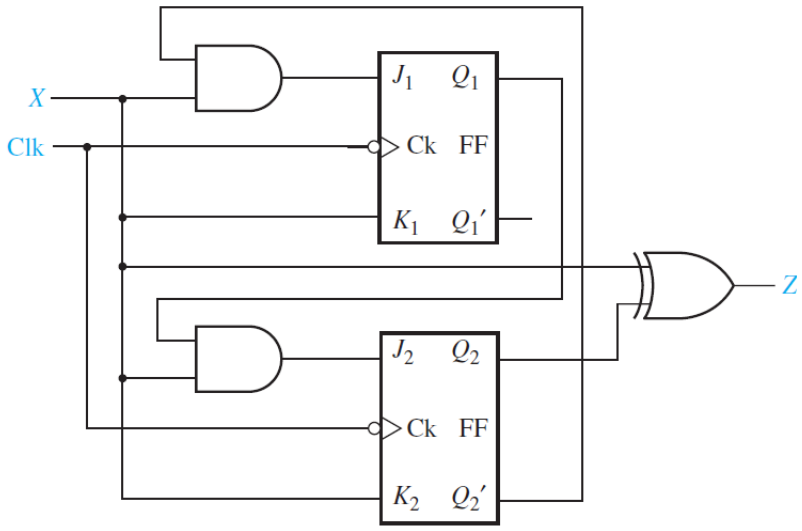
   ii. What is the output sequence when the input sequence is X = 01100? Draw the timing diagram for the input sequence X. Show the clock X, A, B and Z. Assume that the input changes between falling and rising clock edges.



3. Construct a state table and graph for the circuit shown. Construct the timing chart for an input sequence X = 10111. (Assume that initially $Q_1 = Q_2 = 0$ and that X changes midway between the rising and falling clock edges.) List the output values produced by the input sequence.



4. Construct a state table and graph for the circuit shown. Construct a timing chart for the input sequence X = 10101. (Assume that initially $Q_1 = Q_2 = 0$ and that X changes midway between the rising and falling clock edges.) Indicate the times Z has the correct value. List the output values produced by the input sequence.



5. Design a Mealy sequential circuit which investigates an input sequence X and will produce an output of Z = 1 for any input sequence ending in 0010 or 100.

   Example

X =	1	1	0	0	1	0	0	1	0	1	0	0	1	0	1
Z =	0	0	0	1	0	1	1	0	1	0	0	1	0	1	0

The circuit does not reset to start state when an output of Z = 1 occurs. Design your circuit using NAND, NOR gates and three D flip-flops. Assign 000 to the start state. Any solution which is minimal for your state assignment and uses 10 or fewer gates and inverters are acceptable. (Minimum solution requires six states).

6. Design a mealy sequential circuit which investigates an input sequence and will produce an output Z = 1 for any input sequence ending in 1101 or 011.

Example:

X _0	0	1	1	0	1	1	0	1	0	1	1	0	1	0
Z _0	0	0	1	0	1	1	0	1	0	0	1	0	1	0

The circuit does not reset to start state when an output of Z = 1 occurs. Design your circuit using NAND, NOR gates and three D flip-flops. Assign 000 to the start state. Any solution which is minimal for your state assignment and uses 9 or fewer gates and inverters are acceptable. (Minimum solution requires six states).

7. Design a sequential circuit to convert excess-3 code to BCD code. The input and output should be serial with the least significant bit first. The input X represents an excess 3 coded decimal digit and the output Z represents the corresponding BCD code. Design your circuit using D flip-flops NAND gates and NOR gates. Any solution which is minimal for your state assignment and uses 8 or fewer gates and inverters are acceptable. (000- reset state).

X				Z			
t_3	t_2	t_1	t_0	t_3	t_2	t_1	t_0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

8. For the following state table, draw the state diagram. Tabulate the reduced state table. Draw the state diagram corresponding to the reduced state table.

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

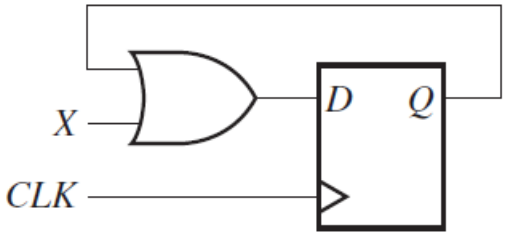
9. Draw the state diagram of a Mealy state machine that detects a sequence of three or more consecutive 1s in a string of bits coming through an input line.

10. A Moore sequential circuit has one input and one output. The output goes to 1 when the input sequence 111 has occurred and the output goes to 0 if the input sequence 000 occurs. At all other times, the output holds its value. Derive a Moore state graph and table for the circuit.

    Example

    $X = 0\ 1\ 0\ 1\ 1\ 1\ 0\ 1\ 0\ 0\ 0\ 1\ 1\ 1\ 0\ 0\ 1\ 0\ 0\ 0$
    $Z = 0\ 0\ 0\ 0\ 0\ 0\ 1\ 1\ 1\ 1\ 1\ 0\ 0\ 0\ 1\ 1\ 1\ 1\ 1\ 1\ 0$

11. A D flip-flop has a set up time of 5 ns, a hold time of 3 ns and a propagation delay from the rising edge of the clock to the change in flip-flop output in the range of 6 to 12 ns. An OR gate delay is in the range of 1 to 4 ns.
    What is the minimum clock period for proper operation of the following circuit?



What is the earliest time after the rising clock edge at which X is allowed to change?

12. In the following circuit XOR gate has a delay in the range of 2 to 16 ns. The D flip-flop has a propagation delay from clock to Q in the range 12 to 24 ns. The setup tie is 8 ns, and the hold time is 4 ns. What is the minimum clock period for proper operation of the circuit? What is the earliest and latest time after the rising clock edge at which X is allowed to change?