Varied bitwidth SERDES

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1 Description

This documentation describes a serial to parallel converter (SERDES) with varied bitwidth. It performs 600 MHz serial data transformation to 75 MHz parallel data with the bitwidths of 8, 10 and 12 bit.

This project is targeted for Artix-7 FPGA and written on VHDL. It uses an existing library element SERDES with the bitwidth of 8 bit.

This project was designed as a qualification task 1 for T871 VHDL Challenge for GSoC 2020.

2 Structure

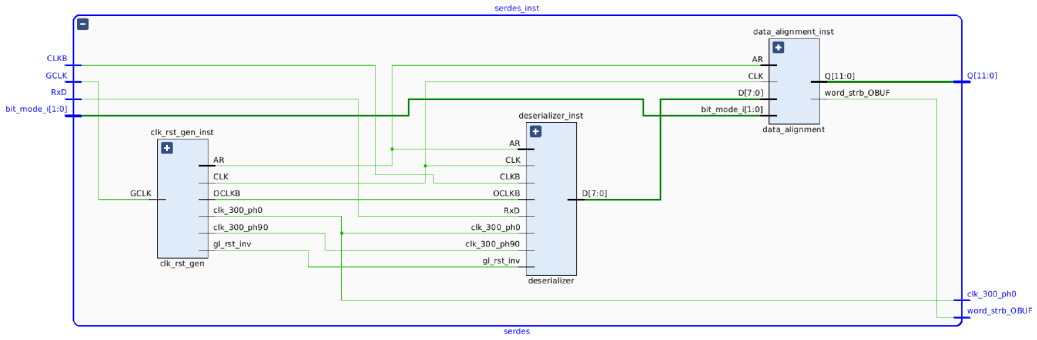

Figure 1: Top-level structure of the varied bitwidth SERDES

Fig. 1 shows the top level schematic of the project. There are three instantiated entities in the top-level module `serdes.vhd`:

- `clk_rst_gen.vhd`
- `deseriazlizer.vhd`
- `data_alignment.vhd`

Each of the modules is described in the section below.

3 Modules

- `clk_rst_gen.vhd`
  This module is responsible for the clock and global reset signals generating.
- `deseriazlizer.vhd`
  This module is responsible for the serial-parallel data transformation, and contains the Xilinx primitive ISERDESE2 configured in 8-bit mode. Although this primitive could be configured in higher bit width modes, it do not provide all required bit width values. Moreover, mode change is not available without reconfiguration.
- `data_alignment.vhd`
  This module reshapes 8-bit data received from the deseriazlizer module into properly aligned words according to the word length settings. The structure of the module is shown on Fig. 2.

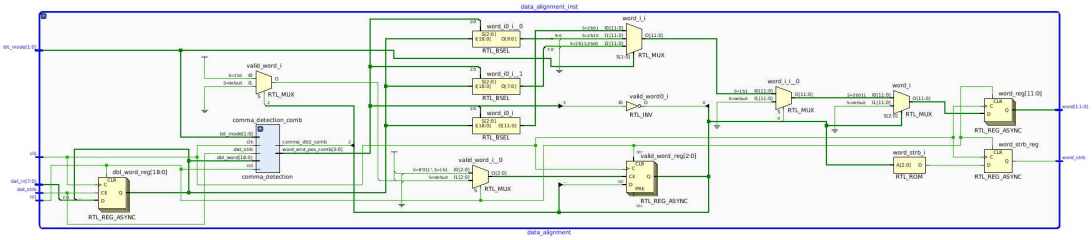

Figure 2: Schematic of the data alignment module

One of the main parts of `data_alignment.vhd` is a submodule:

  - `comma_detection`
    This submodule performs asynchronous comma detection in the 19-bit shift register, fed from the deserializer. It outputs (1) comma detection flag if the comma is detected and (2) the detected word's LSB index in the shift register. The schematic view of this submodule provided in Fig. 3.

4 Comma detection algorithm

Comma detection algorithm is aimed to find the end of the word in the data stream. This submodule inputs through `dbl_word` the last 19 received bits from the serial data line and detects the comma in form of x"BAF" in the received bits.

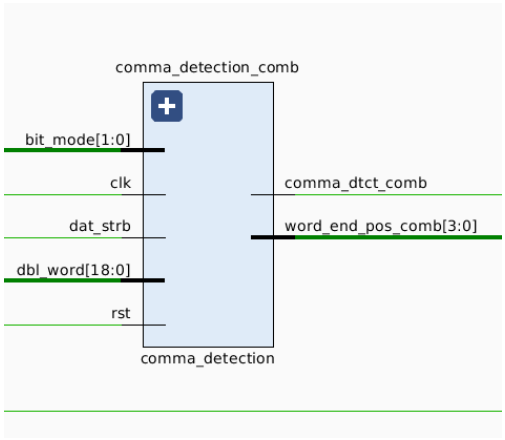

Figure 3: Structure of comma detection submodule

First detected comma means that data transfer is started. It the bitwidth is 8 bits, the comma will be x"BA" , if it is 10 bits the comma will be x"2EB", if the bidwidth is 12 bit - the comma is x"BAF".

The `comma_detection_comb` submodule outputs signal `comma_dtct_comb` which means that comma is detected and the data transfer started.

The bus `word_end_pos_comb` is used for sending a bit number of the last significant bit in the word. This bit is used later in the `data_alignment` module for words separation.

5 Summary

The serial to parallel converter (SERDES) with varied bitwidths was designed, simulated and synthesized on Artix-7 FPGA.

6 References

The $H_I T_E C$ class by Eli Billauer was used for designing this documentation.