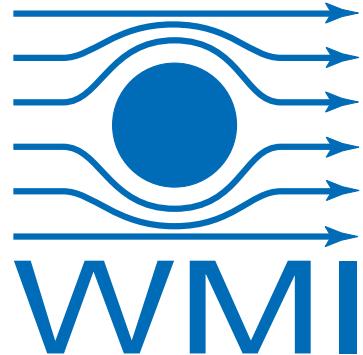


TECHNISCHE
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Akademie der Wissenschaften

Design and characterization of a superconducting beam-splitter for quantum information processing

Diploma Thesis

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TECHNISCHE UNIVERSITÄT MÜNCHEN

Foremost, I want to dedicate this thesis to my wonderful family. They supported me throughout my whole life, and I know it wasn't always easy. It is also in memory of my grandfather, whose absence lies like a shadow on everyday life.

Erklärung / Declaration of Originality

Mit der Abgabe der Diplomarbeit versichere ich, dass ich die Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

By submission of this thesis I hereby certify, that this diploma thesis is my own work and no sources other than the ones given have been used.

Garching, 18. Dezember 2013

Ort, Datum

Ferdinand Loacker

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Chapter 1

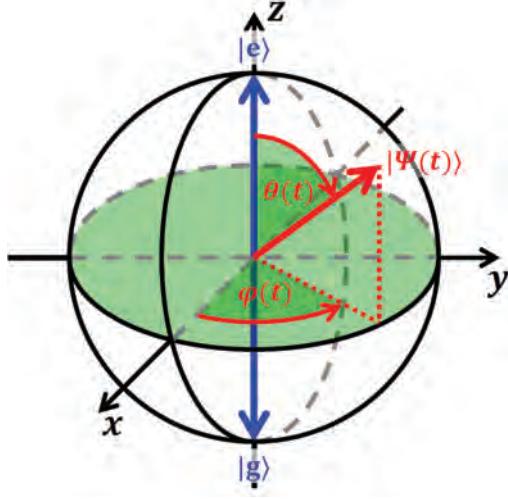
Introduction

Quantum computation has the potential to perform certain computational tasks so efficient, that modern super computers perform like pocket calculators in comparison. However, this does not mean that they are suited for every possible task. The performance is only superior for certain applications, including factorization and decryption. In the context of fundamental research, quantum computers are believed to be relevant because of their ability to efficiently simulate complex quantum systems. This idea was originally suggested by Richard Feynman in 1982 [1] and David Deutsch showed in 1985 that theoretically any physical process could be simulated this way [2].

For a regular computer that relies solely on the two possible states of a classical bit, 0 and 1, computation time increases exponentially with the size of the problems mentioned above. In contrast, a quantum algorithm reduced this scaling to a polynomial law by making explicit use of quantum mechanics on the level of the underlying logic¹. A visual depiction of a quantum bit (*qubit*) is conveniently obtained by the *Bloch sphere* representation, where all possible superposition states of a quantum two-level system with the basis states $|0\rangle$ and $|1\rangle$ are located on the surface of the sphere. As we can see in Fig. 1.1, the qubit state $|\Psi\rangle$ is then represented by the Bloch angles θ (amplitude) and ϕ (phase). In combination with the quantum property of entanglement, this (with respect to the two states of a classical bit) greatly extended computational space forms the basis of the potential speedup achievable by quantum algorithms.

One specific implementation possibility is described in the following: circuit quantum electrodynamics (cQED) [4]) was suggested by Blais in 2004 [5] and first experimentally verified soon after that [4, 6]. In cQED, *qubits* are coupled to (quasi) one-dimensional microwave resonators (CPW structures) with superconducting materials in order to minimize environment-induced losses. These structures are macroscopic in size, since the typical frequency of operation is in the order of several gi-

¹Whereas for the computation of a quantum mechanical system with n two-level systems n^n classical bits are necessary, a quantum computer only requires the employment of n qubits.



$$|\Psi(t)\rangle = \cos\left(\frac{\theta(t)}{2}\right)|e\rangle + e^{i\varphi(t)}\sin\left(\frac{\theta(t)}{2}\right)|g\rangle$$

Figure 1.1: Bloch sphere representation of a *qubit* taken from Ref. [3] (with the two states *ground* $|g\rangle \equiv |0\rangle$ and *excited* $|e\rangle \equiv |1\rangle$).

gahertz, corresponding to several mm long resonators². The superconducting qubits are Josephson-junction-based circuits [7] and act as ‘artificial atoms’ (matter) via the resonator, this quantum matter can interact with microwave light (photons). The information of the system can now be shared or transferred between *qubit* and photon, which can leak out of the resonator. Such a propagating photon itself can act as an information carrier, an approach that was formerly exclusive to quantum optics [8].

The utilization of microwave photons for quantum information processing includes several benefits. They have good coherence properties in superconducting waveguide structures and are naturally bound to distribute quantum information. Furthermore, superconducting circuits can mediate strong interactions between them which should allow for deterministic gates. Consequently, the young field of propagating quantum microwaves is gaining increasing popularity for quantum computation and quantum simulation.

The ability to combine and split propagating waves is a necessity for these tasks and can be achieved through passive components such as the quadrature hybrid which acts as a beam splitter for the microwave photons [9]. It features a scalable port configuration in the sense that a planar interferometer can be constructed from two adjacent hybrids on a single chip without crossing microwave lines.

In this work, this fundamental linear element (the *quadrature 90° hybrid*) is measured and its properties are examined. In addition, the sample package enclosing the device is analyzed and optimized.

²The typical energy gap of a *qubit* is 5 GHz and the *hybrid-ring* has to be designed/matched accordingly.

The thesis is structured as follows: Chapter 2 gives insight into the relevant microwave theory. In Ch. 3, an overview of sample package and measurement setup are presented. Chapter 4 is divided in two parts. In the first section, critical connections between the various components of the sample package are examined and optimized, while the second part employs the achieved accomplishments in an analysis of the *beam splitter*. In Ch. 5, the results (of this thesis) are summarized and an outlook on the future development is given.

Chapter 2

Microwave fundamentals

This chapter presents the theoretical foundations relevant for the design of microwave circuits and devices. First, the geometry of coplanar waveguide transmission lines (CPW) is presented in Sec. 2.1. The scattering parameters are introduced in Sec. 2.2. One possible application, the quadrature (90°) hybrid examined during this thesis, is discussed in Sec. 2.3.

2.1 Coplanar waveguides

A coplanar waveguide is a particular type of a planar microwave transmission line. It commonly consists of a center strip conductor amidst two ground planes ontop a dielectric substrate. It was originally developed by C. P. Wen in 1969 [10]. One advantage of CPWs is their design flexibility, allowing for a significant amount of freedom in the choice of the widths of both center conductor and the gaps to the ground plane. As we will see later, typically only the ratio of these two quantities is fixed. Application in classical microwave engineering range from amplifiers and printed antennas to switches [11].

In this section, the main characteristics of CPWs are discussed and their derivation is presented following Ref. [11, 12]. First, the double-layer CPW is analyzed. This is an extended version of the original design, capable of characterizing a sample with two different substrates of finite thickness. Figure 2.1 shows the schematic composition of such a CPW structure with metal covers, a top substrate layer with thickness h_2 and dielectric constant ϵ_{r2} and a second one at the bottom with hight $h_1 - h_2$ and dielectric constant ϵ_{r1} . The distances to the metal covers are h_3 or h_4 respectively and thickness of the textured metal layer is t . This general approach allows for analyzing a chip placed in a PCB, a setup that is used for several experiments in this thesis, by considering the dielectric constants of both components. In addition, the PCB can be examined by itself with the appropriate parameters, setting $\epsilon_{r1} = 1$ and therefore eliminating the partial capacitance C_2 presented in Fig. 2.2 and only calculating a CPW on a single substrate.

The charactersitic parameters of a CPW are the effective dielectric constant ϵ_{eff} and

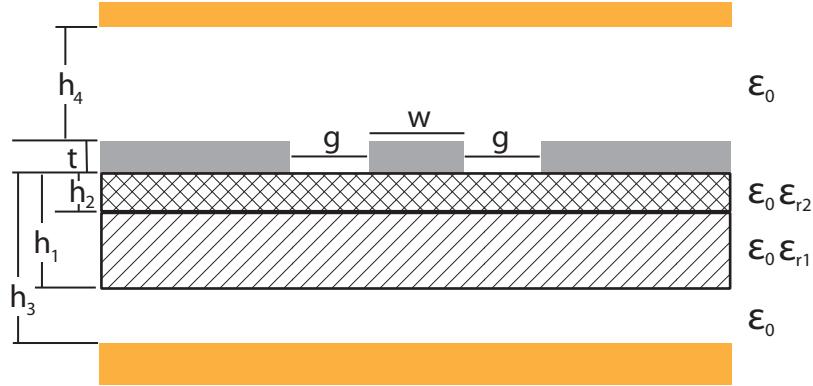


Figure 2.1: Schematic of CPW on double-layer dielectric substrate; adapted version from Ref. [11].

the characteristic impedance Z_0 . They are determined through conductor properties such as its dimensions (width w , gap g and thickness t) and the dielectric substrates (thickness h_i with dielectric $\epsilon_0\epsilon_{ri}$). For this analysis, the conductor is assumed to be lossless. For superconducting materials [13] (perfect conductivity), this assumption should be appropriate and copper is an excellent conductor as well. At this point, the ground planes are of infinite width and the substrate is considered isotropic. A quasi-static approach is utilized to determine the potential in order to calculate the capacitances (using conformal mapping techniques). Usually, the determination is conducted with a full-wave analysis, a complicated process that requires excessive amounts of computing capacity (and time) [14] because of the retarded potential. One possible solution is the employment of analytic formulas in a quasi-static approximation, a technique that achieves good results [15]. According to Ref. [16], one aspect of the quasi-static approximation is that the propagation mode in the transmission lines is a pure transverse electromagnetic modes (TEM). This circumstance concerns the relation of wavelength (λ) and structure dimensions (d) such as w and g . If d is diminutive in comparison to λ , usually fulfilled for frequencies below 10 GHz and the utilized chip designs in particular, the longitudinal field components are significantly smaller than transversal ones. The main principle of this approximation is that for high velocities the change of the self-induced influenced of the retarded potential is slow compared to the velocity (the system is in an equilibrium).

To analyze the CPW from Fig. 2.1, it is first devide into several parts that are examined separately as seen in Fig. 2.2. The electric fields are assumed to be only in the appropriate region.

$$C_{\text{CPW}} = C_{\text{air}} + C_1 + C_2. \quad (2.1)$$

Following the Veyers-Fouad Hanna approximation [15], the total capacitance of the CPW (C_{CPW}) is a superposition of the partial capacitances of these regions.

C_{air} is examined first, giving the capacitance between the plane containing center strip conductor and ground planes and the top and/or bottom metal covers.

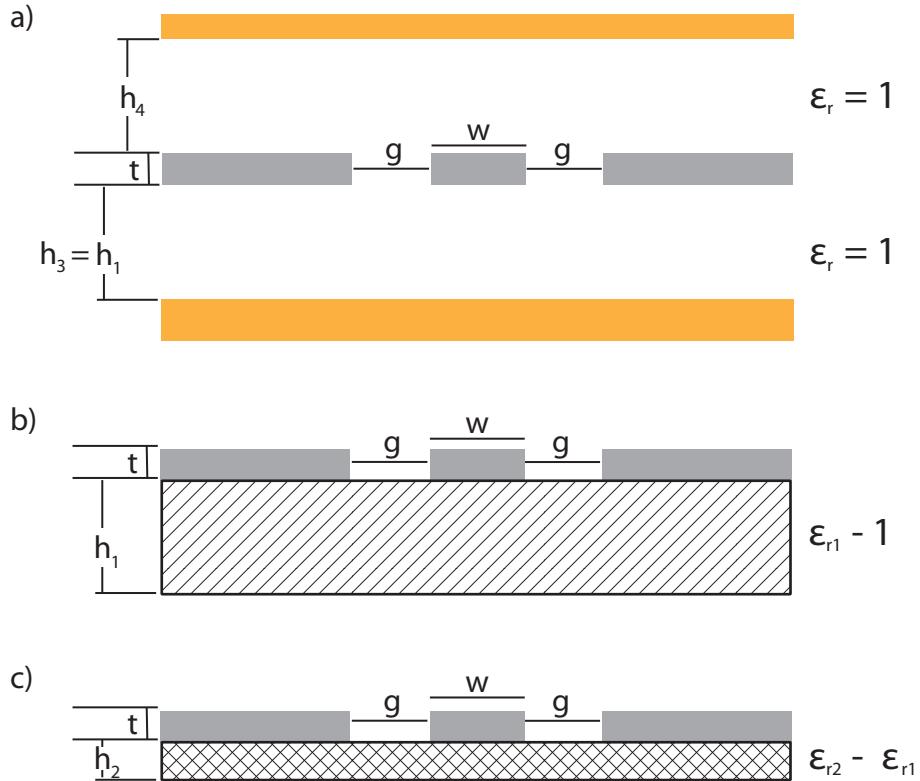


Figure 2.2: Schematic for partial capacitances: **a)** C_{air} , **b)** C_1 , **c)** C_2 .
Adjusted illustration taken from Ref. [11].

The space between these layers is filled with air ($\epsilon_r = 1$). It is defined as:

$$C_{\text{air}} = 2\epsilon_0 \frac{K(k_3)}{K(k'_3)} + 2\epsilon_0 \frac{K(k_4)}{K(k'_4)}, \quad (2.2)$$

where K is the complete elliptical integral of the first kind. The arguments k and k' are dependent on the geometry:

$$k_i = \frac{\tanh\left(\frac{\pi w}{4h_i}\right)}{\tanh\left(\frac{\pi(w+2g)}{4h_i}\right)} \quad (2.3)$$

$$k'_i = \sqrt{1 - k_i^2}, \quad i = 3 \text{ or } 4 \quad (2.4)$$

The top metal cover represents the box where the PCB is placed, while the layer at the bottom in our case refers to the conductor backed coplanar waveguide (CBCPW). The CBCPW is presented later in this section since some adjustments have to be considered. According to Ref. [17], an approximation for the complete elliptic integrals can be given for arbitrary k_i .

If $0 < k \leq 1/\sqrt{2}$, the approximation takes the following form with $m = k^2$:

$$\frac{K(k)}{K(k')} = -\pi \left[\ln\left(\frac{m}{16} + 8\left(\frac{m}{16}\right)^2 + 84\left(\frac{m}{16}\right)^3 + \dots\right) \right]^{-1}, \quad (2.5)$$

while for $1/\sqrt{2} \leq k < 1$, this equation is utilized with $m_1 = 1 - k^2$:

$$\frac{K(k)}{K(k')} = -\frac{1}{\pi} \left[\ln \left(\frac{m_1}{16} + 8 \left(\frac{m_1}{16} \right)^2 + 84 \left(\frac{m_1}{16} \right)^3 + \dots \right) \right]. \quad (2.6)$$

The expressions for the other (partial) capacitances as depicted in Fig. 2.2 are:

$$C_1 = 2\epsilon_0(\epsilon_{r1} - 1) \frac{K(k_1)}{K(k'_1)}, \quad (2.7)$$

with

$$k_1 = \frac{\sinh \left(\frac{\pi w}{4h_1} \right)}{\sinh \left(\frac{\pi(w+2g)}{4h_1} \right)}, \quad (2.8)$$

$$k'_1 = \sqrt{1 - k_1^2}. \quad (2.9)$$

For C_2 , the equation is as follows:

$$C_2 = 2\epsilon_0(\epsilon_{r2} - \epsilon_{r1}) \frac{K(k_2)}{K(k'_2)}, \quad (2.10)$$

with

$$k_2 = \frac{\sinh \left(\frac{\pi w}{4h_2} \right)}{\sinh \left(\frac{\pi(w+2g)}{4h_2} \right)} \quad (2.11)$$

and

$$k'_2 = \sqrt{1 - k_2^2}. \quad (2.12)$$

Substituting the Eqs. (2.2), (2.7) and (2.10) into Eq. (2.1) gives for the capacitance C_{CPW} :

$$C_{\text{CPW}} = 2\epsilon_0 \left[\left(\frac{K(k_3)}{K(k'_3)} + \frac{K(k_4)}{K(k'_4)} \right) + (\epsilon_{r1} - 1) \frac{K(k_1)}{K(k'_1)} + (\epsilon_{r2} - \epsilon_{r1}) \frac{K(k_2)}{K(k'_2)} \right]. \quad (2.13)$$

An expression for ϵ_{eff} under quasi-static approximation is:

$$\epsilon_{\text{eff}} = \frac{C_{\text{CPW}}}{C_{\text{air}}}. \quad (2.14)$$

With the equations for C_{air} (2.2) and C_{CPW} (2.13), ϵ_{eff} can be converted to:

$$\epsilon_{\text{eff}} = 1 + q_1(\epsilon_{r1} - 1) + q_2(\epsilon_{r2} - \epsilon_{r1}). \quad (2.15)$$

where the partial filling factors q_1 and q_2 are defined as follows:

$$q_1 \equiv \frac{K(k_1)}{K(k'_1)} \frac{2\epsilon_0}{C_{\text{air}}}, \quad (2.16)$$

$$q_2 \equiv \frac{K(k_2)}{K(k'_2)} \frac{2\epsilon_0}{C_{\text{air}}}. \quad (2.17)$$

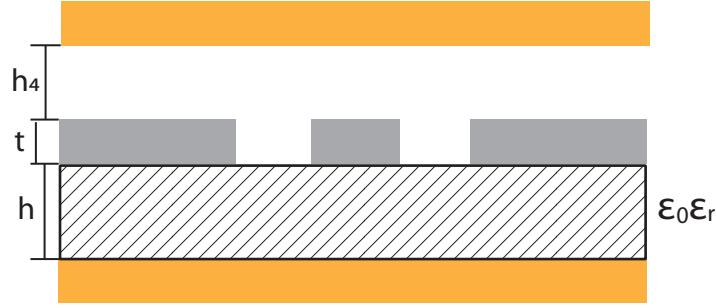


Figure 2.3: Schematic for CBCPW with top metal cover on a dielectric substrate taken from Ref. [11].

This leads to the expression for the characteristic impedance Z_0 :

$$Z_0 = \frac{1}{C_{\text{CPW}} v_{\text{ph}}} = \frac{1}{c C_{\text{air}} \sqrt{\epsilon_{\text{eff}}}}, \quad (2.18)$$

using

$$v_{\text{ph}} = \frac{c}{\sqrt{\epsilon_{\text{eff}}}} \quad (2.19)$$

with the velocity of light in free space c .

The PCB used in this thesis has a particular design, namely a CBCPW. However, identifying the conductive layer at the bottom with the real ground plane of a CBCPW is not entirely correct. In the following discussion, the differences are emphasized. For a first overview, only one dielectric (ϵ_r) of thickness h is considered. Figure 2.3 illustrates the appropriate schematic. The distance to the top metal cover remains h_4 .

The effective dielectric constant ϵ_{eff} now fulfills the following equation:

$$\epsilon_{\text{eff}} = 1 + q(\epsilon_r - 1), \quad (2.20)$$

where

$$q = \frac{\frac{K(k_3)}{K(k'_3)}}{\frac{K(k_3)}{K(k'_3)} + \frac{K(k_4)}{K(k'_4)}} \quad (2.21)$$

$$k_i = \frac{\tanh\left(\frac{\pi w}{4h_i}\right)}{\tanh\left(\frac{\pi(w+2g)}{4h_i}\right)}, \text{ with } h_i = h \text{ for } k_3 \text{ and } h_i = h_4 \text{ for } k_4, \quad (2.22)$$

$$k'_i = \sqrt{1 - k_i^2}, \quad i = 3 \text{ or } 4. \quad (2.23)$$

This expression for ϵ_{eff} resembles Eq. (2.15) when $\epsilon_{r2} = 1$ (and for $h_2 = 0$), thus h equals h_1 and $\epsilon_r = \epsilon_{r1}$. Although, the filling factor q has changed. Comparing q to

q_2 [Eq. (2.16)] for $h = h_1 = h_3$ exemplifies the difference:

$$\frac{q}{q_1} = \frac{\operatorname{sech}\left(\frac{\pi w}{4h_i}\right)}{\operatorname{sech}\left(\frac{\pi(w+2g)}{4h_i}\right)} \quad (2.24)$$

using the expression for the hyperbolic secant

$$\frac{1}{\cosh(x)} = \operatorname{sech}(x). \quad (2.25)$$

Considering a second substrate C_2 [Eq. (2.10)], it is again assumed that the electric field is only present in the appropriate regions (see Fig. 2.2). Therefore, C_1 is unaffected as in Eq. (2.7) and C_2 remains identical to Eq. (2.10). Hence ϵ_{eff} for a double-layer CBCPW is given by:

$$\epsilon_{\text{eff}} = 1 + q(\epsilon_r - 1) + q_2(\epsilon_{r2} - \epsilon_{r1}), \quad (2.26)$$

with the partial filling factors q from Eq. (2.21) and q_2 given by Eq. (2.17).

The finite dimensions of the ground plane must also be considered, especially in the case of PCB and chip. First, the partial capacitance concept is extended for C_{air} [Eq. (2.2)] by adding the new region C_0 , giving the capacitance between center strip conductor and ground planes in their layer of thickness t :

$$C_0 = 4\epsilon_0 \frac{K(k)}{K(k')} \quad (2.27)$$

with

$$k = \frac{c}{b} \sqrt{\frac{b^2 - a^2}{c^2 - a^2}}, \quad (2.28)$$

where $a = w/2$, $b = a + g$ and $c = (w/2) + g + d$ with d being the width of the ground planes.

Then, the expressions for the other k , k_i has to be adjusted as follows:

$$k_i = \frac{\tanh\left(\frac{\pi c}{2h_i}\right)}{\tanh\left(\frac{\pi b}{2h_i}\right)} \sqrt{\frac{\tanh^2\left(\frac{\pi b}{2h_i}\right) - \tanh^2\left(\frac{\pi a}{2h_i}\right)}{\tanh^2\left(\frac{\pi c}{2h_i}\right) - \tanh^2\left(\frac{\pi a}{2h_i}\right)}} \quad (2.29)$$

with substituting sinh for tanh in the case of C_2 . The expression for k' and every k'_i is allways given by:

$$k' = \sqrt{1 - k^2} \quad (2.30)$$

With these last equations, every component of the real sample package (Sec. 3.2) is covered by our discussion: The possible presence or absence of a chip in form of a double-layer CPW, the immediate conductor backing of a CBCPW and the

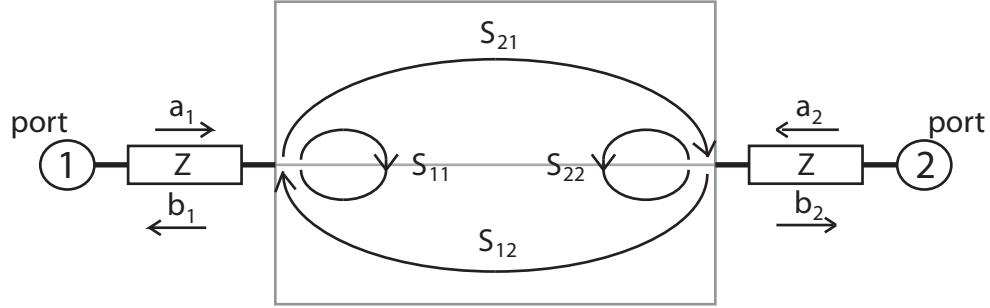


Figure 2.4: Illustration from Ref. [18] of a two port model, denominating and explaining the appropriate S-parameters. The reflection at a port is also denoted as Γ , for example at port 1 with $S_{11} = \Gamma$.

finite dimensions of the of ground planes (FWCPW). With the presented equations it is possible to determine the design parameters for width and gap to match a characteristic impedance of generally 50Ω , a standard value of microwave equipment. Width and gap are very adjustable and for a fixed value for one of these parameters, the other one can be calculated for a given characteristic impedance.

2.2 Scattering parameters

In this section, the scattering parameters (or S-parameters) are explained assuming a lossless network. An illustration to designate them is shown in Fig. 2.4. For a two-port device, the S-parameters are definded as described in Ref. [18] and their expression is in accordance with the general approach for a N -port network presented in Ref [12]:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \quad (2.31)$$

The independent variables a_i ($i = 1, 2$ denotes the port) are normalized *incident* voltages (V_i^+)and the dependent factors b_i the normalized *reflected* voltages (V_i^-). At first, port 1 is excited with no incident wave at port 2, thus setting $a_2 = 0$. Under the assumptions of a termination of matched characteristic impedance Z at port 2 and a lossless network, no power is lost. Therefore, the input reflection coefficient S_{11} can be calculated according to Eq. (2.31):

$$S_{11} = \frac{V_1^-}{V_1^+}, \quad (2.32)$$

The forward voltage gain S_{21} (or transmission from port 1 to port 2) is given by:

$$S_{21} = \frac{V_2^-}{V_1^+}, \quad (2.33)$$

Similarly, for an incident wave at port 2 with the appropriate setup one gets:

$$S_{22} = \frac{V_2^-}{V_2^+}, \quad (2.34)$$

and

$$S_{12} = \frac{V_1^-}{V_2^+}. \quad (2.35)$$

S-parameters are usually given in decibel (dB):

$$S_{ij}[\text{dB}] = -20 \log_{10} |S_{ij}|. \quad (2.36)$$

With the quadrature value of a scattering parameter $|S_{ij}|^2$, the relation for power is given instead of voltages.

2.3 The quadrature (90°) hybrid

In this section, the standard quadrature hybrid, also known as 90° hybrid ring or branch-line hybrid/coupler, is discussed following Ref. [11, 12]. The device acts as a 3 dB beam splitter. When a signal is incident on port 1 (2,3,4), it is divided equally (3 dB) into the “direct” port 2 (1,4,3) and the “coupled” port 3 (4,1,2). The remaining port 4 (3,2,1) is isolated, i.e., there is no outgoing voltage. First, an overview of the general design and the important parameters is presented. Then the scattering matrix of the device is calculated using even-odd-mode analysis. The hybrid ring is assumed to be lossless and an illustration of the actual layout can be found in Sec. 4.2.

An equivalent circuit model of the quadrature hybrid is shown in Fig. 2.5. This illustration also contains important design information concerning the four sections of the hybrid, the two through lines and the two branch lines.

Since the structure is very symmetric, S can be simplified as shown in Eq. (2.37). For an ideal device, the entire matrix can be expressed in terms of the S-parameters S_{i1} :

$$S = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{21} & S_{31} & S_{41} \\ S_{21} & S_{11} & S_{41} & S_{31} \\ S_{31} & S_{41} & S_{11} & S_{21} \\ S_{41} & S_{31} & S_{21} & S_{11} \end{bmatrix} \quad (2.37)$$

To determine the entries of the first column (S_{i1} with $i = 1, 2, 3, 4$), the symmetry of the hybrid ring is utilized, allowing for an even-odd-mode analysis¹. It describes the propagation of an electromagnetic wave along a CPW as the superposition of the two normal modes responses even and odd. For the case of the hybrid ring, an input of intensity I applied at port 1 is therefore divided into two equal ones ($+I/2$) at the ports 1 and 4 for the even mode and $+I/2$ at port 1 and $-I/2$ at port 4 for the odd mode. When combined, the superposition results in a total input at port 1 of I and 0 at port 4 as intended. Figure 2.6 illustrates this excitation. The

¹Usually, this method is employed for CPWs which are in close proximity so that their electromagnetic fields can interact, observed through power coupling in between them.

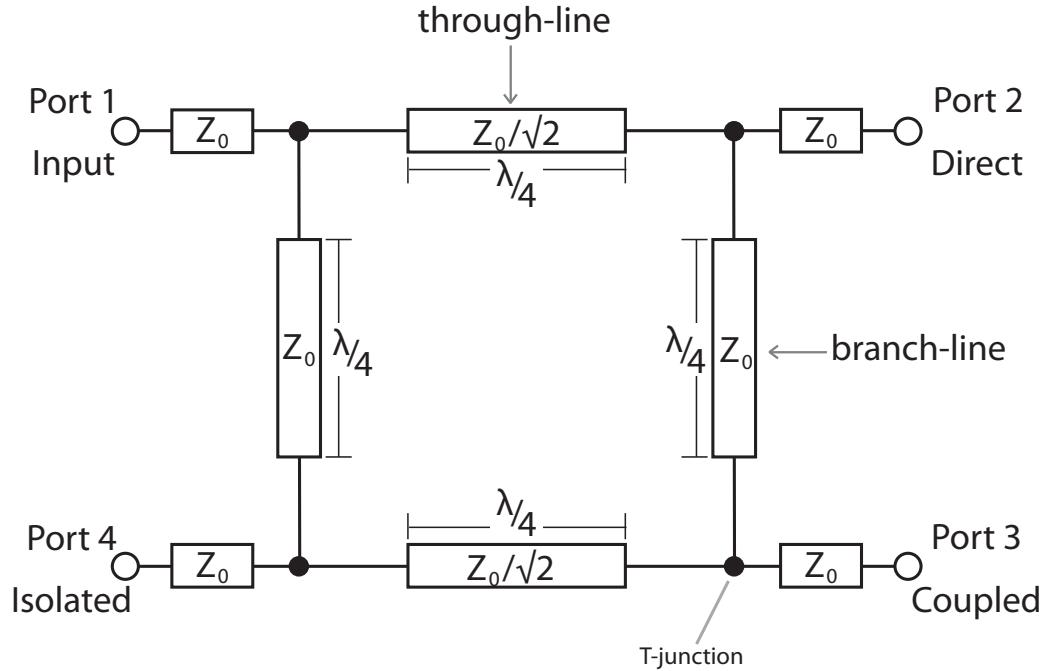


Figure 2.5: Illustration of equivalent circuit model of the quadrature hybrid, taken from Ref. [11]. Z_0 is the characteristic impedance of the input and output lines and λ refers to the working frequency of the device. $\lambda/4$ also determines the physical dimensions of the hybrid ring.

advantage of this technique is that through the symmetric application of sources, the already symmetric structure of the hybrid ring can be divided into two identical sub-circuits at the symmetrical plane while the information of the excluded section remains in the form of the boundary condition that is determined through the type of termination (for example an open termination for the even mode) [19]. Therefore, it is sufficient to analyse one sub-circuit while retaining all the relevant information. The actual branch-line hybrid presented in Fig. 2.5 is first divided into two identical halves, utilizing the symmetry of the structure as seen in Fig. 2.7. The excitation of one port (or input voltage V) is divided in even (or symmetric) and odd (anti-symmetric) excitations. For the even mode, there is the voltage V at both sides of the symmetry axis, a so-called magnetic wall, and an electric wall in the case of the odd mode where the voltages have an identical amplitude $|V|$ but show a switched sign. Splitting the circuit along this axis is equivalent to an open termination (even-mode) or short termination (odd-mode) respectively. Additional splitting (along the symmetry axis) of the remaining circuit further reduces the structure that can in turn be excited with an even- and odd-mode as shown in Fig. 2.8. This simplifies the calculation while retaining a complete description of the quadrature hybrid. In conclusion, there is only one port left with 4 modes that can be analyzed separately while preserving circuit symmetry: the T-junction. The planes of symmetry become virtual short or open terminations respectively. Using superposition, the final result is a coherent summation of these results following Ref. [20].

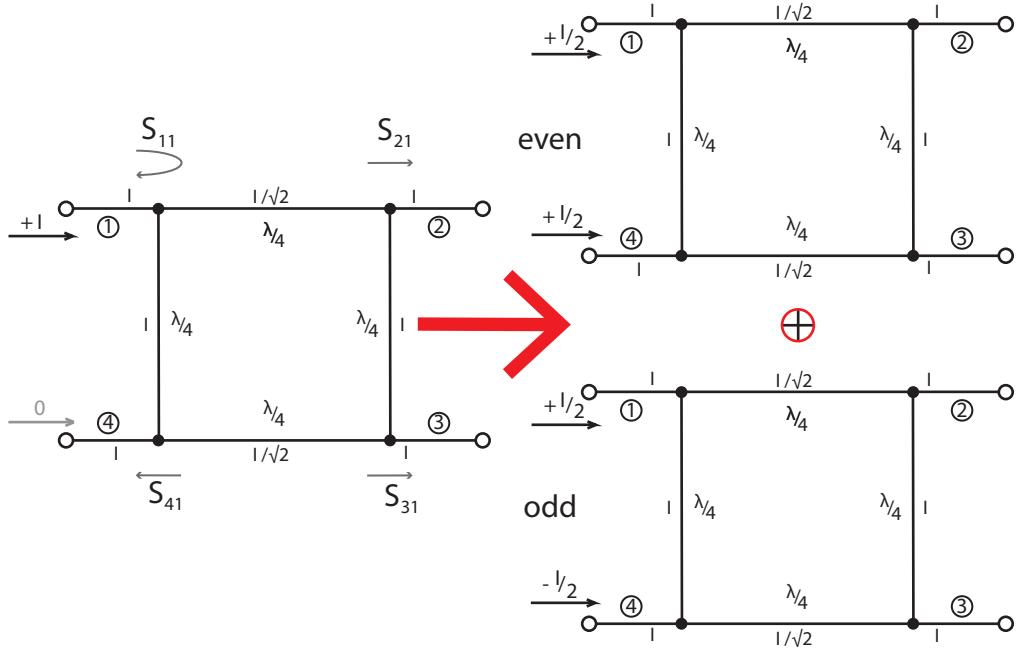


Figure 2.6: Division of an excitation at port 1 (with corresponding scattering parameters) in a superposition of even- and odd-mode excitations at the ports 1 and 4.

The equations for the scattering parameters S_{i1} ($i = 1, 2, 3, 4$) are defined by Ref. [21] as follows:

$$S_{11} \equiv \frac{1}{2}(b_{1e} + b_{1o}), \quad (2.38)$$

$$S_{21} \equiv \frac{1}{2}(b_{2e} + b_{2o}), \quad (2.39)$$

$$S_{31} \equiv \frac{1}{2}(b_{2e} - b_{2o}), \quad (2.40)$$

$$S_{41} \equiv \frac{1}{2}(b_{1e} - b_{1o}). \quad (2.41)$$

The values for b_{ie} ($i = 1, 2$) are obtained by analyzing Fig. 2.8 a) and c), while b_{io} ($i = 1, 2$) is calculated employing the illustration shown in b) and d). b_{1e} can be understood as b_{ee} while b_{2e} corresponds to b_{oe} and so forth, using the same analogy for Fig. 2.8. According to Ref. [12, 22], their values are defined through the reflection coefficients Γ_n and Γ'_n ($n = e, o$) which are illustrated in Fig. 2.8:

$$b_{1e} = \frac{\Gamma_e + \Gamma_o}{2}, \quad (2.42)$$

$$b_{2e} = \frac{\Gamma_e - \Gamma_o}{2}, \quad (2.43)$$

$$b_{1o} = \frac{\Gamma'_e + \Gamma'_o}{2}, \quad (2.44)$$

$$b_{2o} = \frac{\Gamma'_e - \Gamma'_o}{2}. \quad (2.45)$$

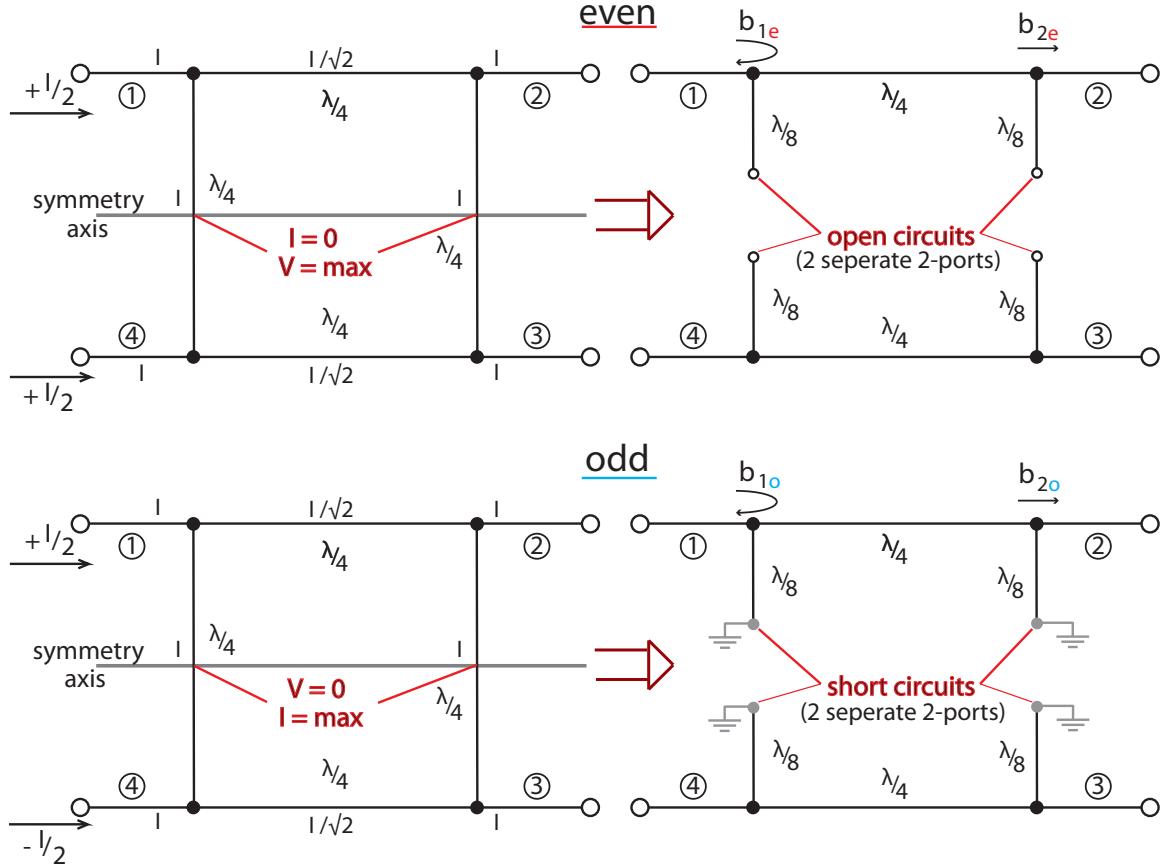


Figure 2.7: Decomposition of the quadrature hybrid into even- and odd-mode excitations. Accordingly, new reflection (b_{1j}) and transmission coefficients (b_{2j} with $j = e, o$) are defined for both modes of this two-port circuit. Adapted illustration taken from Ref. [12].

They are calculated with the complex input admittance Y_{in} . The appropriate expressions are dependent on the termination and given by:

$$Y_{\text{in}} = iY_0 \tan(\beta l) \quad (2.46)$$

for open and

$$Y_{\text{in}} = -iY_0 \cot(\beta l) \quad (2.47)$$

for short terminations, where Y_0 is the characteristic admittance of the circuit component with characteristic impedance Z_0 (following $Y_i(Z_i) \equiv 1/Z_i$), electrical length l and the wavenumber β . With the circuits presented in Fig. 2.8, Y_{in} can be simplified by using $l = \lambda/8$ and with

$$\beta l = \frac{2\pi}{\lambda} \frac{\lambda}{8} = \frac{\pi}{4}, \quad (2.48)$$

one obtains

$$\tan(\beta l) = \cot(\beta l) = 1. \quad (2.49)$$

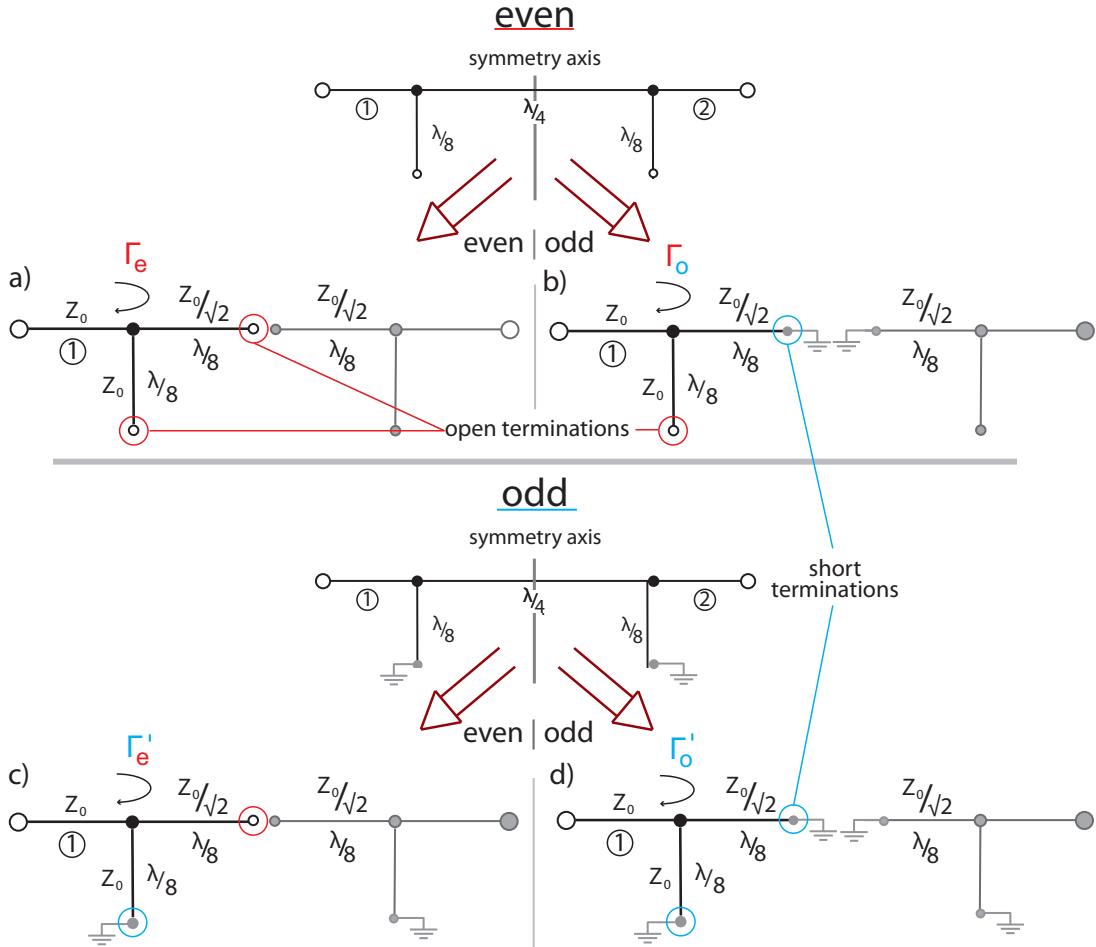


Figure 2.8: Further dividing of the quadrature hybrid structure into parallel one-port circuits (black) with even- [a) and c)] or odd-mode excitations [b) and d)]. The illustrations located at the top labeled with **even** and **odd** resemble the initial setup before the second division as seen in Fig. 2.7 and mark the starting point for this second splitting.

Initially, the even-mode from Fig. 2.7 is analysed. The total input admittance for one parallel circuit is defined as the sum of both components with $l = \lambda/8$ and characteristic admittance $1/Z_0$ or $\sqrt{2}/Z_0$ respectively. The even-mode [Fig. 2.8 a)], where both tracks end in a magnetic wall, can now be derived by using Eq. (2.46) according to the open termination of the track as well as Eq. (2.49).

$$Y_{\text{in},e} = Y_{\text{in},e}(Z_0) + Y_{\text{in},e} \left(\frac{Z_0}{\sqrt{2}} \right) = \frac{i\sqrt{2}}{Z_0} + \frac{i}{Z_0} = \frac{i}{Z_0}(1 + \sqrt{2}). \quad (2.50)$$

Therefore, Γ_e can be calculated.

$$\Gamma_e = \frac{Z_{\text{in},e} - Z_0}{Z_{\text{in},e} + Z_0} = \frac{\frac{-iZ_0}{1 + \sqrt{2}} - Z_0}{\frac{-iZ_0}{1 + \sqrt{2}} + Z_0} = \frac{-i - 1 - \sqrt{2}}{-i + 1 + \sqrt{2}}, \quad (2.51)$$

where the correlations $Z_{\text{in},e} = 1/Y_{\text{in},e}$ and $\Gamma = (A - Z_0)/(A + Z_0)$ are applied² by substituting the input impedance of the even-mode $Z_{\text{in},e}$.

The odd-mode [Fig. 2.8 b)] is identified accordingly, employing the Eqs. (2.46), (2.47) and (2.49):

$$Y_{\text{in},e} = -i \frac{\sqrt{2}}{Z_0} + \frac{i}{Z_0} = \frac{i}{Z_0}(1 - \sqrt{2}), \quad (2.52)$$

where the path with characteristic impedance $Z_0/\sqrt{2}$ is terminated through an electric wall, resulting in the minus-sign. This is also visible in the equation for the corresponding Γ_o :

$$\Gamma_o = \frac{-i - 1 + \sqrt{2}}{-i + 1 - \sqrt{2}}. \quad (2.53)$$

Equation (2.42) and Eq. (2.43) can now be solved with substituting Eq. (2.51) and Eq. (2.53) and expanding the equation to a common denominator:

$$b_{1e} = 0 \quad (2.54)$$

and

$$b_{2e} = \frac{-1}{\sqrt{2}}(1 + i). \quad (2.55)$$

Calculating the odd-mode from Fig. 2.7 follows the same procedure, and using the appropriate signs for open and short terminations results in:

$$\Gamma'_e = \frac{i - 1 + \sqrt{2}}{i + 1 - \sqrt{2}}, \quad (2.56)$$

$$\Gamma'_o = \frac{i - 1 - \sqrt{2}}{i + 1 + \sqrt{2}}. \quad (2.57)$$

This allows the calculation of Eq. (2.44) and Eq. (2.45):

$$b_{1o} = 0 \quad (2.58)$$

and

$$b_{2o} = \frac{1}{\sqrt{2}}(1 - i). \quad (2.59)$$

Substituting Eqs. (2.54), (2.55), (2.58) and (2.59) into Eqs. (2.38), (2.39), (2.40) and (2.41) from Eq. (2.37), the S-parameters can be calculated and the resulting scattering matrix, presented in Eq. (2.60), is in accordance with Ref. [11, 12].

$$S = -\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & i & 1 & 0 \\ i & 0 & 0 & 1 \\ 1 & 0 & 0 & i \\ 0 & 1 & i & 0 \end{bmatrix} \quad (2.60)$$

²The expression for Γ resembles Eq. (3.1).

The matrix is exactly as expected and the presented derivation indicates that the performance of a quadrature hybrid is independent of absolute values, allowing for a very flexible design easily adapted to the desired working frequency by adjusting λ . A comparison of the quadrature relationship ($S_{21}^2 = -1/2$ and $S_{31}^2 = 1/2$) proves that for an excitation of port 1, power is fully divided between the ports 2 and 3 (with half-power). Furthermore, the phase shift between the ports 1 and 2 is 90° and 180° for the ports 1 to 3, confirmable by using $S_{21} = iS_{31}$ for a 90° shift from port 2 to 3 [23]. The relation between input **I** and output **O** is now well defined and the quadrature hybrid fully characterized:

$$\mathbf{O} = S \mathbf{I} = -\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & i & 1 & 0 \\ i & 0 & 0 & 1 \\ 1 & 0 & 0 & i \\ 0 & 1 & i & 0 \end{bmatrix} \begin{bmatrix} 1_{\text{in}} \\ 2_{\text{in}} \\ 3_{\text{in}} \\ 4_{\text{in}} \end{bmatrix} = \begin{bmatrix} 1_{\text{out}} \\ 2_{\text{out}} \\ 3_{\text{out}} \\ 4_{\text{out}} \end{bmatrix}. \quad (2.61)$$

Chapter 3

Experimental techniques

This chapter introduces the general measurement setup and the sample package. In Sec. 3.1, an overview of the experimental setup is given. Section 3.2 presents the sample package, including common design parameters and material properties as well as the sample (chip) fabrication. In Sec. 3.3, a measurement device, the TDR, is introduced.

3.1 Measurement setup and equipment

In this section, the measurement setup used in this thesis is presented. Figure 3.1 illustrates a typical setup for low temperature measurements which allow the analysis of Nb circuits in the superconducting state. An actual picture is shown in Fig. 3.2. The setup contains a network vector analyzer (VNA) at room temperature. The VNA is linked with a PC for data collection. Via coaxial cables, the VNA is connected to the sample package that is located inside a liquid helium bath cryostat. The VNA measures the frequency-dependent transmission between two ports of the sample package as described in Sec. 2.2. In this thesis, the network analyzer *8722D* from *Hewlett Packard* with two ports is used.

For low temperature measurements, the cryostat is a necessary device, allowing the sample chip (Sec. 3.2.1) to be examined while its niobium (Nb) layer is in the superconducting state. The cryogenic setup consists of an insert placed inside a dewar. Figure 3.3 contains a picture of the actual insert utilized during the experiments with a sample package. In order to cool the sample, liquid Helium is slowly transferred from its container into the cryostat until the sample package is fully covered in liquid ${}^4\text{He}$. The temperature of the bath is approximatley 4.2 K [24], and the sample quickly thermalizes to this temperature. Since this value is well below the critical temperature of Nb (approximately 9 K). The sample package is connected with the top of the cryostat via eight semi-rigid coaxial cables. More information in this regard is presented in Sec. 3.3. The cables can be separated into two types. The one most commonly used for our experiments is the copper-clad stainless steel cable from *Astrolab*. With regards to the hybrid ring, which requires four desirable

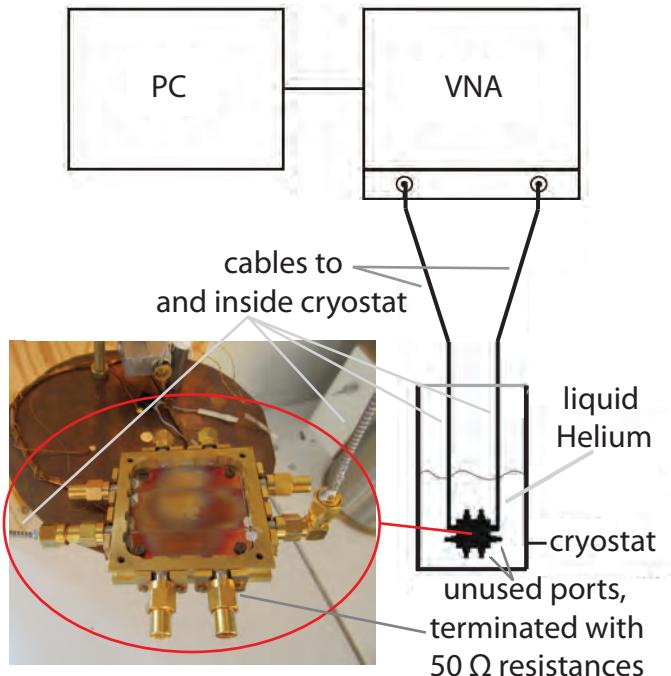


Figure 3.1: Schematic overview of a typical low temperature measurement setup with PC, VNA, cryostat and sample package. The photograph shows the sample package with the side-mount SMA connectors used in the beginning of this work.

identical connections, this type is preferred because there is a total of six of them divided into three sets that are calibrated for the *8722D*.¹ The other set, consisting of two pure stainless steel cables, has a higher loss per unit length, effectively reducing the effect of multiple reflections caused by these cables. An overview showing data for the different cable types is presented in App. C.

¹Calibration includes cables to and inside the cryostat.

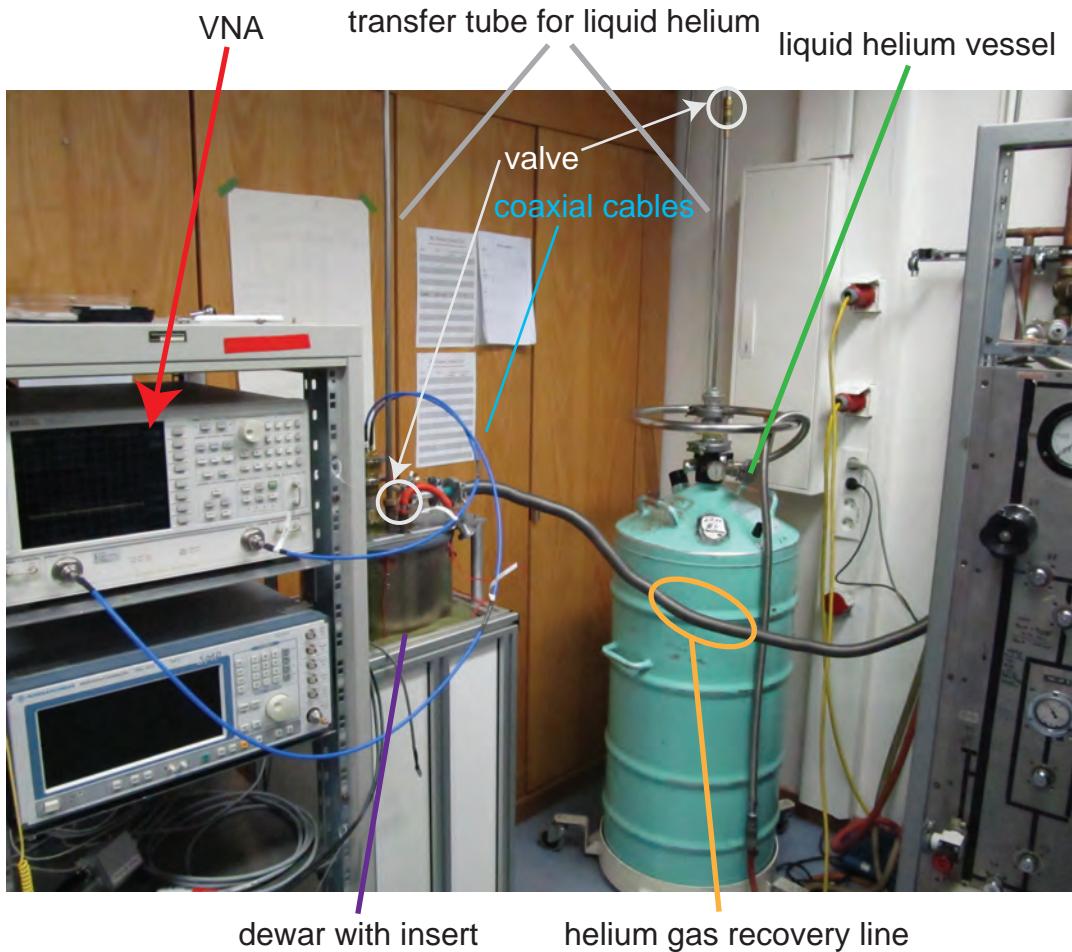


Figure 3.2: Picture of the lab containing VNA and cryostat.

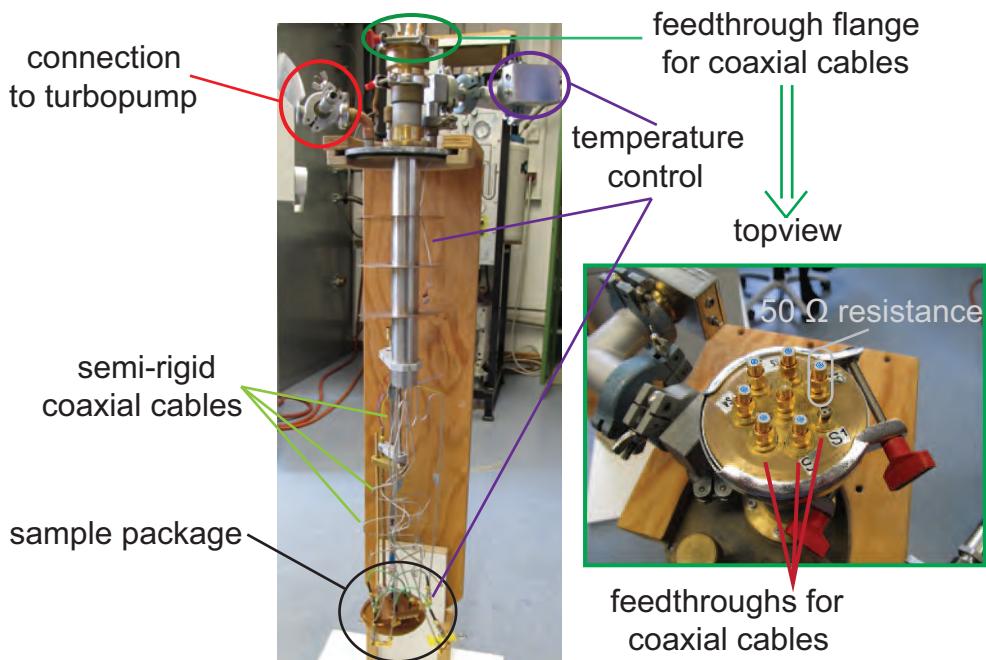


Figure 3.3: Photograph of the cryostat insert.

3.2 Sample package

This section covers the sample package: a structured chip amidst a printed circuit board (PCB) that is assembled in a gold-plated copper box. A picture of the setup can be found in Fig. 3.4. The chip in the center is connected to the PCB with aluminum bonds. We explain general design parameters and material properties as well as examine important characteristics and fabrication procedure where necessary.

3.2.1 Sample Chip and PCB

The sample is fabricated on a $12 \times 12 \text{ mm}^2$ silicon (Si) substrate, which has a thickness of $250 \mu\text{m}$ and is covered with a 150 nm thick layer of thermal oxide. It can be either a calibration chip with several waveguides on it or it can contain a quadrature hybrid structure. In both cases, the waveguides have a CPW design (see Sec 2.1) and are patterned in a sputtered 100 nm thick Nb film using optical lithography. The fabrication process takes place at the *Walther-Meissner-Institut* (WMI). An overview can be found in App. A.

The PCB is a CBCPW as introduced in Sec. 2.1. It serves as a connection between chip (through bonds) and cable connectors since it is difficult to attach the latter directly to the chip. In this section, the PCB's composition and material properties are presented. The PCBs consist of a $635 \mu\text{m}$ thick dielectric layer of *Rogers 3010* (see Ref. [25] for details on the substrate) which is covered from both sides with a $55 \pm 5 \mu\text{m}$ thick, textured copper film. An exact value for the thickness of the copper film is not available due to the uncertainty of the metallization process necessary to create vias (see Fig. 3.5). Vias are metal coated holes² that connect the conducting layer at the bottom with the ground planes at the top, thus balancing the potential. Following Ref. [11], vias are expected to improve measurement performance by suppressing parasitic parallel plate modes, a major cause of crosstalk between adjacent circuits and thus a major source of leakage. Therefore, they are employed in this thesis if/whenever possible. Typically, a PCB contains several hundreds of vias across the whole extent of the ground planes.

In general, it is desired that the characteristic impedance of the CPWs matches 50Ω which is a standard for microwave equipment and used in all our measurement setup and sample package components. With the characteristic impedance, the ratio between width and gap of the CPW is immediately defined. Due to fabrication uncertainties by the company fabricating our PCBs, we deviate from 50Ω matching. In the case of press-contact type PCBs, previous design errors further reduce matching quality especially for the unique PCB utilized during the experiments presented in Sec. 4.1.1. More details on the used connector types and their

²In this case, copper is used for coating the vias. During the metallization process, the copper thickness increases. The final thickness is not verified in this work because it is not particularly important for the microwave properties of the PCB according to Sec. 2.1, although *TXLine* shows a variation of the characteristic impedances for different thicknesses.

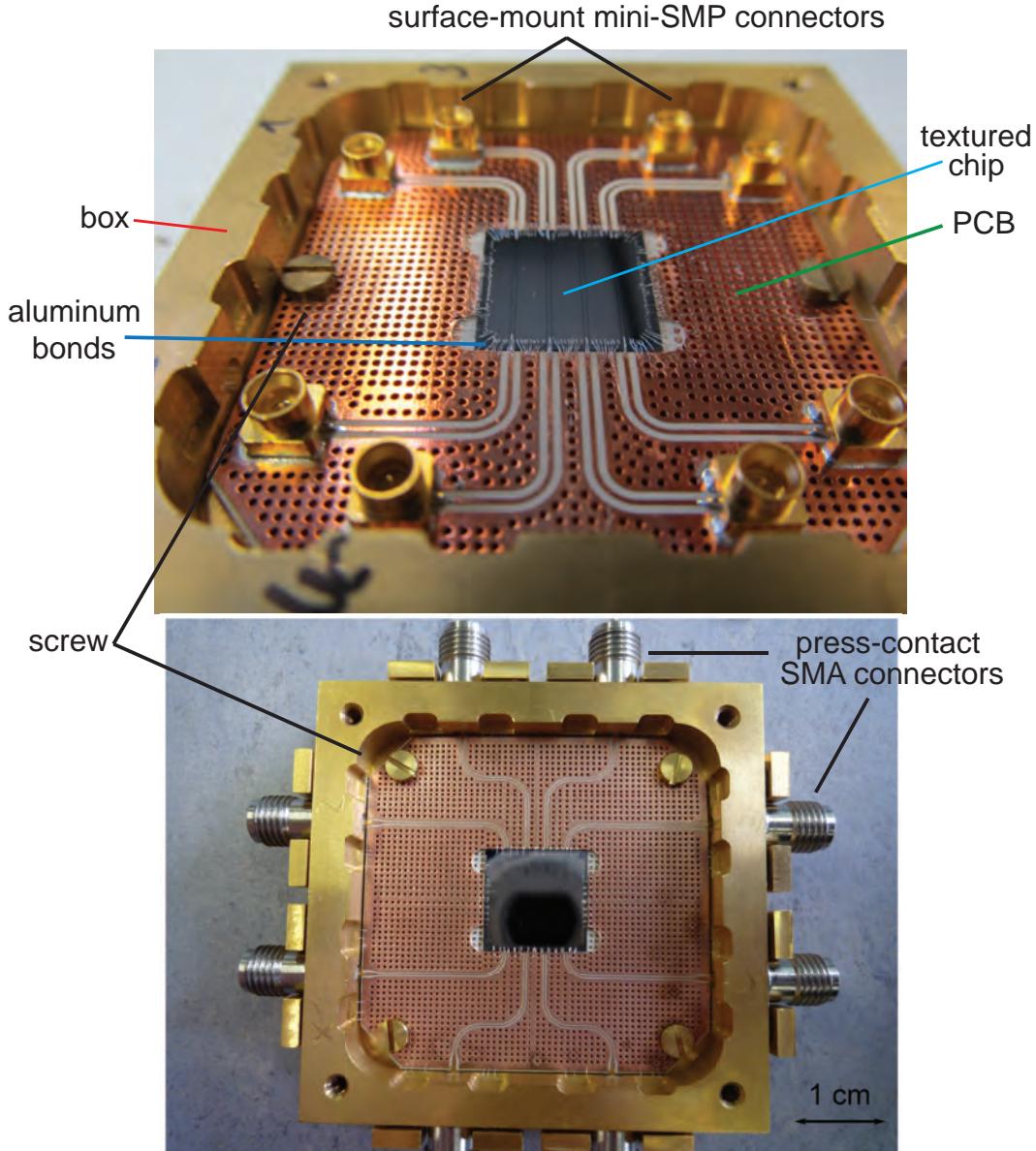


Figure 3.4: Picture of the entire sample package consisting of chip, PCB and box. While screws keep the PCB in place inside the box, connection to the chip is guaranteed through bonding. Shown are both PCB designs with the appropriate connector types (see Sec. 3.2.2 for details). The box is identical for either case and the PCBs have the same physical dimensions.

respective designs specifics can be found in Sec. 3.2.2. Our sample package features eight ports. Although only four of them are needed for the beam splitter, the other four are important for later applications.

The dielectric layer consists of *Rogers 3010*, laminated ceramic-filled polytetrafluoroethylene (PTFE) composites provided by the *Rogers Corporation* [26]. The consideration for *Rogers 3010* as the substrate is based upon its application environment at low temperatures. Under these conditions, one factor becomes more important:

thermal expansion [13]. According to Ref. [26], *Rogers 3010* has the same lateral expansion coefficient of 17 ppm $^{\circ}\text{C}^{-1}$ as copper³. Another advantage of *Rogers 3010* is that the dielectric constants of *Rogers 3010* and Si are very similar [see Ref. [27] for $\epsilon_{r,\text{Si}}(T)$]. A detailed analysis of the dielectric constant is presented in Sec. 4.1.3. As discussed in Sec. 2.1, the configuration of a chip integrated within a PCB resembles a double-layer structure and differing dielectric constants alter the performance of the device. Through matching, these effects can be compensated and the composition is effectively reduced to a regular PCB, thus allowing for separate analysis and design of the components. The metal layer consists of copper, an element with the second highest conductivity of all elements with $60 \text{ m mm}^{-2} \Omega^{-1}$ at 20°C [28], thus approaching the assumption of a lossless medium made in Sec. 2.1. The layer thickness is at least 50 μm , which translates to at least 20 times the skin depth for frequencies⁴ in the gigahertz regime (2 μm for 1 GHz according to Ref. [29]). Furthermore, copper is resilient against atmospheric corrosion by building a protective patina, has marginal low-temperature brittleness and is available for a reasonable price in high purity. The patina has to be removed at times. To this end, we dip the PCB in a mixture of 1/3 weak formic acid and 2/3 deionized H_2O for 10 s. Subsequently, it is put into a 70°C hot bath of Aceton tech., similar to the processing of a chip. It is then washed with isopropyl alcohol and blow-dried with gaseous N_2 . A clean surface is especially important when it comes to bonding.

3.2.2 Packaging

This section concentrates on the combination of the different components: packaging. Furthermore, the two main PCB designs are presented since they require different assembly techniques. In this regard, the appropriate connectors for each type are introduced as well.

Initially, the integration and connection of PCB and sample chip are described. In the center of the PCB, a square area with a side length of 12.2 mm is milled, slightly larger than the chip itself. This tolerance allows for adjustments to the chip placement. With a depth of approximately 250 μm , the surfaces of PCB and chip are on the same level. PCB and chip are then combined through conglutination, utilizing one drop of the *AZ 5214 E* resist as an adhesive. Finally, the metal surface structures are linked electrically by bonding, connecting corresponding ground planes or conductor tracks. At this point, separate steps follow for each design. They are introduced and discussed in the following. Figure 3.5 gives an overview of the different approaches.

One difference between the two PCB designs is important to note: for the PCB with the surface-mount mini-SMP connectors, all feed lines have the same length, while in the press-contact design inner and outer feedlines differ by 1.3 mm. For the

³ppm=parts per million

⁴For good conductors such as copper, the frequency dependency of the skin depth is proportional to $1/\sqrt{\omega}$. Therefore, a reduction to 10% requires a 100 times larger frequency.

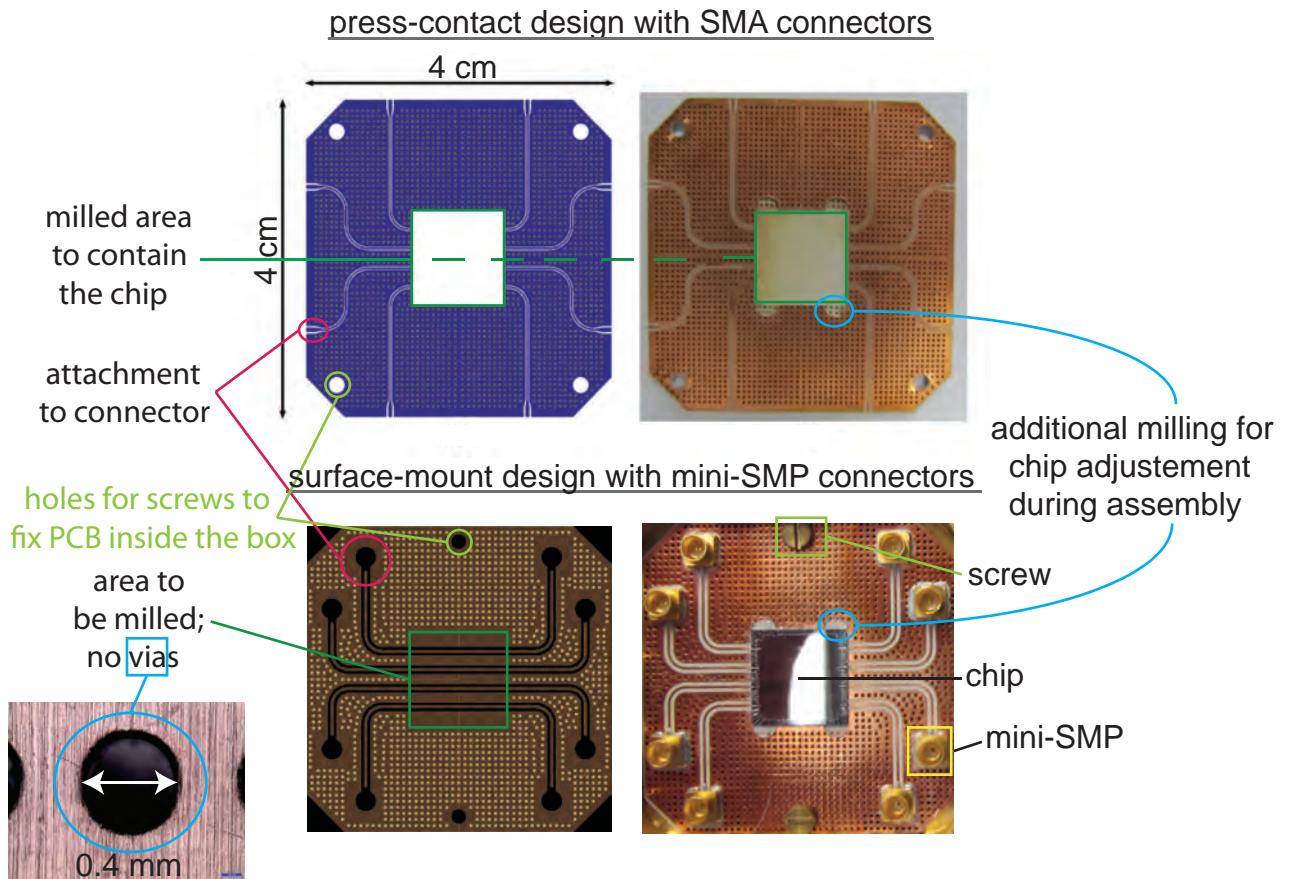


Figure 3.5: Layout (left) and photographs (right) of the press-contact and surface-mount type PCBs.

mini-SMP PCB, the line between connector and chip is now approximately 15.5 mm long. Without the $12 \times 12 \text{ mm}^2$ long chip, the total length between two connectors is 37.1 mm. The idea behind these specific lengths is to control the phase shift along the conductor.

Press-contact connectors - SMA

This initially available PCB design [Fig. 3.5 a)] relies on press-contact SMA connectors of the type 32K724-600S5 from *Rosenberger* (see Fig. 3.6 and data sheet Ref. [30] or homepage Ref. [31] for more details) to link the PCB with the measurement equipment or other hardware such as the cryostat. The PCB with chip is placed inside the box and fixed in place with four screws located at the edges. The box has two holes on each side to mount the connectors. Their center pins fit through the holes and end directly above the PCB. A connection is then establishing by elevating the PCB. Therefore, screws at the bottom of the box directly underneath the pins are tightened, thus pushing up the PCB and pressing it to the connectors. Care has to be taken to avoid bending or breaking of the connector pin in this process.

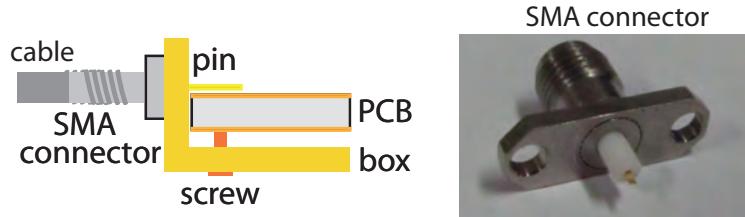


Figure 3.6: Left: schematic illustrating the functionality of a SMA press-contact connector. Right: photograph of the connector. The pin of the SMA fits through a hole in the side of the box. Connection to the PCB is accomplished by pressure through an elevating screw.

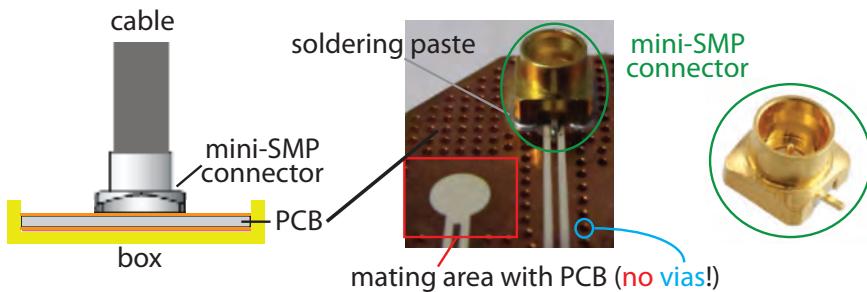


Figure 3.7: Illustration and photograph of the surface-mount mini SMP connector used in the new PCB design. It is soldered directly onto the PCB, connecting both conductor and groundplanes this way. Also indicated in the left figure is the adaptor, labeled as 'cable'.

Surface-mount connectors - mini-SMP

The second design utilizes the 18S101–40ML5 mini-SMP connectors from *Rosenberger* [32], compact surface-mounts that are $4 \times 4 \text{ mm}^2$ wide. The full detent version is chosen for a further increase in connection stability with a disengagement force of approximately 29 N. Surface-mount connectors are soldered directly onto the PCB as illustrated in Fig. 3.7. Therefore, a small amount of soldering paste⁵ is applied to the PCB at the attachment areas and the connectors are positioned ontop. The PCB is then placed on a hotplate for 10 to 12 seconds at 230 °C. A positive side effect is the self-adjustment of the connectors due to capillary forces. The soldering process turns out to be reversible, i.e. it is possible to recover the connectors for a potential later reuse. Careful handling is required when taking the PCB off the hot plate as long as the soldering paste is still liquid to avoid unwanted displacement. After the connectors are soldered to the PCB, the sample chip can be mounted and the PCB is then placed inside the sample box. For linking the PCB with the remaining setup that uses SMA connections entirely, a SMA/mini-SMP adaptor cable is necessary (see Sec. 3.3). The PCB is fixed in the box with two screws. Furthermore, a lid for the box suppresses air modes.

⁵No-Clean SMD-Lotpaste CR44 Sn62Pb36Ag (alloy) with flux FSW-32

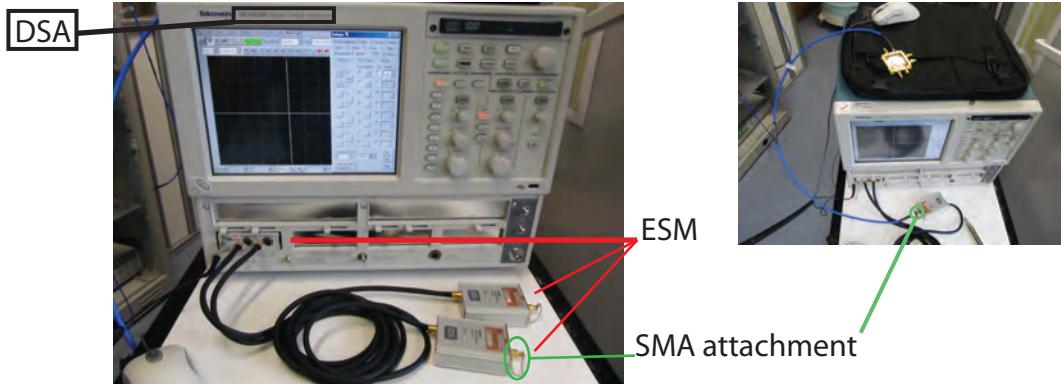


Figure 3.8: Photograph of TDR setup with DSA and ESM. The small picture also shows the measured device connected to the TDR sampling module.

3.3 Time Domain Reflectometry

TDR is used to measure impedances and impedance mismatches inside a device. Impedance has already been recognized as an important indicator when it comes to the properties of CPWs. But alternating impedances, for example at the connection between two components, cause reflections. The associated reflection coefficient r is:

$$r = \frac{Z_1 - Z_2}{Z_1 + Z_2}. \quad (3.1)$$

Here, Z_1 and Z_2 are the impedances on either side of the connection. The TDR makes use of this characteristic and detects reflection of a probe pulse as a function of time. Figure 3.8 shows a picture of the device used in a typical setup. It consists of a Digital Serial Analyzer (DSA) from Tektronix, the *DSA8200* [33], and an Electrical Sampling Module (ESM), the *80E08* [34]. For low-temperature measurements, the ESM can be connected to the feedthroughs of the coaxial cables of our cryostat containing the device under test.

In the following, we discuss a few fundamental TDR measurements on our devices. In particular, we identify the position of physical objects such as the measurement box or the PCB. First, it is important to recognize PCB and sample holder as isolated devices as well as in a typical setup environment. Therefore, experiments are done with and without a cryostat. The utilized PCB with press-contact SMA connectors has no vias and only two straight CPW lines running across. More details on the PCB can be found in Sec. 4.1.2. Figure 3.9 a) focuses on the actual PCB which is connected with the TDR through a 16" *minibend* coaxial cable. For a full analysis, the data for the cable with and without the box is shown to confirm the exact position of the box. Thereby, the following relation can be utilized to correlate a time span Δt with a length in position space using Eq. (2.19) or a comparative calibration:

$$v_{\text{ph}} = \lambda f \quad (3.2)$$

In other words, the phase velocity v_{ph} is the product of the wavelength λ and the frequency f . Note that the TDR has an internal delay of 42.5 ns. The PCB can be clearly identified as a short flat section of the curve between two peaks indicating the mismatch of the connectors. For the second setup, the box is placed inside the cryostat to identify its position for later experiments when the PCB is intended to match 50Ω with low peaks from the connectors. Its characteristic impedance of less than 43Ω proves useful at this point, making the PCB very distinguishable from the 50Ω -matched cables of the cryostat. Figure 3.9 b) shows the TDR results for a cryogenic situation, where the one waveguide inside the sample package is connected to the ports 5 and 6 of the cryostat. In all these measurements, the external cable length is determined through a calibration, using a 16" *minibend* ($\Rightarrow x$) for a TDR analysis (Δt). The resulting velocity is confirmed for several cables of the same type. For the internal cryostat cables, we determine the phase velocity according to the data sheet [35] and the measured Δt . In Fig. 3.9 c), the effect one can see is that the cables in the cryostat exhibit significant length differences. Hence most TDR measurements presented in this thesis are modified by a suitable time offset to allow for a better comparison of the results.

In the next experiment, we examine more closely the impedance inside the sample package at low temperatures. The same PCB with press-contacts as in the previous measurements is utilized, although this time a different waveguide inside the sample package is investigated. In Fig. 3.10, the TDR probing pulse is applied to the waveguide in the sample package from opposite directions. For ideal connections to the PCB, the curves are expected to be symmetric with respect to a vertical axis through the midpoint of the waveguide on the PCB. While the PCB is indeed symmetric, the mismatch of the connectors clearly differ from each other. Since the signatures of the input connector are very similar, we identify most of this effect as an artifact due to the strongly reduced probe signal reaching the second connector. We next turn to a PCB with mini-SMP surface mount connectors. With the mini-SMP connector type (Fig. 3.7), we use short SMP-SMA adaptor cables for the connection to the SMA cables in the cryostat. Figure 3.11 shows TDR measurements of the PCB for all adaptor cables available at that time. These belong to one of the two types *SCA97047-10* and *GPPO* [36]. The setup for these and the following measurements contains a PCB with surface-mount connectors, connected with the TDR via a 1 m long cable. The PCB does not contain a milled pocket for the chip. The four adapter cables are each connected to a different waveguide on the PCB. While different cables of the same model do perform similarly, there is a significant discrepancy between the two adaptor cable types. The initial dip is more than 5Ω deeper for SCA97047 and the peak afterwards is almost 5Ω higher. According to Eq. (3.1), this results in a difference of reflection losses by more than 100% between the adaptor cable types, assuming both features count as separate reflection points. In agreement with the different connector reflection properties, also the characteristic ripples along the waveguide on the PCB are higher when the SCA97047 adaptor cables.

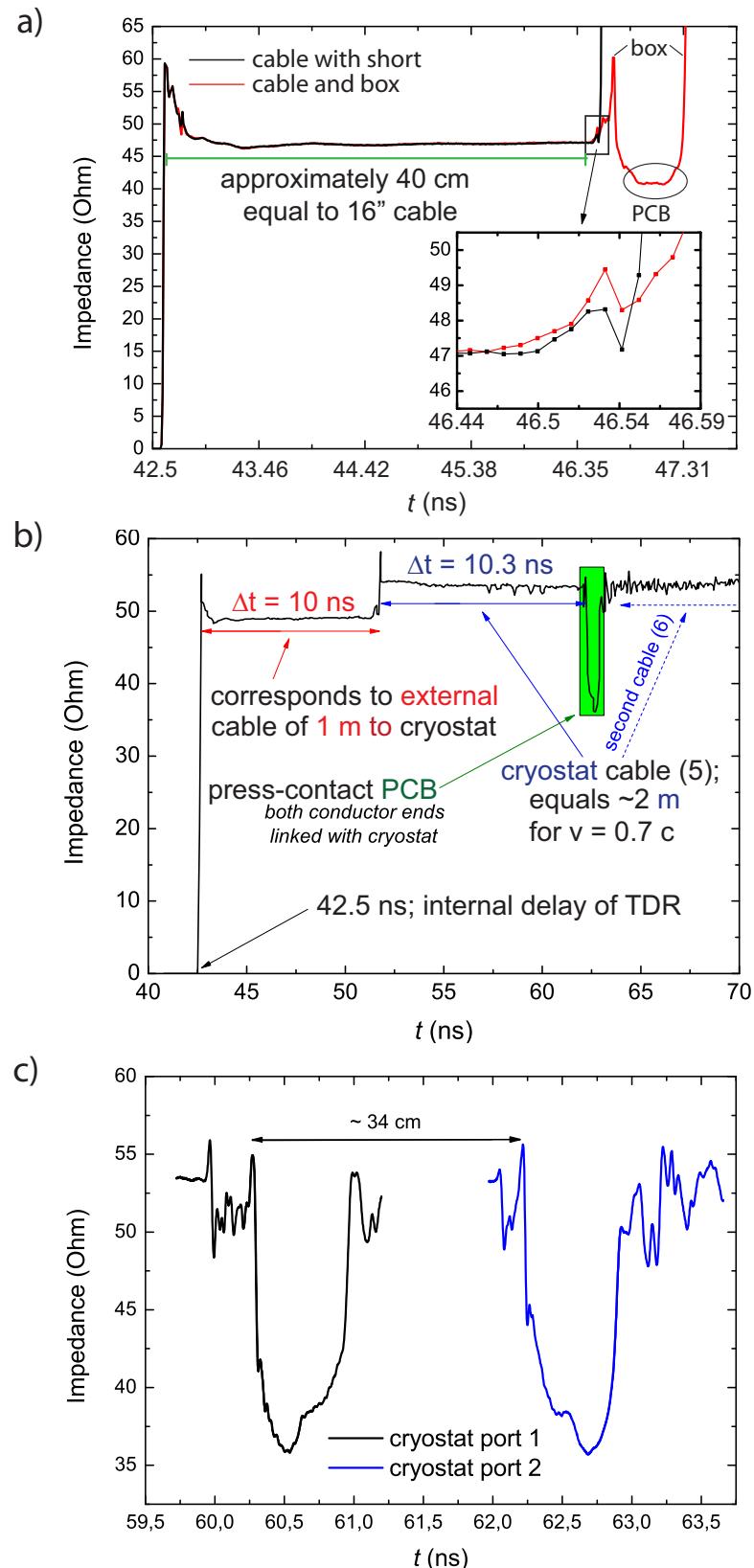


Figure 3.9: TDR experiments with the press-contact PCB from Sec. 4.1.2 out- and inside the cryostat. **a)** Sample package at room temperature outside the cryostat. **b)** Low temperature analysis inside the cryostat. The numbers in parentheses indicate the corresponding ports. **c)** The length of the cryostat cabling can be deduced from the occurrence of the characteristic PCB feature.

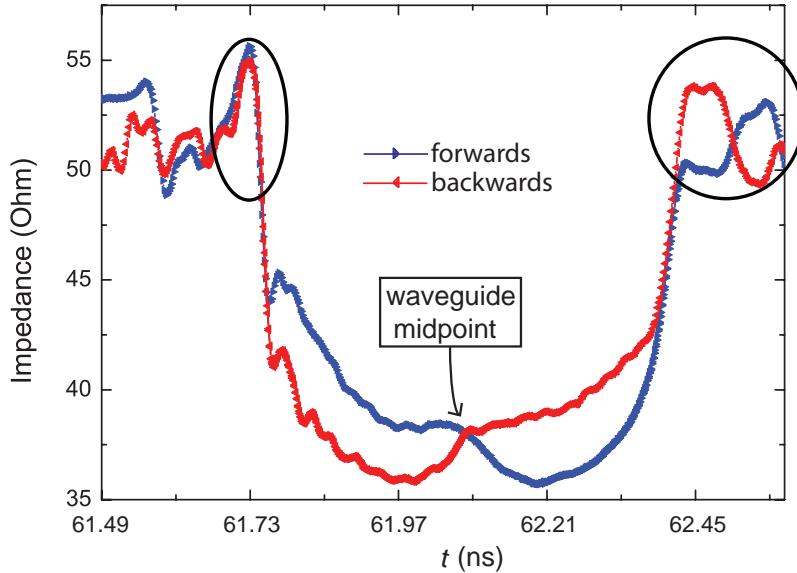


Figure 3.10: Impedance of the sample package measured from opposite directions. Strongly asymmetric features (connectors) are encircled.

Because these ripples are artifacts due to multiple reflections, their magnitude is expected to roughly scale with the magnitude of the impedance mismatch at the connectors acting as reflection points. In Fig. 3.12 a), connector, adaptors and the PCB are marked. In accordance with the previous results, GPPO adapter cables are utilized. In one measurement, the unused connectors at the opposing end of the waveguide on the PCB is unattached and thus equal an open termination. For the other, a second adaptor is connected instead. This data leads to the conclusion, that the initial dip can be associated with the transition at the connector. Therefore, the PCB is assumed to be located in between those features. The second experiment, shown in Fig. 3.12 b), concentrates on the chip and is therefore conducted at low temperatures. An area of the PCB is milled to include a calibration chip with four parallel waveguides and both ends of the sample package are connected to the cryostat with adaptor cables. The first measurement reveals the chip position. It is distinctly and visibly positioned in the center of the PCB, bounded by two peaks that mark the transition to and from it. The connection at the end of the PCB cannot be seen because it is covered by the ripples already seen in Fig. 3.11. The first connector signature designates the beginning of the PCB. In the second measurement though, the PCB location, and thus the (relative) position of the chip, is verified by showing both intersections with the connectors. Here, the connection to the chip has improved so much compared to the other measurement, that the transition to and from it can barely be seen at all. The data is presented in the time domain because, depending on the position, there are different phase velocities involved for the different media. For the external cabling, 62 ps roughly correspond to 2 m, one each from cables to and inside the cryostat.

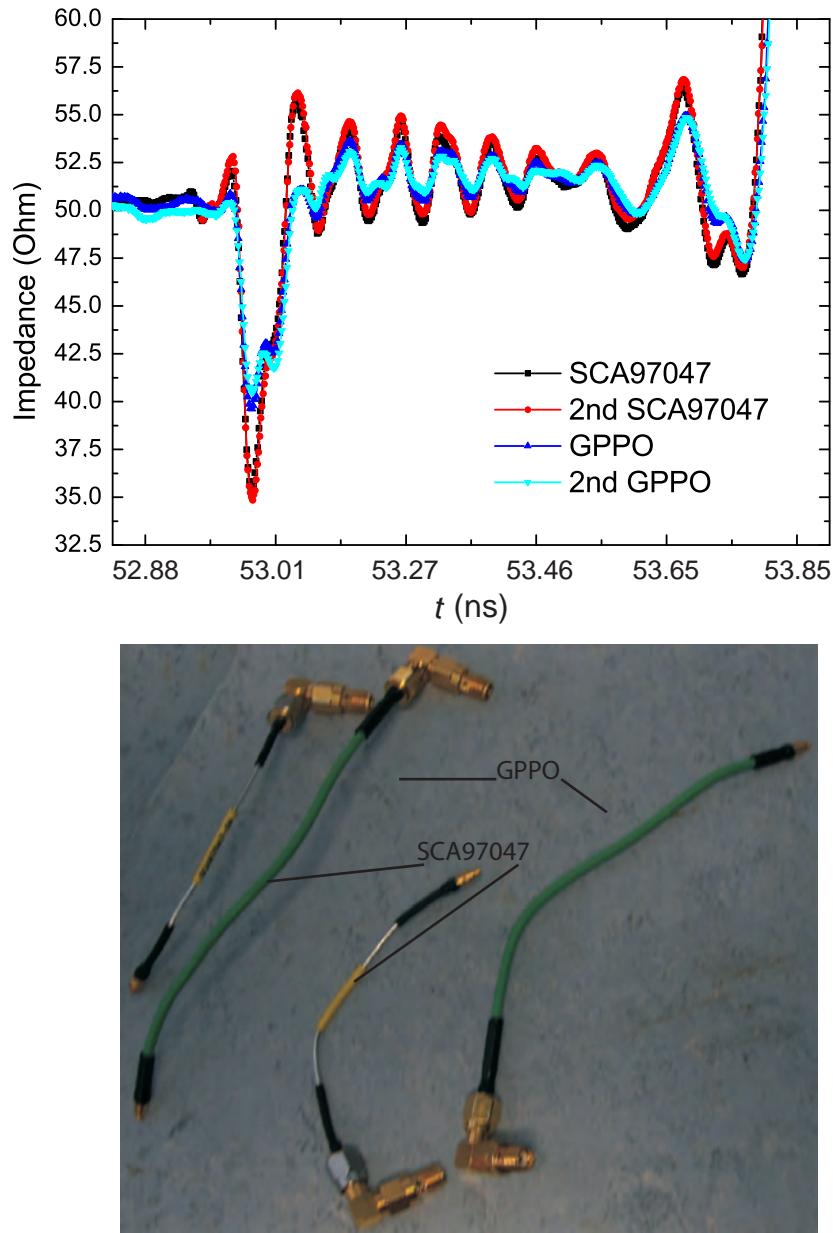


Figure 3.11: Contrasting both available adaptors, *SCA97047* and *GPPO*, regarding performance quality in exemplary measurement and physically via photograph.

After this general TDR analysis of our setup, we turn to a more detailed analysis with optimized parameters and a discussion on the details of the sample package in the next section.

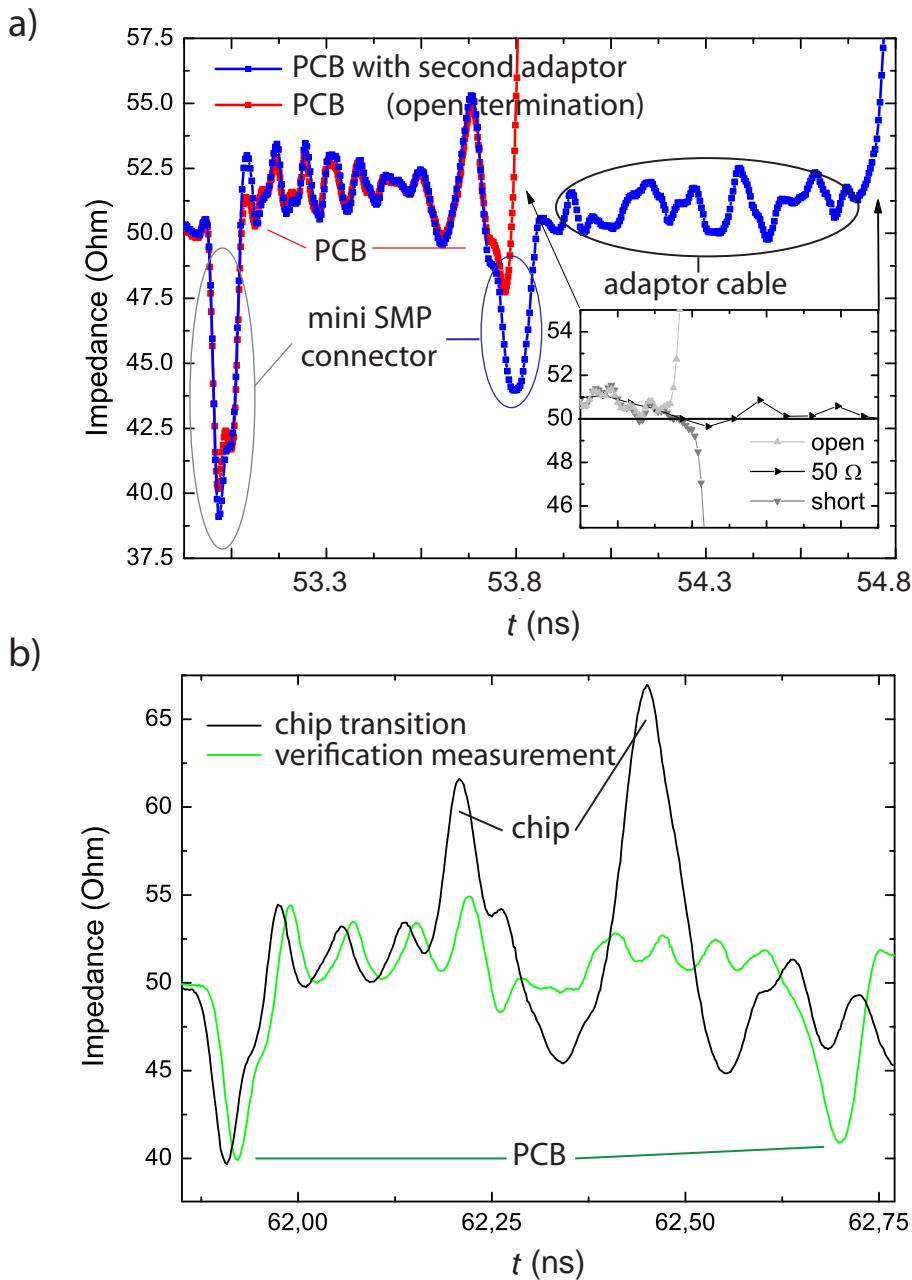


Figure 3.12: TDR measurements using a PCB with mini-SMP surface-mount connectors. **a)** Typical traces. Inset: typical signatures for the three fundamental termination types. **b)** PCB with chip. In the verification measurement, the PCB-chip matching has improved significantly, making the output connector at the PCB visible.

Chapter 4

Experimental results

In this chapter, the main results are presented and discussed. In Sec. 4.1, improvement possibilities regarding the connections between the various components of the sample package are examined and the different PCB designs from Fig. 3.5 are compared. The 90° hybrid ring, as described in Sec. 2.3, is discussed in Sec. 4.2.

4.1 Characterization and optimization of the sample package

This section primarily addresses the PCB since it functions as the connection between actual sample, the chip, and the measurement equipment. First, a PCB with press-contact connectors (see Fig. 3.5) is examined in Sec. 4.1.1. As a result, alternative approaches for improving the connection between setup and PCB are presented and analyzed in Sec. 4.1.2. Section 4.1.3 employs the previous findings and combines them with preliminary considerations in an alternative approach with the PCB. A comparison of old and new design for the PCB is conducted in Sec. 4.1.4, comparing the performance and other crucial properties. Section 4.1.5 concentrates on the remaining critical connection onto the chip, utilizing the new PCB design with surface-mount mini-SMP connectors.

4.1.1 Analysis of press-connector sample holder

The starting point of this work is the quadrature hybrid measured during Michael Fischer's bachelor thesis [37]. The S-parameters of this device were measured using the press-contact sample package shown in Fig. 3.4. However, the results were not at all satisfactory as seen in Fig. 4.1. In particular, there is no frequency where the S-parameters of the “direct” and the “coupled” port are close to 3 dB simultaneously. Therefore, we perform additional calibration measurements on this sample package at low temperatures to get an overall impression of the performance or uncover potential design flaws.

The designs of the two used calibration chips are presented in Fig. 4.2. Figure 4.3 shows the corresponding data where several unexpected features confirm the presence of design problems. The setup for these experiments is the one presented in Ch. 3.1: a transmission measurement through a PCB with chip, conducted in the frequency domain and at low temperatures using the two lossy steel cables of the cryostat. The utilized press-contact PCB can be found in Fig. 3.5 **a)**. The design parameters for the CPWs are $w = 200 \mu\text{m}$ and $g = 130 \mu\text{m}$. The two ports of the sample package required for the transmission measurement are connected to the cryostat cables 1 and 2. The other six unused ports are terminated with 50Ω loads. The performance observed is not satisfactory. Especially the large dip of -2.5 dB seen at 6 GHz is close to the desired working frequency of the beam splitter of 5.77 GHz (defined through geometry, see Sec. 4.2). The utilized VNA calibration, which includes cables to and inside the cryostat, does not appear to be responsible for the features, since the transmission is otherwise near 0 dB . One possible explanation for this behaviour might be spurious resonances caused by multiple reflection points inside the sample package. The most prominent candidates for such reflection points are the connector-PCB transitions and the PCB-chip transitions. When checking the resonant frequencies of various hypothetical half-wavelength resonators in our sample package (see Fig. 4.4), we indeed find that they are close to the center frequencies of the dips in Fig. 4.3.

For further clarification, the calibration chip is exchanged in favor of another design [Fig. 4.2 **b)**]. As a result, we can see in Fig. 4.5 that the 6 GHz -dip, which we identified as most likely chip-resonance (see Fig. 4.3 and Fig. 4.4) changes significantly while most other features don't. We hence conclude that it is of utmost importance to optimize the impedance matching between all components of the sample package when working with open waveguide structures such as transmission lines or quadrature hybrids.

Furthermore, the 0.5 dB offset between both measurements shown in Fig. 4.3 illustrates a general problem with our setup. Reproducibility is not guaranteed and cooldown-to-cooldown deviations are regularly encountered. A detailed examination in this direction is conducted in Sec. 4.1.4.

The instructive analysis of calibration chips presented in this section enabled the identification of weak points in the design of the sample package.

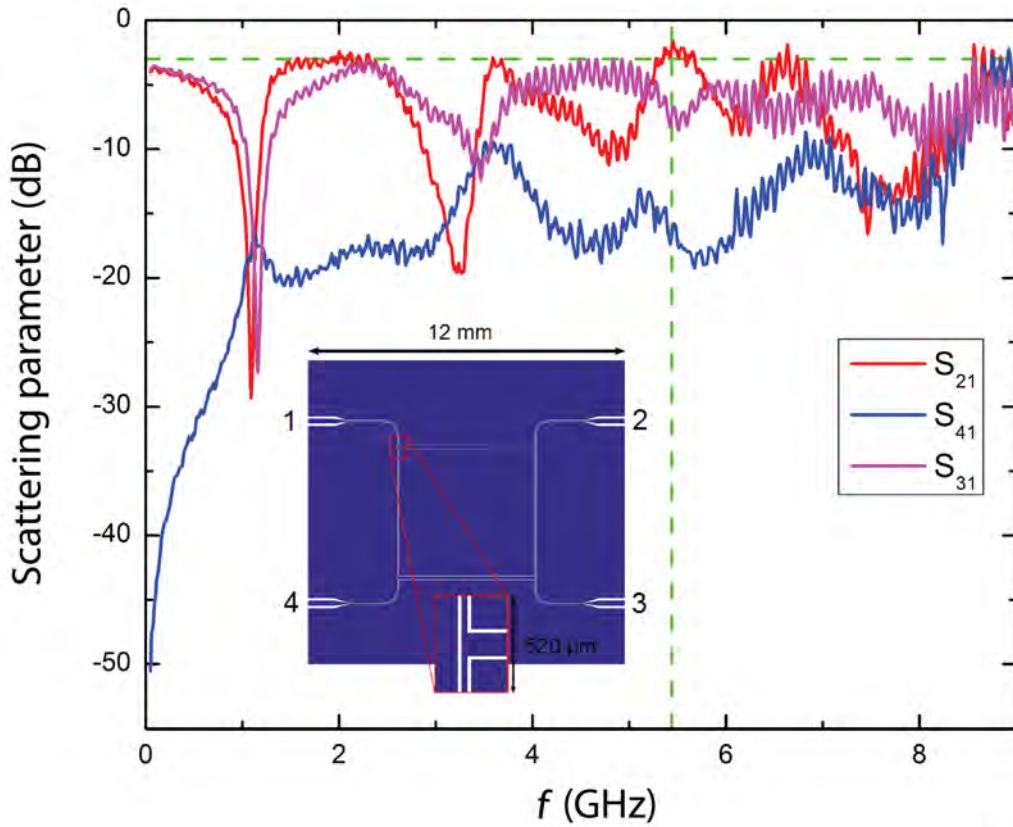


Figure 4.1: Data of hybrid ring measurement with kind permission from Michael Fischer, conducted during his bachelor thesis [37].

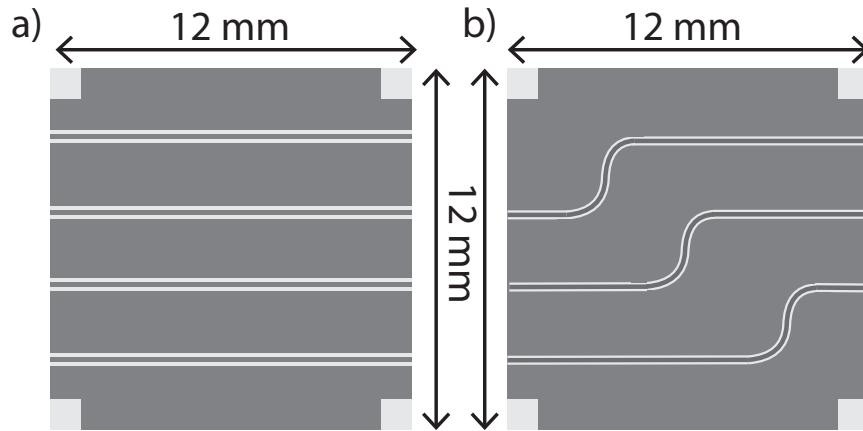


Figure 4.2: Two calibration chip designs with different waveguide lengths and characteristic impedance $Z_0 = 50 \Omega$. The corresponding parameters are: width $w = 200 \mu\text{m}$ and gap $g = 100 \mu\text{m}$.

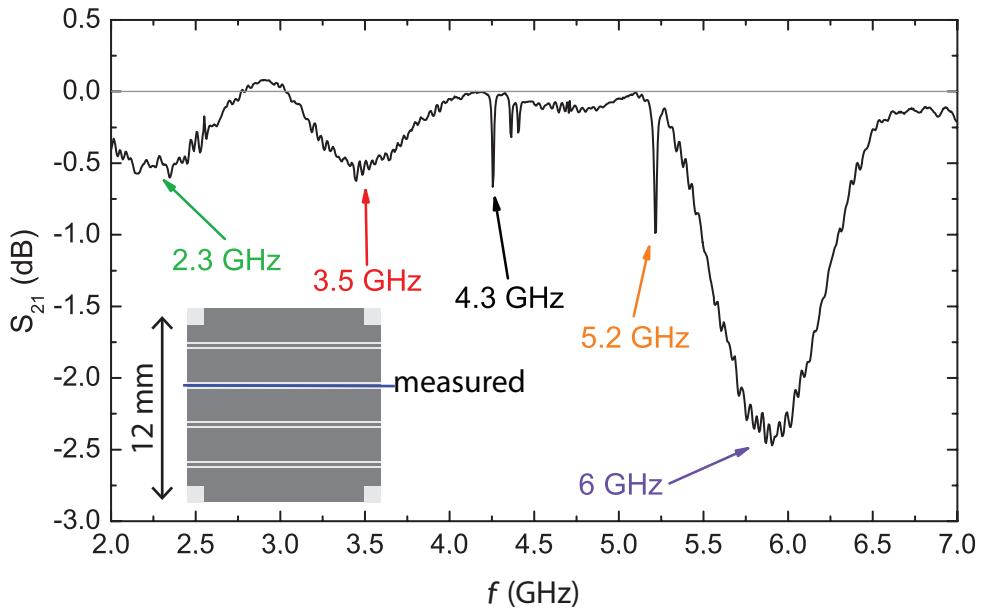


Figure 4.3: First frequency domain measurement using the calibration chip design shown in inset from Fig. 4.2 a). The measurement path is denoted in blue.

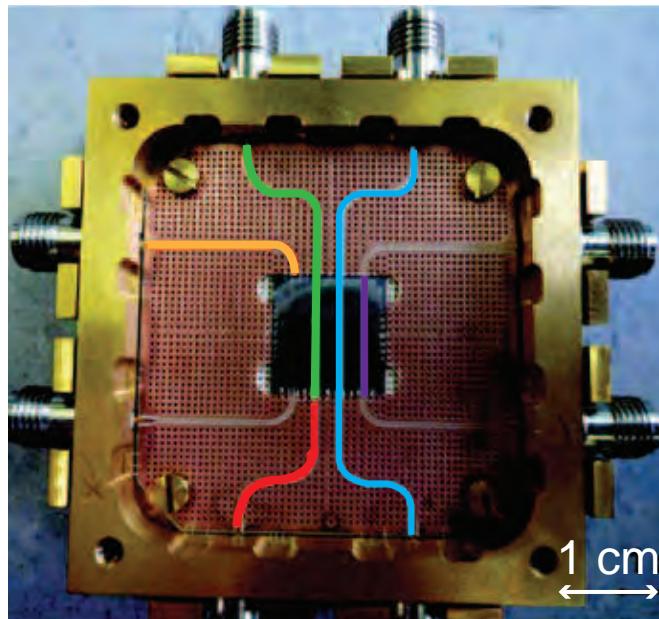


Figure 4.4: Different paths to possible reflection points at intersections using PCB with SMA connectors.

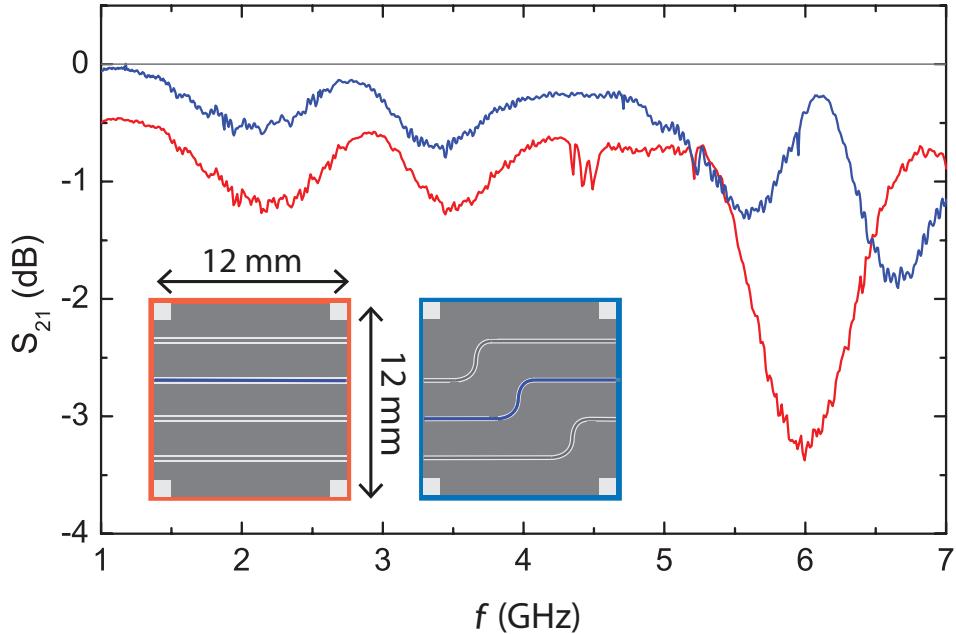


Figure 4.5: Measurements with different calibration chip designs shown in inset where measured transmission path is marked in blue.

4.1.2 Matching between PCB and SMA press-contact connector

The first critical connection to be examined comprises the transition regions of a box with SMA connectors and the PCB. In this section, several techniques to improve the matching are discussed. The measurement series is divided into two parts. Initially, the transition from connector pin to PCB waveguide is analyzed. Then, we examine how to best connect the corresponding ground planes, using the best result from before. The performance is examined via time domain reflectometry measurements, allowing for a direct analysis of the characteristic impedance. Finally, the best result of the second series are compared with the initial setup from Sec. 4.1.1 to visualize the progress achieved.

For these experiments, a PCB with press-contact SMA connectors that is designed especially for this particular task is utilized. To concentrate on the region in question, no chip is incorporated since it would only complicate the analysis at this point by introducing more reflection points. In addition, the PCB only contains two waveguides with a width of 490 μm and gap 230 μm that are completely straight to reduce the possibility of unwanted reflections at waveguide bends. A picture is included in Fig. 3.1. With this critical component (chip) of a regular setup missing, measurements with a vector network analyzer are not included at this point. Without a chip and therefore no superconducting component, this measurement series can also be conducted at room temperature, approximately 293 K. Nevertheless, a prototypical analysis at 4 K is done for one of the ports but not the whole series¹.

¹Low temperature measurements require a cryostat as described in Sec. 3.1.

Unused connectors are terminated with 50Ω loads. There are no vias in this PCB. A schematic of the PCB is shown in Fig. 4.6 and a picture of the general setup can be seen in Fig. 3.8.² The examined port is connected to a TDR sampling module with a 16" *minibend* cable.

Connection between connector pin and PCB conductor

The first experiments concentrate on the center conductor of the CPW, and several techniques are applied to improve the connectivity between the PCB and the connector pin. Figure 4.6 shows a schematic of the setup for these measurements. One port is the classical press-contact as described in Sec. 3.2.2 and no further improvements are utilized. The opposite connector across the conductor track is additionally bonded to the CPW center conductor. For the second conducting lane, silver glue is carefully applied with a toothpick to one connector, avoiding a connection between center conductor and groundplane. At the second port, a small amount of soldering paste is deposited on the connector pin and then heated with a hot air gun. This technique proved to be disadvantageous as described at the end of this section. Box and groundplane are ignored and not connected. The measurement data can be found in Fig. 4.7.

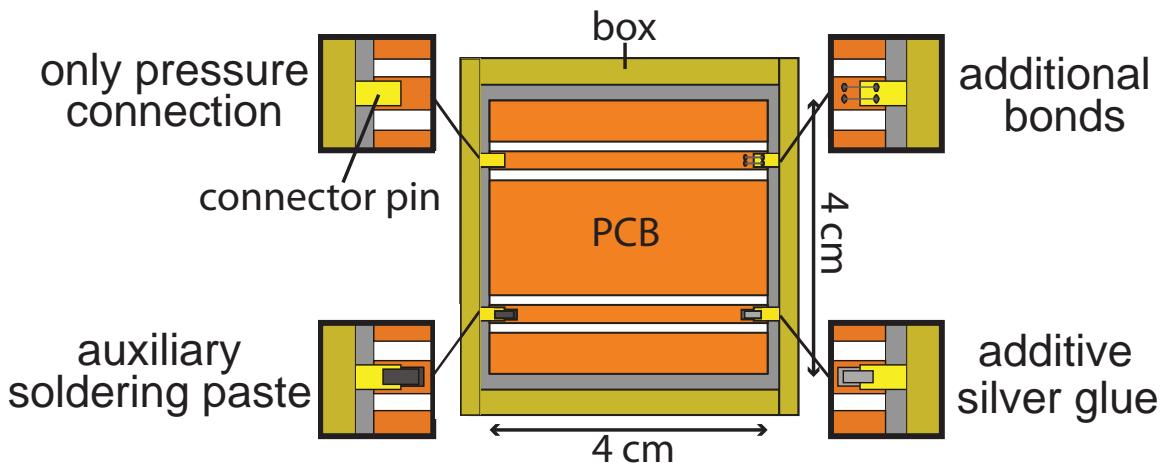


Figure 4.6: Measurement setup for comparing different techniques of connecting the connector pin to the PCB waveguide center conductor with each pin pressed to the board as shown in Fig. 3.6. While the first method only relies on this type of connection, two bonds are further linking pin and center conductor for the second. For the third, soldering paste is utilized and silver glue is applied to the final one. The materials of the last two techniques are applied above and under the pin, after assembly as described in Sec. 3.2.2.

²The PCB is concealed in a covered box for these experiments

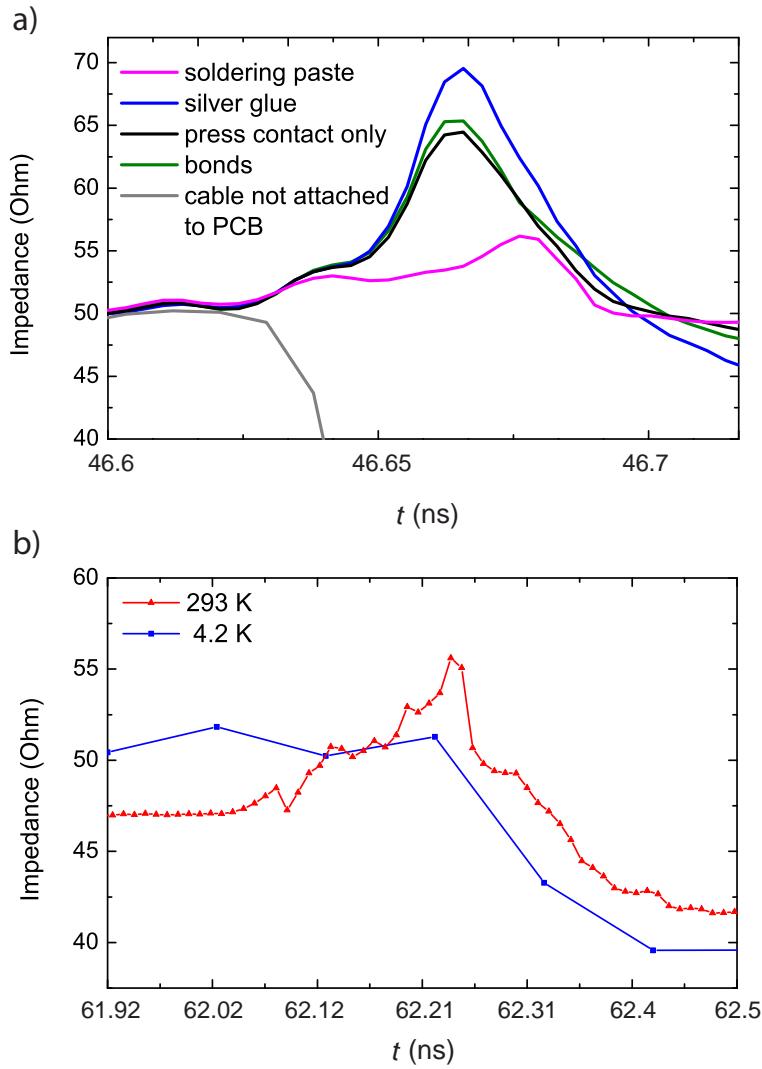


Figure 4.7: Results of time domain reflectometry measurement for various connection methods of the center pin. **a)** Measurement series at room temperature and **b)** one selected port (soldered connector) compared to its results at 4.2 K.

According to the data presented in Fig. 4.7, soldering clearly depicts a preferable connection possibility. Compared to the pure press-contact, the characteristic impedance peak has decreased by approximately 10Ω . The other techniques are clearly inferior. Since they are also not very reproducible and, except for the bonding, not stable during thermal cycling, we do not investigate them further. In contrast, the thermal stability of the soldered connector is very good as we can see from Fig. 4.7 b). A particular problem of the non-soldered connections resides in the contact area between connector pin and PCB. The delicate pins do bend easily (Fig. 4.8), especially when under constant pressure of the PCB. This in turn results in a variation of the total mating surface, accordingly decreasing the connection



Figure 4.8: Picture of connector, showing a minor bending of the pin.

quality significantly. In some cases, the connection between press-contact connector and PCB is even lost during cool down because of differing thermal expansion coefficients. This effect is visible in VNA measurements where the transmission at low frequencies is drastically suppressed, resulting in a capacitive transission characteristics as shown in Fig. 4.9. Additionally, open contacts can be confirmed with a dc resistance measurement. The measured resistance accross the sample package is then above a megaohm while a usual value would be approximately 67Ω . In conclusion, it is assumed that most differences observed in Fig. 4.7 can be explained with the unreliability of press-contact connectors. This is an issue that immediately prevents reproducibility of measurement results and represents a main motivation for switching to mini-SMP connectors.

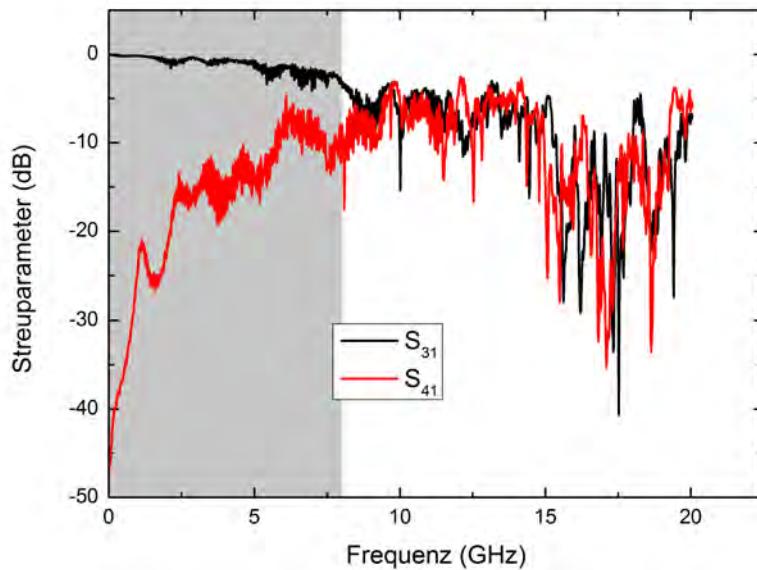


Figure 4.9: Transmission measurement with the VNA. Graph is showing the scattering parameter as a function of the frequency. In contrast to the black curve, the red curve corresponds to an open connection. The capacitive characteristic is most prominent in the shaded area. Taken from his bachelor thesis with kind permission from Michael Fischer [37].

Contacting box and PCB ground planes

In the next measurement series, the effects of joining the ground planes of PCB and connector, and therefore the box, are examined and the various techniques from the previous series are applied again and an identical setup is utilized. Here, all center pins are soldered. A setup schematic is presented in Fig. 4.10. The ground planes act as resonators as well and their huge width softens the boundary condition for excitations. We compare the cases of no ground plane connection, bonded, silver-glued, and soldered ground plane connection. However, the relatively large distance of at least 1 mm between PCB and box complicates some of these approaches. For the first scenario of a missing connection, there are no disruptions and the same is the case for bonding. Silver glue, on the other hand, is problematic and has to be applied in large amounts to actually bridge the gap. Soldering paste is also utilized in larger quantities to cover a sufficient area, requiring more power for the necessary heating process. The corresponding data is presented in Fig. 4.11. It can be seen that a solid connection between ground plane and box does have a positive effect on the impedance peak. For the initial peak, a decrease of more than 5Ω can be observed with increasing connection quality. Soldering proves to be the preferable technique again, since the thermal stability of silver glue is questionable. The addition of bonds on the other hand seems to have no beneficial effect at all. It should be noted that due to the box design, the bonds can only be applied further off the conductors, a circumstance that is eventually deteriorating the comparison.

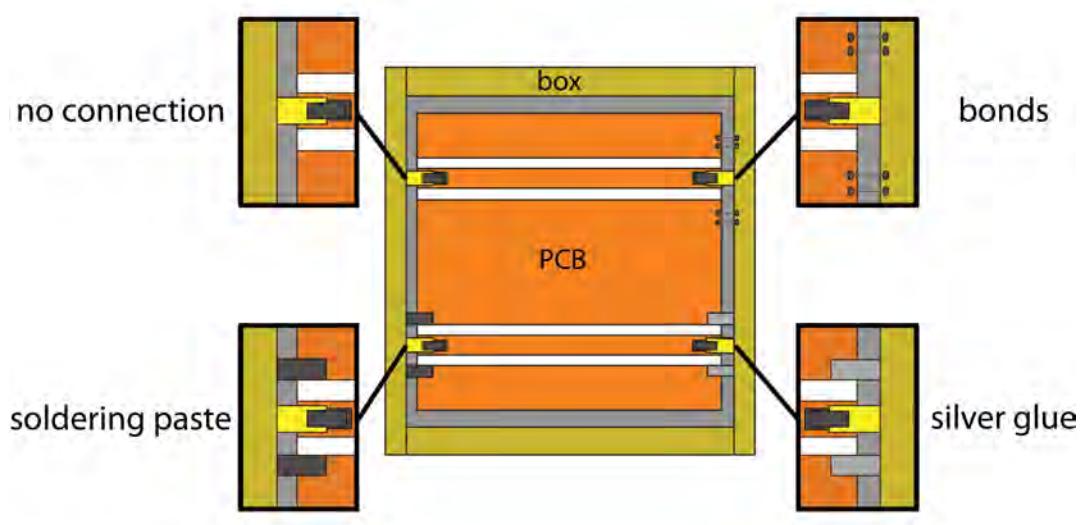


Figure 4.10: Schematic overview of "ground plane connection" measurement series experimental setup. The different techniques, applied in the immediate neighbouring space of the conductor, are: no connection, bonds, silver glue and soldering. All connector pins are soldered to the center conductors.

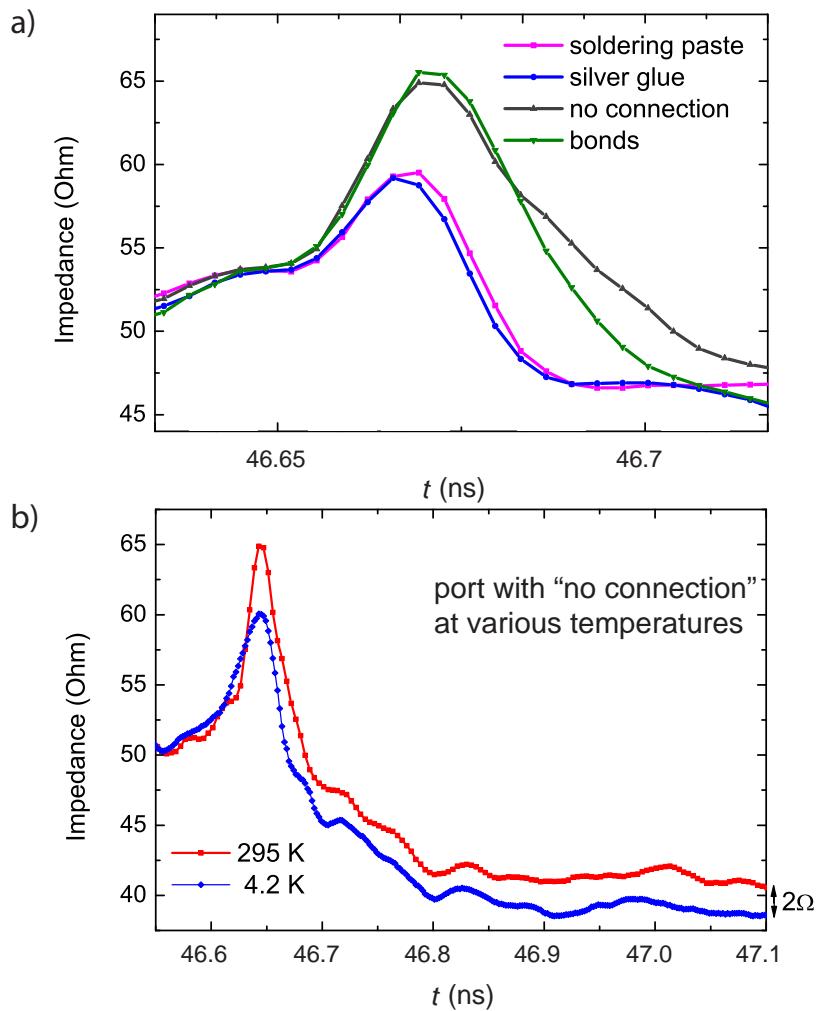


Figure 4.11: Time domain reflectometry measurements for soldered center pins and various connection methods between ground plane and box. **a)** At room temperature. **b)** Temperature dependence of the “no connection” port.

Conclusion

We now compare the results from the Fig. 4.7 and Fig. 4.11 in detail. We find that soldering is the preferred connection method for both center conductor and ground planes. In addition, the quality of the soldered contact can vary when applying excessive heat (air gun, see also Fig. 4.12) to the PCB. This is the reason why the characteristic of “no ground plane” (Fig. 4.7) is a few ohm better than the “soldered ground plane” characteristic in Fig. 4.11. However, the latter figure clearly demonstrates that for a given situation, a solid connection between ground plane and box is important.

A concluding summary is presented in Fig. 4.13, illustrating the progress during the measurements above. The transition onto the PCB of the initial setup with pure press-connection is compared to the best performing composition of this series: soldered conductor and ground planes. Already in Fig. 4.13, the impedance mismatch is reduced by 5Ω despite an accidental mistreatment of the PCB. In the more optimistic approach of independently considering the effects of the two measurement series of this section, the impedance mismatch could be reduced by 15Ω . This corresponds to a reduction of reflection losses by at least 10 % according to Eq. (3.1). Nevertheless, the box-mount SMA connectors require to make the connections with the PCB inside the box. This situation promotes problems such as excessive heating of the PCB. Hence, we explore solder-on surface-mount connectors, which can be placed on the PCB outside the sample box, in the next section.

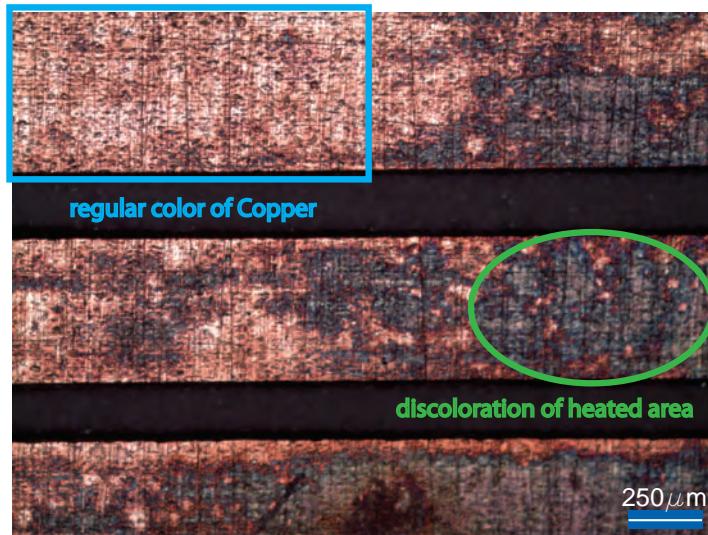


Figure 4.12: Photograph showing the degrading of the copper layer after excessive heat exposure during the soldering process.

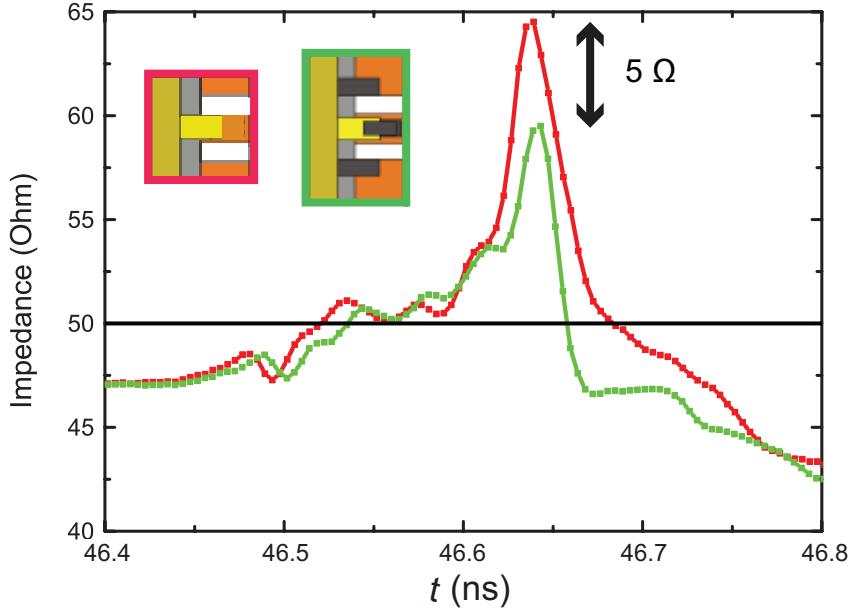


Figure 4.13: Overview of achievements during the connector-PCB matching series. Comparison of first (red; see Fig. 4.7 with only pressure connection) and last measurement (green; from Fig. 4.11 with soldered conductor and ground planes).

4.1.3 Design parameters and performance of PCBs with surface-mount mini-SMP connectors

According to the results from the previous section, soldering is the preferable connection type but also somewhat unreliable, possibly damaging the sample package. To include this beneficial technique nonetheless while also avoiding the observed negative effects, a new connector type is tested: the surface-mount mini-SMP. It is designed specifically for this particular treatment, so no damage to this component can be expected from the soldering process. The surface-mount connectors are soldered to the PCB in a controlled way using a hotplate. The PCB is placed directly on the hot plate without its box. Therefore, unnecessary heating can be avoided because of the excellent thermal conductivity of copper. This minimizes the danger of a deteriorated PCB performance.

In this section, a small summary is presented, giving an overview of general characteristics of the design. But beforehand, *Rogers 3010* is analyzed to guarantee that the characteristic impedance of the designed waveguides is as close as possible to 50Ω . Therefore, the PCB from Sec. 4.1.2 is reinvestigated with the focus on its dielectric constant. In this way, we can verify equations, test calculation methods and compare the measured data with the datasheet [25].

First, the TDR data for this PCB is shown in Fig. 4.14, where measurements at room temperature (approximately 300 K) and at 4.2 K are presented for a soldered connector pin and no ground plane connection. We can clearly identify the PCB between the two peaks marking the connectors. Taking the average over the yellow

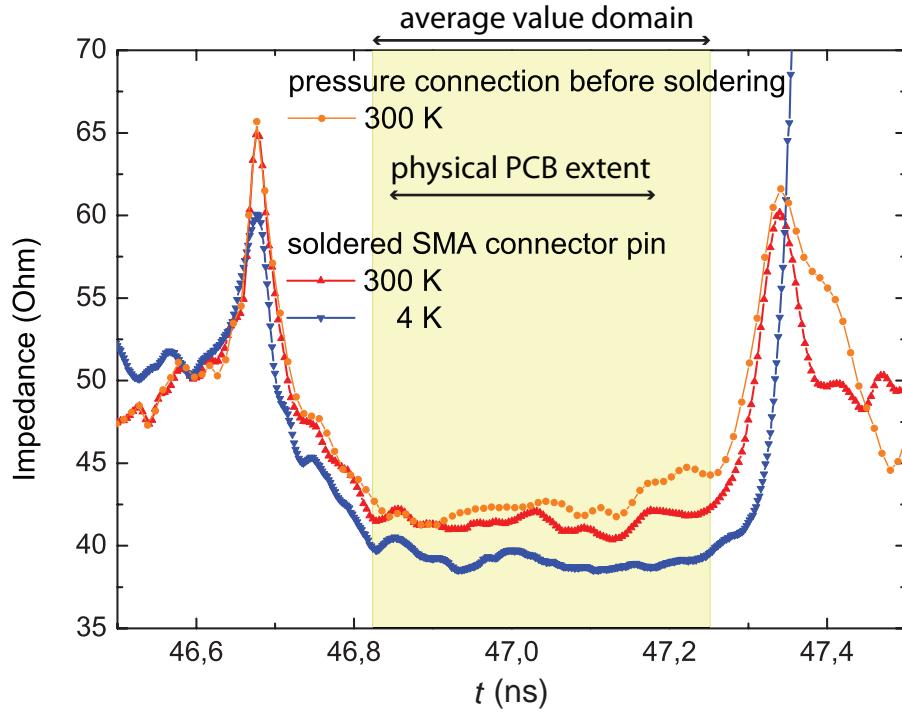


Figure 4.14: Characteristic impedance for certain temperatures extracted from TDR measurements. The measured port for all three experiments is the same, and likewise is the connector; the PCB is the one used throughout Sec. 4.1.2. The dashed line marks the possible physical extension of the PCB.

Table 4.1: Characteristic impedance for certain temperatures extracted from TDR measurements seen in Fig. 4.14 for soldered SMA connector pin. Z_0 for the pre-soldering PCB at 300 K is $43.5 \pm 0.9 \Omega$.

4.2 K	300 K
$39.9 \pm 1.2 \Omega$	$41.4 \pm 0.5 \Omega$

region in Fig. 4.14, we can extract the characteristic impedance of the waveguide on the PCB for both temperatures. The values are given in Tab. 4.1.

The equations presented in Sec. 2.1 are now employed and compared to the measured data. The PCB itself is a single-layer CBCPW and its characteristic impedance Z_0 is given by Eq. (2.18), using the expressions for ϵ_{eff} introduced in Eq. (2.20) and C_{air} [Eq. (2.2)]. With the parameters for width ($w = 490 \mu\text{m}$), gap ($g = 230 \mu\text{m}$), substrate thickness ($h = 635 \mu\text{m}$) and the distance to the lid (approximately $h_1 = 7000 \mu\text{m}$), the k arguments can be calculated. According to Eq. (2.22), this gives $k_3 = 0.51597$ for the substrate and $k = 0.51613$ for air, so almost identical values. Since both arguments are smaller than $1/\sqrt{2} = 0.70\dots$, the approximation presented

in Eq. (2.5) can be used and the result is 0.767 for both values.³ Therefore, q as defined in Eq. (2.21) is approximately 0.5, resulting in an effective permittivity of 5.6 for a dielectric constant of *Rogers* of 10.2 at room temperature as given by the *Rogers data sheet* [25]. Accordingly, the characteristic impedance of the PCB should be 51.4Ω . This result differs significantly from the experimental value of $41.4 \pm 0.5\Omega$. Inserting the same parameters in the program *TX-Line* [38] (with conductor thickness $t = 35\mu\text{m}$), a characteristic impedance of 42.2Ω is computed for a CBCPW at 10 GHz (with regards to Ref. [25]). Changing the frequency to 20 GHz or 30 GHz, the possible bandwidths of the *80E08 ESM* [34], only modifies the result negligible. Using a permittivity of 10.5 on the other hand, a value included in the domain of uncertainty provided by the *Rogers Corporation*, gives a characteristic impedance of 41.7Ω . This value is in excellent accordance(/agreement) with the measured data and confirms the reliability of the program *TX-Line* which is used from now on rather than analytical formulas to calculate design parameters. To verify the dielectric constant of *Rogers 3010* at low temperatures, the used permittivity value is adjusted until the characteristic impedance matches the measured data. For $\epsilon_r = 11.55$, the measured impedance $Z_0 = 39.9\Omega$ can be realised. Consequently, ϵ_{eff} changes to 6.275 for the above described q of 0.5. With Eq. (2.19) and $v = x/\Delta t$, the marked area from Fig. 4.14 of 'length' $\Delta t = 0.42\text{ ns}$, utilized to determine the average/mean value, corresponds to a phycisal length x of 5 cm. For the real waveguide length of 4 cm, a time span of $\Delta t = 0.33\text{ ns}$ is determined instead, using the same phase velocity.⁴ This leads to the conclusion, that the effect of the connectors is even more significant than expected.

Figure 4.15 compares the results for the dielectric constant of *Rogers 3010* evaluated with *TX-Line* to the denominated values for the temperature dependency from the *Rogers 3010* data sheet [26] with a range of ± 0.3 , marked as the grey area. The uncertainty of the measured numbers is an estimation, resulting from combined uncertainties, for example when determing width and gap magnitudes with a range of at least $\pm 5\mu\text{m}$ or the exact assignment of PCB and connectors made in Sec. 3.3. The comparison shows that the measured values at low temperatures are close to the range expected from an extrapolation of the datasheet values. Therefore, $\epsilon_r = 11.55$ is used for width and gap evaluation with *TX-Line*, to accommodate the real measurement environment of liquid Helium.

With regarads to the actual PCB design, where a metallization process is necessarily included in order to creat vias, the effects of conductor thickness variation are calculated as well. For a typical increase of the textured top metal facing from $35\mu\text{m}$ to $50\mu\text{m}$, the characteristic impedance Z_0 is expected to further reduce by 0.8Ω . This change is not in consent with the assumption of copper being a nearly perfect conductor and has not been considered in the discussion of the CPW presented in

³For an integral of the first order, only the term proportional to m is considered. Including the second term with m^2 as well would result in $k_3 = 0.79$.

⁴This actual time span is also included in the figure, but note that only the period can be depicted with no specific starting point.

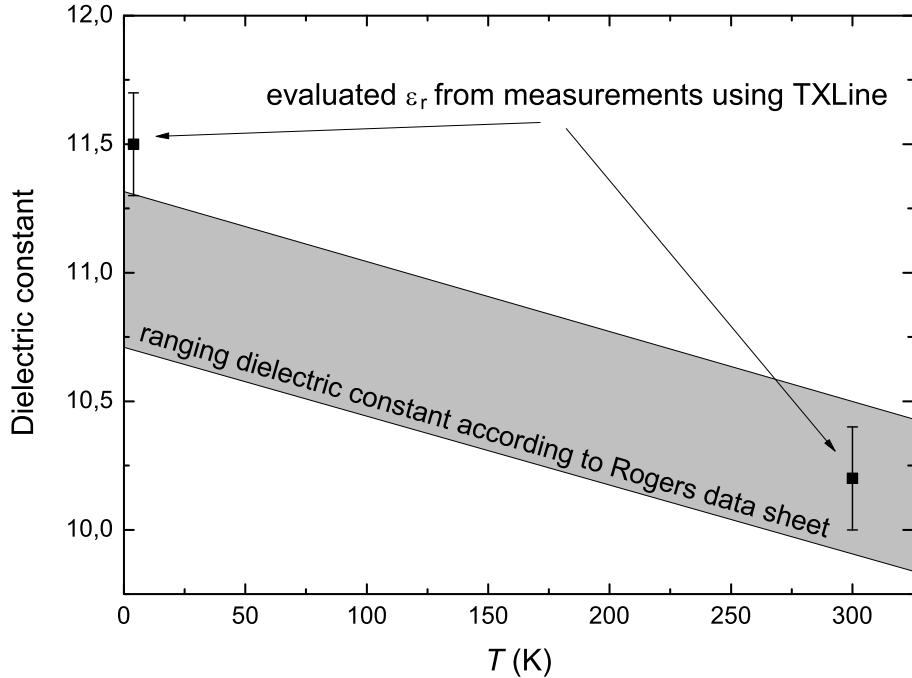


Figure 4.15: Measured temperature dependence of the dielectric constant of *Rogers 3010*.

Sec. 2.1. Since values computed with *TX-Line* match well with the measured ones, this prediction should be taken into account for new designs.

Furthermore, the waveguides on the PCB are assumed to have infinitely wide ground planes because their width is not identical from a symmetrical perspective, a circumstance not considered in detail, but also not explicitly included in the computation with *TX-Line*. Unfortunately, the exact equations used during computation are unknown, so the possibility remains that typical numbers of a FWCPW are taken into account indeed. In addition, the already mentioned dependency of conductor thickness on characteristic impedance depicted during computation could at least decrease the discrepancy between predicted and measured values. It should be mentioned that not considering a top metal cover results in the same value of ϵ_{eff} and an increased characteristic impedance of 51.9Ω , see Ref. [11] for more information about the derivation. This is in accordance with the measurements presented in App. D.

In the following, the performance of several surface-mount PCBs is depicted to get a general overview of what to expect and how to verify the design parameters. All of these designs are as described in Sec. 3.2.1 and utilize the laminated substrate *Rogers 3010*. According to the company doing the texturing and metallization, metal thickness ranges between 50 and 60 μm . The resulting vias are approximately 400 μm in diameter (depending on metallization) and have an identical distance between one another of also 400 μm . Width and gap variations ensure a universal characterization and a chip is not yet included.

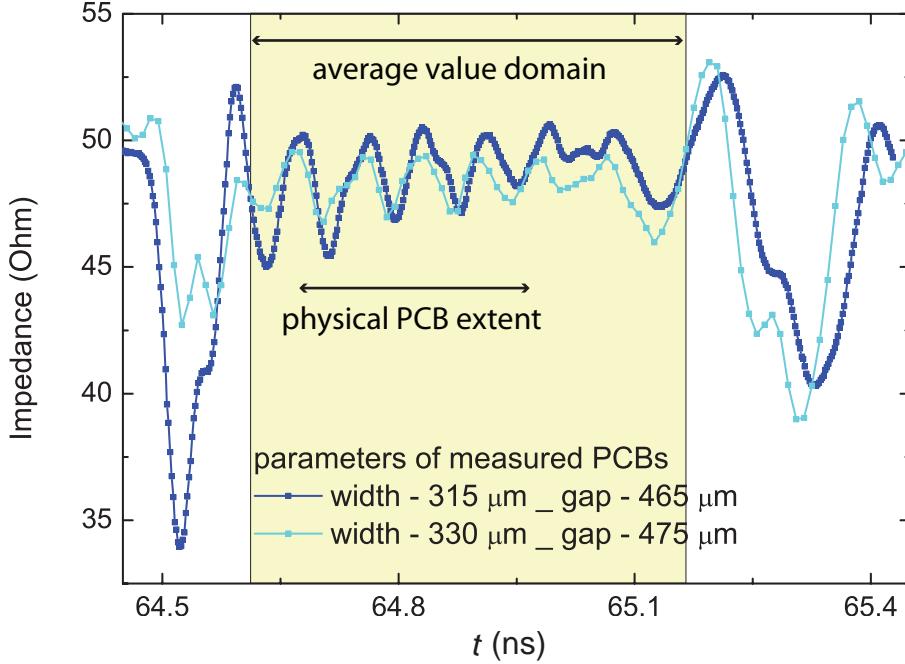


Figure 4.16: TDR analysis of surface-mount PCBs with various design parameters for the CPWs, conducted at 4 K.

Table 4.2: Measured and computed characteristic impedance for the PCBs presented in Fig. 4.16. For the computations, thickness of $t = 60 \mu\text{m}$ and permittivity $\epsilon_r = 11.5$ are assumed. Note that only the width value is directly given, the appropriate gap parameter can be extracted from Fig. 4.16.

width parameter (μm)	315	330
measured impedance (Ω)	48.7 ± 1.4	48.2 ± 0.9
computed impedance (Ω)	52.8	52.1

The measured impedance for the PCB with $w = 315 \mu\text{m}$ is $48.7 \pm 1.4 \Omega$. The corresponding characteristic impedance for a CBCPW with $\epsilon_r = 11.5$ and a thickness t of $60 \mu\text{m}$ is 52.8Ω . For $t = 55 \mu\text{m}$, an impedance of 53Ω is calculated⁵. An overview over all numbers, including the second examined design, is given in Tab. 4.2. Again, a comparison of the marked area with the physical dimensions is conducted.

In order to achieve a characteristic impedance of 50Ω , calculated using *TX-Line*, a dielectric constant $\epsilon_r = 13$ is necessary for the denoted values of w , g and t ($t = 60 \mu\text{m}$) at 10 GHz. This result lies within the uncertainty of the measured value with $\pm 1.4 \Omega$.⁶ and corresponds to a physical conductor length x of 6 cm, while the actual length is $x = 3.7 \text{ cm}$. Therefore, using $\Delta t = x/v$, the actual time span

⁵With regards to the uncertainty of the total copper thickness from additional layers during metallization, other values for t are analyzed as well.

⁶In order to achieve a characteristic impedance of 49Ω , $\epsilon_r = 13.6$ is required, but this value appears unrealistically large at this point.

necessary for a wave with velocity v_{ph} to cross the PCB can be calculated. The result equals only 62 % of the assumed extension for the average value domain with 1.16 ns. This again indicates a significant extension of the connectors in the time domain since the assumed extension of the PCB is derived from the results of Sec. 3.3. For $\epsilon_r = 11.55$, x would correspond to 22 cm! Although there is still a noticeable discrepancy between the expected and the measured dielectric constant (see Tab. 4.2) of the *Rogers 3010* substrate, we also clearly see the positive effect of our careful analysis. The characteristic impedance of the waveguide on the surface-mount connector PCB is now much closer to the desired 50Ω than that of the old press-contact connector PCB. The ripples in the PCB section of the TDR traces can again be attributed to multiply reflected probe pulses. This interpretation is supported by the observation that the ripple amplitude is larger for the trace with larger connector impedance mismatch.

4.1.4 Comparison between press-contact and surface-mount connector sample holder

This section contrasts the efficiency of the two design approaches with the PCB: press-contact and surface-mount connectors. This comparison can not rely solely on the measured performance, but must also include other essential factors. These consist of reproducibility in general, implementation techniques and their possible reversibility. Included within the PCB is also a calibration chip as seen in Fig. 4.2 a), with bonding between chip and PCB conductors and ground planes.

Reproducibility is a major criterion in our experiments. The setup with SMA connectors (see Fig. 3.5) does not satisfy this crucial criterion. Evidence can be found in Fig. 4.17, where the measured data of a 16 " *minibend* cable (40.6 cm) connecting the TDR with various ports of a PCB placed inside a box is shown. For these measurements, connector and PCB are connected according to Fig. 3.6, with bonds linking the corresponding ground planes. Most problems are accessible directly. First, when assuming identical connectors, the supposedly identical connections (ports 1 through 3) result in very different data with peak heights ranging between 70Ω (port 1) and below 65Ω (port 3). This is a major problem because it prohibits reproducible experimentations. Therefore, the method with pressure contacts is too unreliable, sometimes even resulting in open contacts (see Fig. 4.9), and is also likely to damage the sensible connector pins when elevating the PCB excessively. As for the performance, the total mismatch of up to 20Ω is rather unsatisfactory as well. In addition, the PCB impedance is not 50 , but 47.5Ω .

In comparison, Fig. 4.18 presents the data for a PCB with mini-SMP connectors. For these measurements, the PCB is cooled repeatedly below 77 K in liquid Nitrogen to simulate consecutive low temperature experiments. After a reheating period of approximately five minutes, its performance is analysed with the TDR. We find that the discrepancy to the previous measurements reduces with every cycle after the

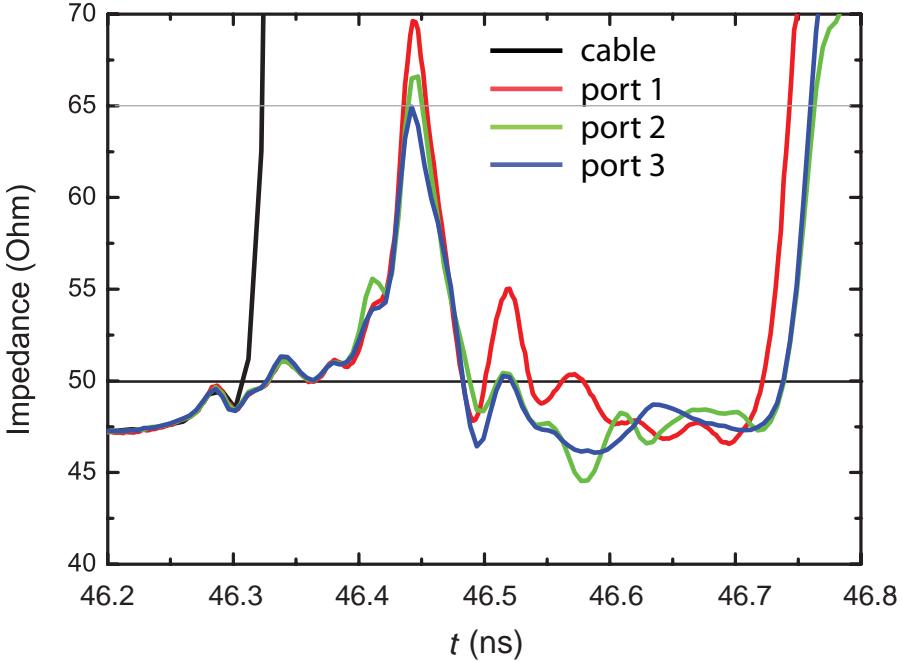


Figure 4.17: TDR measurement at room temperature of press-contact PCB design (with chip) as seen in Fig. 3.5 a). Also included is the measurement of the cable without the sample package, effectively resulting in an open termination.

initial cooldown. This implies that the properties evolve towards a stable condition after the initial *shock*, a behaviour that is in agreement with other cycling experiments [39]. The overall aberration of less than 1Ω is negligible. Higher differences observed in b) are mainly a result of a shifting along the x-axis and not a variation of the characteristic impedance. Note that the PCB has not been cooled ahead of the first measurement.

Furthermore, there is of course the general performance of the connection technique. With regards to reflection losses, the transition areas are first examined with the TDR. A comparison is shown in Fig. 4.19 of a press-contact type PCB as seen in Sec. 4.1.1 and the surface-mount variation. It can be seen that with the switch to mini-SMP connectors, the peak that marks the intersection onto the PCB can be decreased from 20Ω to 10Ω . For the minimal measured peak reduction of 5Ω , this implies a reduction of reflection losses from 15 % to approximately 11 % according to Eq. (3.1). The PCB's deviating impedance already makes a complete redesign with adapted width and gap parameters necessary. Furthermore, as the waveguide length on the PCB are proven to be of importance (see 4.1.1), careful selection of these lengths must be considered as well to avoid spurious resonances. This is achieved within the surface-mount PCB type, designed to a phase shift of 260° between connector and chip (15.5 mm) at 5.6 GHz (with $\epsilon_r = 11.55$) and a more closely matched characteristic impedance. As indicated during the analysis of Fig. 4.5, avoiding spurious resonance is impossible throughout the whole measured frequency range

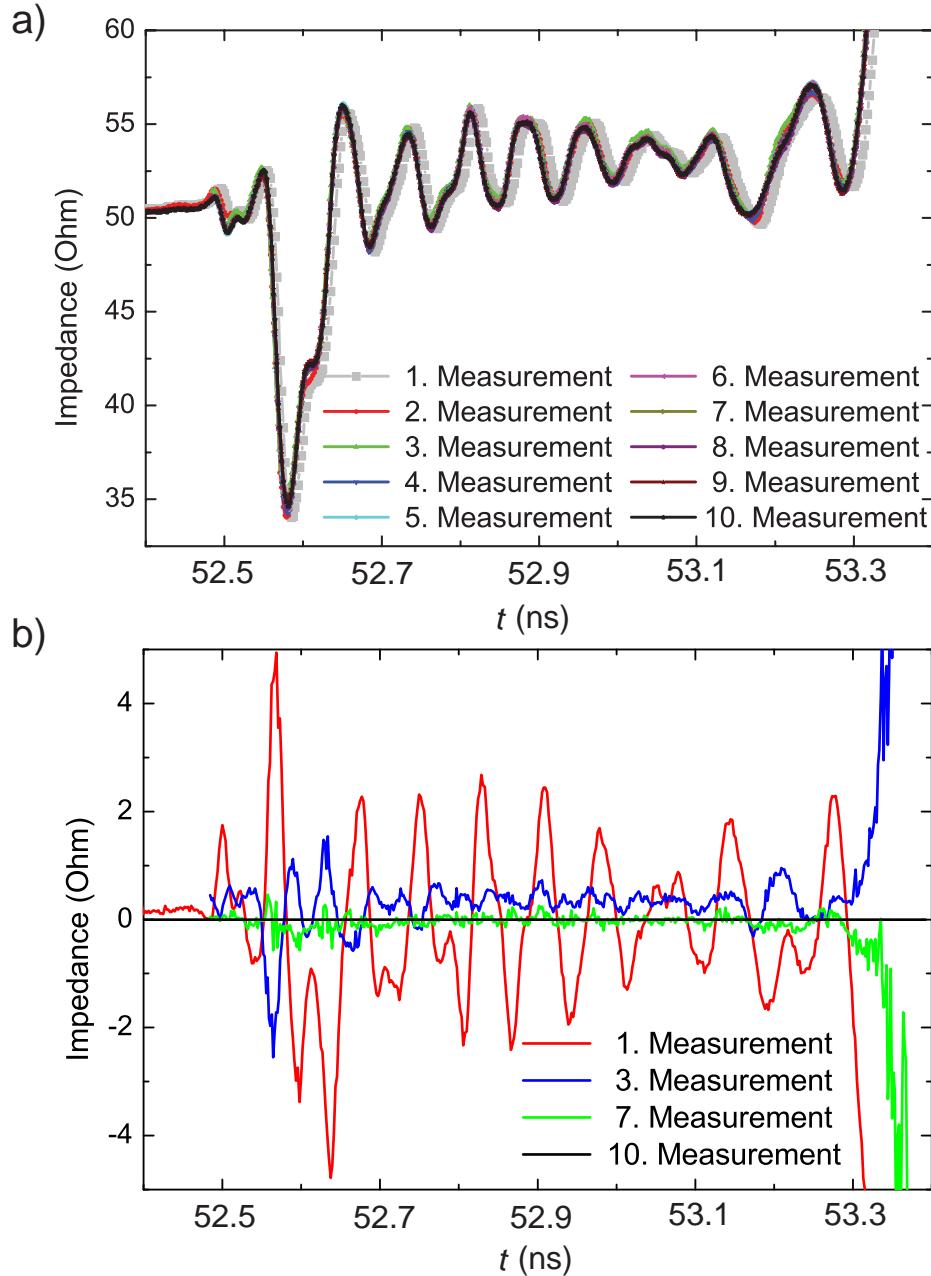


Figure 4.18: Results of thermal cycling measurements in liquid nitrogen at 77 K in a). For illustration, the difference of measurements correspondent to the tenth one are plotted in b).

(0 GHz to 10 GHz) is impossible, but feasible in the important region around the working frequency of the planned beam splitter. Regarding the performance, soldering already proved to be a enhanced connection type, there is however the problem of the heating process discussed in Sec. 4.1.2. Surface-mount connectors on the other hand benefit from the adapted heat exposure which can be reduced to the required minimum within a reproducible process, increasing the probability of retaining the improved transition performance. In addition, any amount of (mini-SMP) connec-

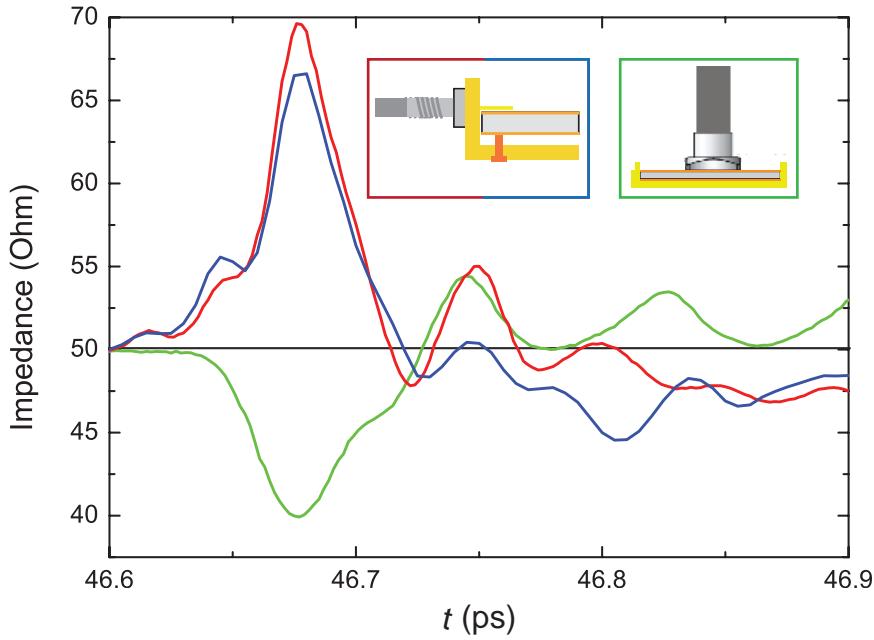


Figure 4.19: TDR data of the transition onto the PCB for a mini-SMP connector and two exemplary measurements that correspond to the press-contact PCB design without any connection enhancements.

tors can be assembled during one soldering process, although the required time may vary by 10 – 20 % or rather a couple of seconds, further limiting damaging effects. The overall performance quality of soldered connections is retained. In comparison, the connectivity is improved, lowering reflection losses by approximately 15 % or a mismatch reduction of at least 5Ω respectively.

In conclusion, switching to a new PCB design using mini-SMP connectors proves to be successful. It features the advantageous connection quality of soldering while indicating to eliminate most negative effects due to the hot air gun by using a hot plate instead. The new connectors further guarantee reproducibility and a reliable connection is achieved. Therefore, a PCB with surface-mount mini-SMP connectors is established as the new setup for the rest of this thesis, combining low reflection losses with mechanical stability.

4.1.5 Analysis of PCB/chip connection with surface-mount sample holder using mini-SMP connectors

With the discovery of a reliable connection method between setup, connector and PCB, the next critical connection can be examined. In this section, the transition from PCB to chip is analysed in a low temperature environment with a PCB of the surface-mount type. Taking the asymmetry of the sample package into account, the analysis of the upper two waveguides is necessary for a complete overview (see Fig. 4.20). Both conductors as well as all four corresponding ports are measured during the same cooldown. Therefore, a combination of *GPPO* and *SCA97047* adaptors has to be used (illustrated in the picture presented in Fig. 4.21). Also, low-loss copper-clad coaxial cables are used in the cryostat (see App. C). Unfortunately, a false time frame for port 4 has been used, resulting in the uselessness of measured data. In the following analysis, the inferior adaptor (port 3) has to be taken into account as indicated in Fig. 3.11 where a discrepancy of up to 2Ω is detected. However, the concluding analysis at the end of this section does consider this fact.

This series is devided again into separate center conductor and ground plane analysis with four cooldowns for each component. With $w = 290\mu\text{m}$ and $g = 490\mu\text{m}$, it is close to an characteristic impedance of 50Ω . Naturally, the PCB has to be adapted by milling to accommodate a chip. Since the chip is arranged symmetrically, it is sufficient to observe the top two waveguides. For better comparison with the initial setup, the calibration design presented in Fig. 4.2 a) is chosen again with the corresponding dip encountered and verified in Sec. 4.1.1 which covers the working frequency of the hybrid ring. Therefore, achievements in transition improvement should have a distinct visual effect in transmission measurements. Differently from Sec. 4.1.2, design and dimensions of the chip do not allow for different techniques besides bonding though. The areas in question are simply to small for another approach, as is exemplified at the relevant points. As a result, only the number of bonds, and thus the connectivity, is increased and the changes to transmission and impedance measured. The data collection is again devided in conductor path and ground planes.

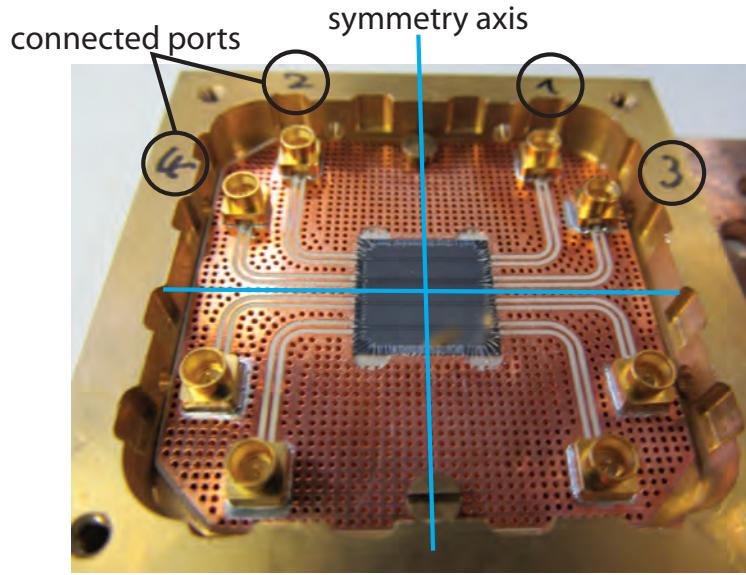


Figure 4.20: To illustrate the symmetry, a picture is shown of the sample package with calibration chip in an advanced state of the measurement series. The superscribed ports have to be measured for a full analysis.

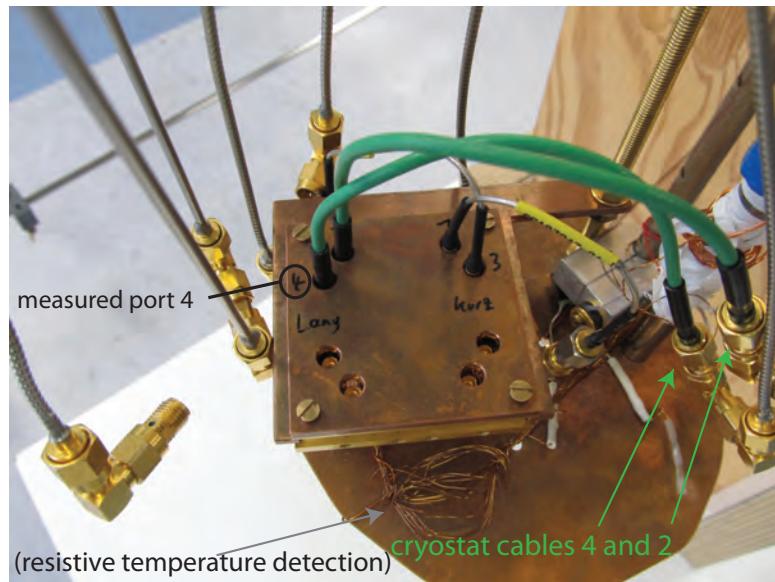


Figure 4.21: Sample box inside the cryostat insert.

Inner conductor

In correspondence with Sec. 4.1.2, the connection with the center conductor is analyzed first. Therefore, the number of bonds is gradually raised for all investigated ports. For the ground plane, a minimum amount of 12 bond connections is applied. A schematic of the setup can be found in Fig. 4.22. The evaluation data for both TDR and VNA measurements are presented in the Fig. 4.23 and Fig. 4.24 as well as Fig. 4.25. With the TDR, the ports 2 and 3 are analyzed to examine the effect of varying surrounding ground plane dimensions. For the VNA, the two paths corresponding to the four denominated ports are measured.

Both ports share a direct/more or less linear dependency of bond quantity to transition quality with saturating peak heights for a sufficient number of bonds. In this measurement, for a total of five bonds per connection between connector and CPW center conductor, the impedance can be lowered to approximately 60Ω . However, the decrease per additional bond is not constant. This is most obvious when comparing the ports directly: for port 3, the increase to two bonds results in a drop of 3Ω when for port 2 peak height is only lowered by 2Ω at most. It seems that the ground plane configuration does affect the performance since this represents the most apparent difference. This may not only be the case for the presented discrepancy but also the absolute values in general. Although the deviation can be reduced by at least 1Ω during this measurement series, port 3 shows an initial maximum at 68Ω compared to 65Ω for port 2.

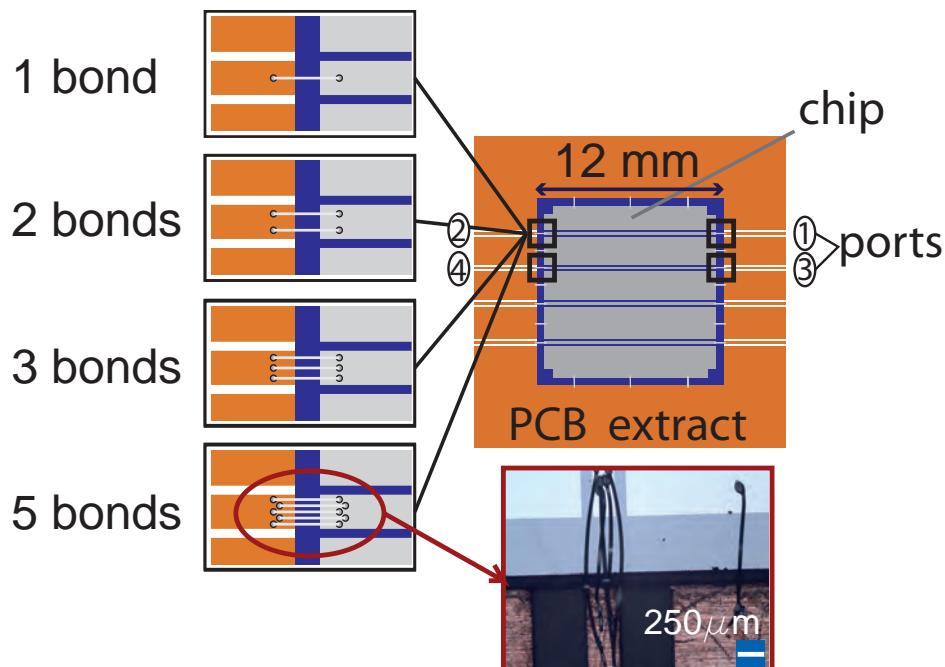


Figure 4.22: Connection between the center conductors on PCB and chip.

Including more than five bonds becomes technically complicated. To illustrate this, a photograph of the chip before the last measurement of the series is included.

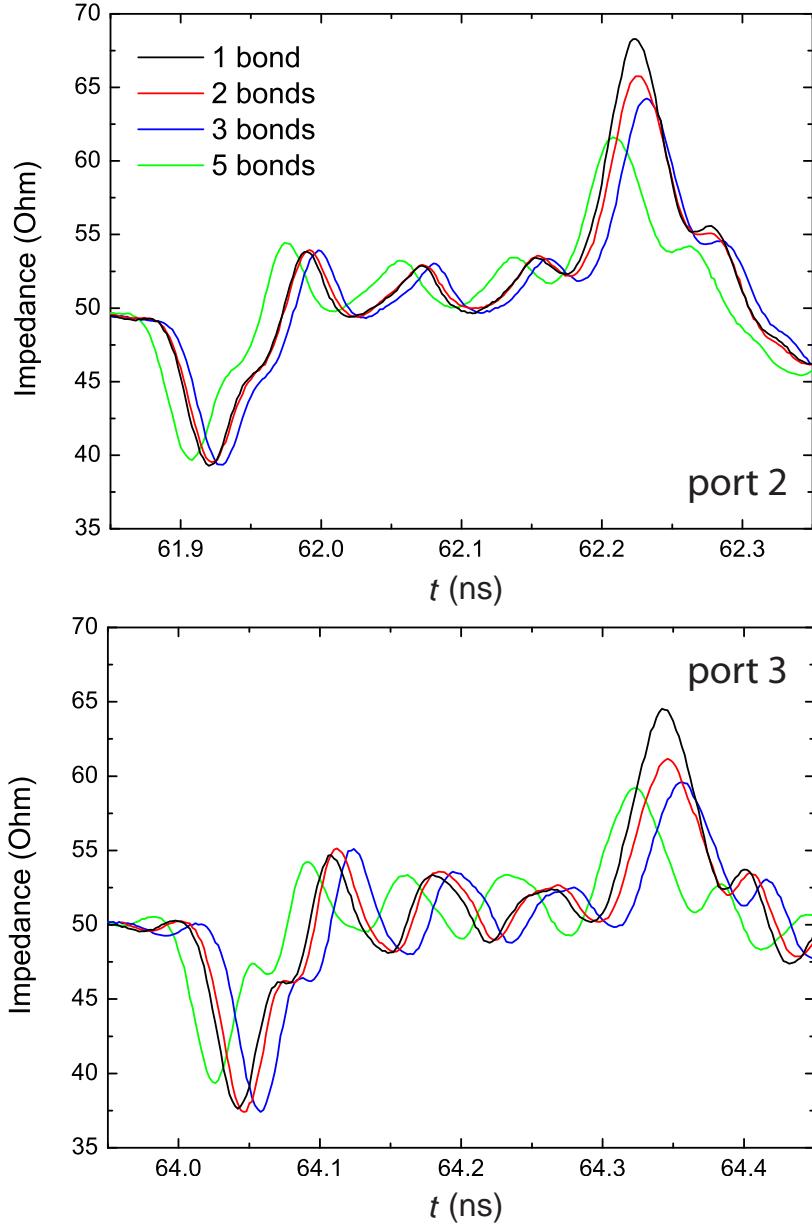


Figure 4.23: Low temperature analysis of setup from Fig. 4.22 for two ports with TDR.

In Fig. 4.24 and Fig. 4.25, transmission measurements along the two paths are shown in the frequency domain. We first notice a series of impressive dips in agreement with the strong mismatch at the PCB-chip transition. We then notice the significant difference between the spectra of the two paths, which we contribute to the different ground plane configurations influencing the spurious resonances. In Fig. 4.24, we see that the dip near 5 GHz shifts to lower frequencies with the increasing number of bonds. This indicates that it is influenced by the boundary condition of the bonds, making the “chip”-mode effectively longer because of reduced reflection effects. In Fig. 4.25 (for the other path), the depth of this dip is drastically reduced and its width increased. Instead, a new dip appears near 3.5 GHz. This

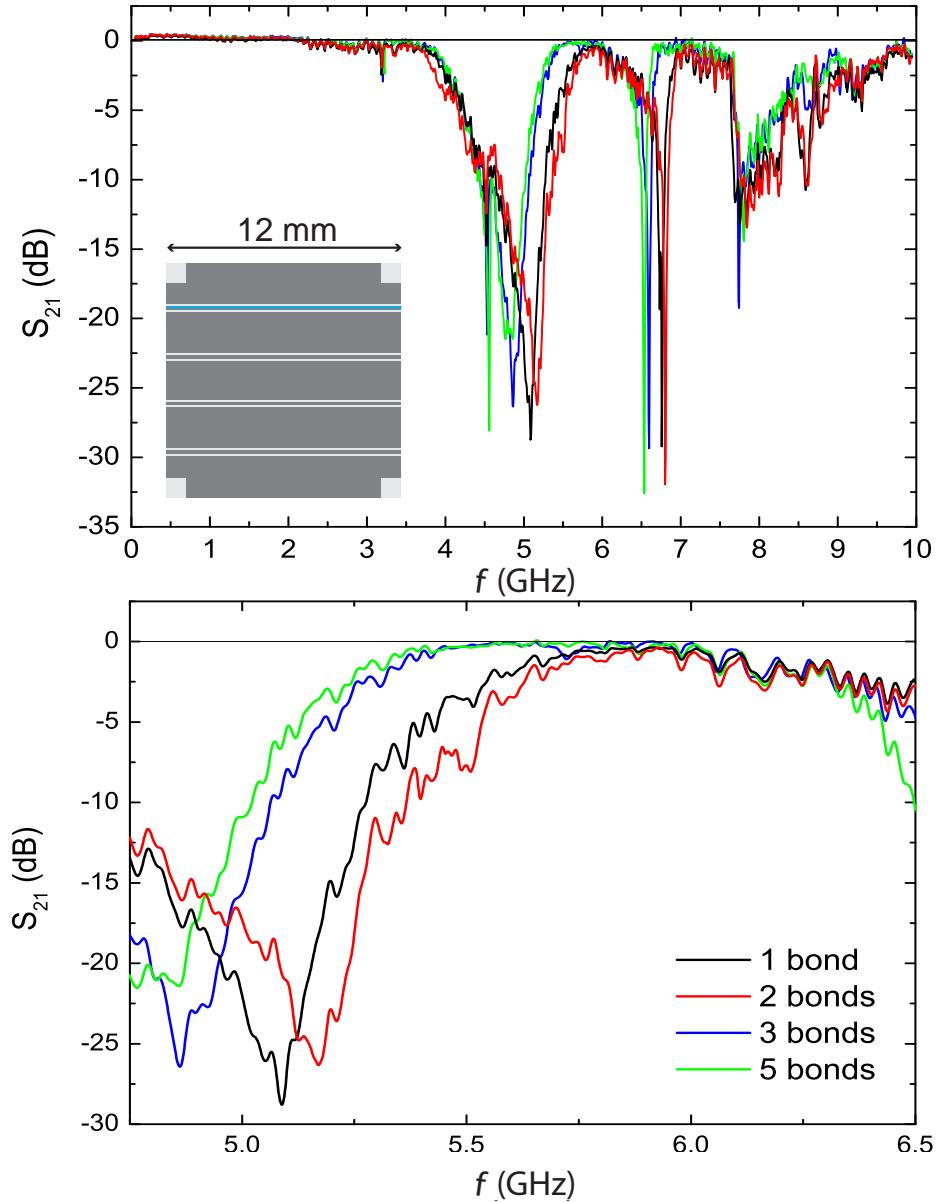


Figure 4.24: VNA data using setup presented in Fig. 4.22 showing S_{21} , the transmission between the ports 1 and 2, for different frequency spans to give a total overview as well as analyzing performance close to the working frequency of the future beam splitter.

indicates that the shallow wide dip is present as a “foot” feature also in Fig. 4.24 and corresponds to the “chip mode”. The comparatively narrow but deep dip could be attributed to an effect of the ground planes. (We further support this idea later when discussing the ground plane bonds.) Finally, we observe the characteristic ripples due to reflections in the long low-loss cryogenic cables in the lower panel of Fig. 4.25. Based on the results in this section, we believe that the PCB-chip connection could be improved further by the use of ribbon bonds. Unfortunately, this variant could not be investigated due to the lack of proper equipment.

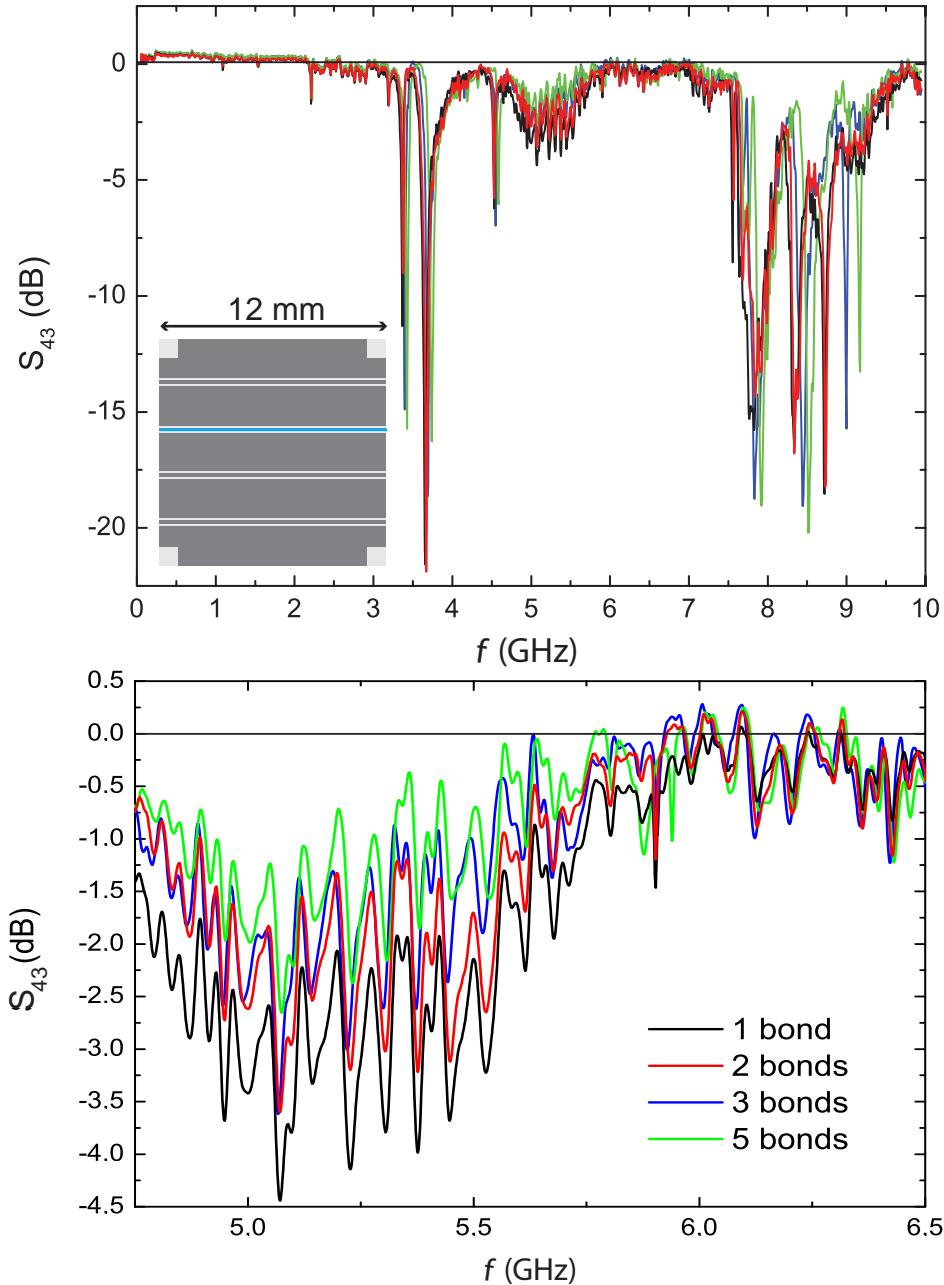


Figure 4.25: VNA data using setup presented in Fig. 4.22 showing S_{43} for different frequency spans to give a total overview as well as analyzing performance close to the working frequency of the future beam splitter.

Ground planes

We next investigate the connection of the ground planes of chip and PCB. This situation is shown in Fig. 4.26. While bonds and maybe ribbon bonds are the only way of connecting PCB and chip conductors, the ground planes have to be connected over a much larger region. For the long edge (red square in Fig. 4.26), silver glue might prove to be a viable possibility instead of using bonds, for it is large and distant enough and as such not as frail for rough application. Soldering paste on the other hand seems inappropriate for this purpose, even when using a hot plate. The heat might destroy the sensible structure or at least influence the physical properties of the dielectric. For this thesis, other possibilities are put aside and the general importance of connectivity is examined instead through variation of bond quantity. In this next measurement series, the effects of ground plane bonding on the general performance at 4K are examined. The total number of bonds is increased in four steps from initially 12 to 184 in the last measurement. The setup for this ground plane analysis, more complex in its consistency than in previous measurements, has to be divided into several regions. For comparable areas with respect to symmetry, the amount of bonds is raised equally for each new measurement. These regions are indicated in Fig. 4.26.

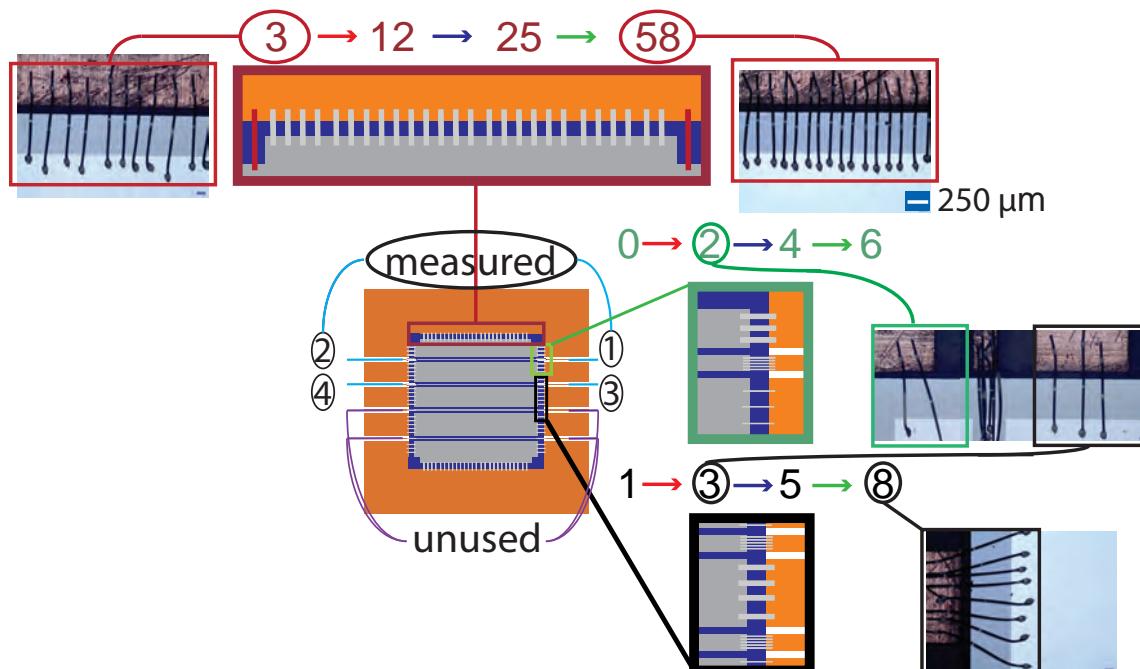


Figure 4.26: The ground plane is divided into several sectors by the conductors. Different characteristic areas are marked with an individual colour. The total number of those bonds rises from 12 in the first measurement to 50 for the second, then 96 and finally 184. The numbers next to the areas represent the bond count of a region for the appropriate measurement. Example photographs of the bonded sample are also shown.

For the TDR analysis presented in Fig. 4.27, the ports 2 and 3 are measured. The initial setup of this series is equivalent to the last one from the conductor examination as depicted in Fig. 4.23 '*5 bonds*'. It can be seen, that independent from the surrounding geometry of a conductor, both transistions to the chip improve to a peak value of 55Ω (equal to 5 % reflection). In addition, no change is observed between the third and last measurements. The shared final peak hight for both conductors indicates that for a well-connected ground plane, the geometry is negligible in regards of reflection losses. However, a certain amount of bonds is required to equilibrate the ground plane potentials and performance is improved until a saturation count of approximately 100 bonds (for this particular structure) is reached. Additional bonds are decreasingly effective in further augmenting the performance. The data of the frequency domain analysis shown in Fig. 4.28 and Fig. 4.29 confirm this conclusion. The VNA measurements also provide support to the assumptions made in the previous section since the very distinct features are reduced for a better linked ground plane. The remaining dips, or generally speaking, the less clean spectrum in Fig. 4.28 is understandable because this path is closer to and therefore more influenced by the unused paths. Still, the zoom-ins of Fig. 4.28 and Fig. 4.29 show how clean the spectrum has become in the relevant frequency range. The remaining small ripples can again be attributed to cable reflections and are expected to disappear by using, for example, attenuators at the sample box inputs.

An overview of the performance improvement in the PCB-chip connection by appropriate bonding is shown in Fig. 4.30 and Fig. 4.31 (time domain) and in Fig. 4.32 (frequency domain). The connector mismatch decreases by up to 15Ω , significantly reducing the reflection losses. This can also be seen in the transmission data, although here the ground plane bonding plays a key role.

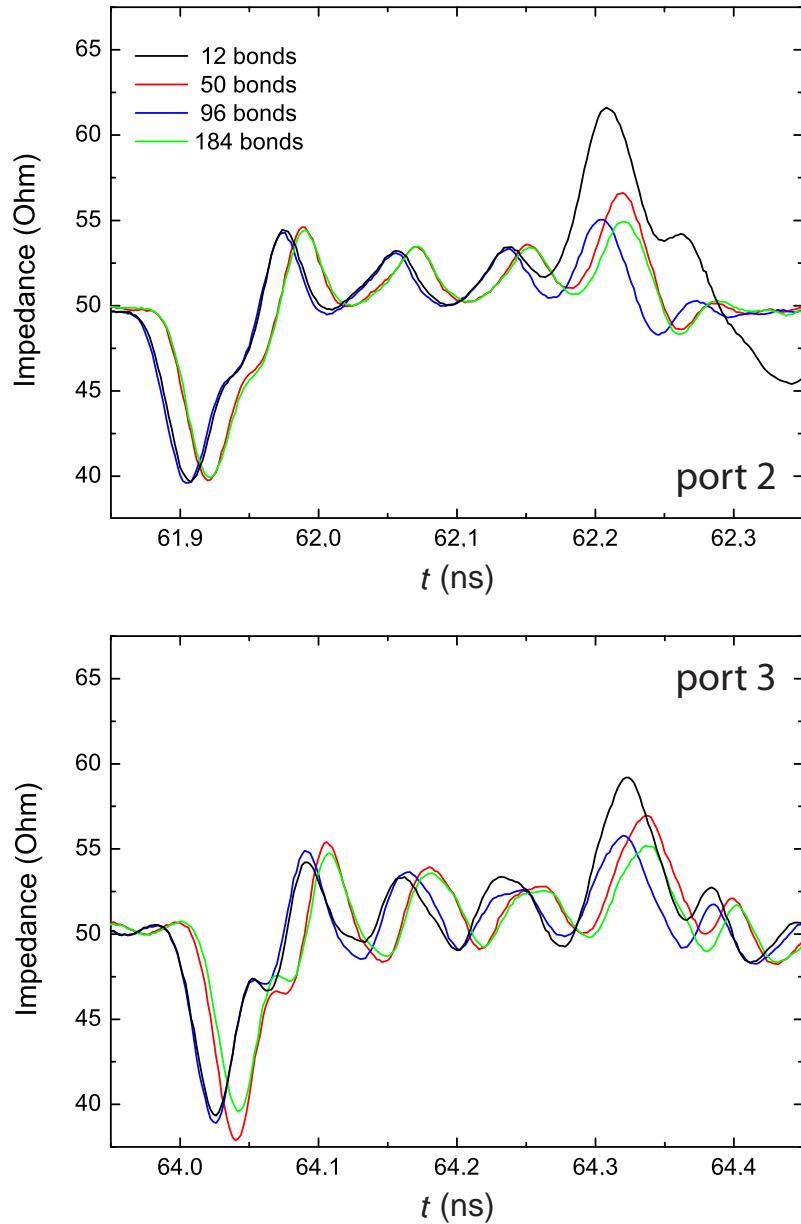


Figure 4.27: TDR data for ports 2 and 3, using the setup presented in Fig. 4.26 at low temperatures.

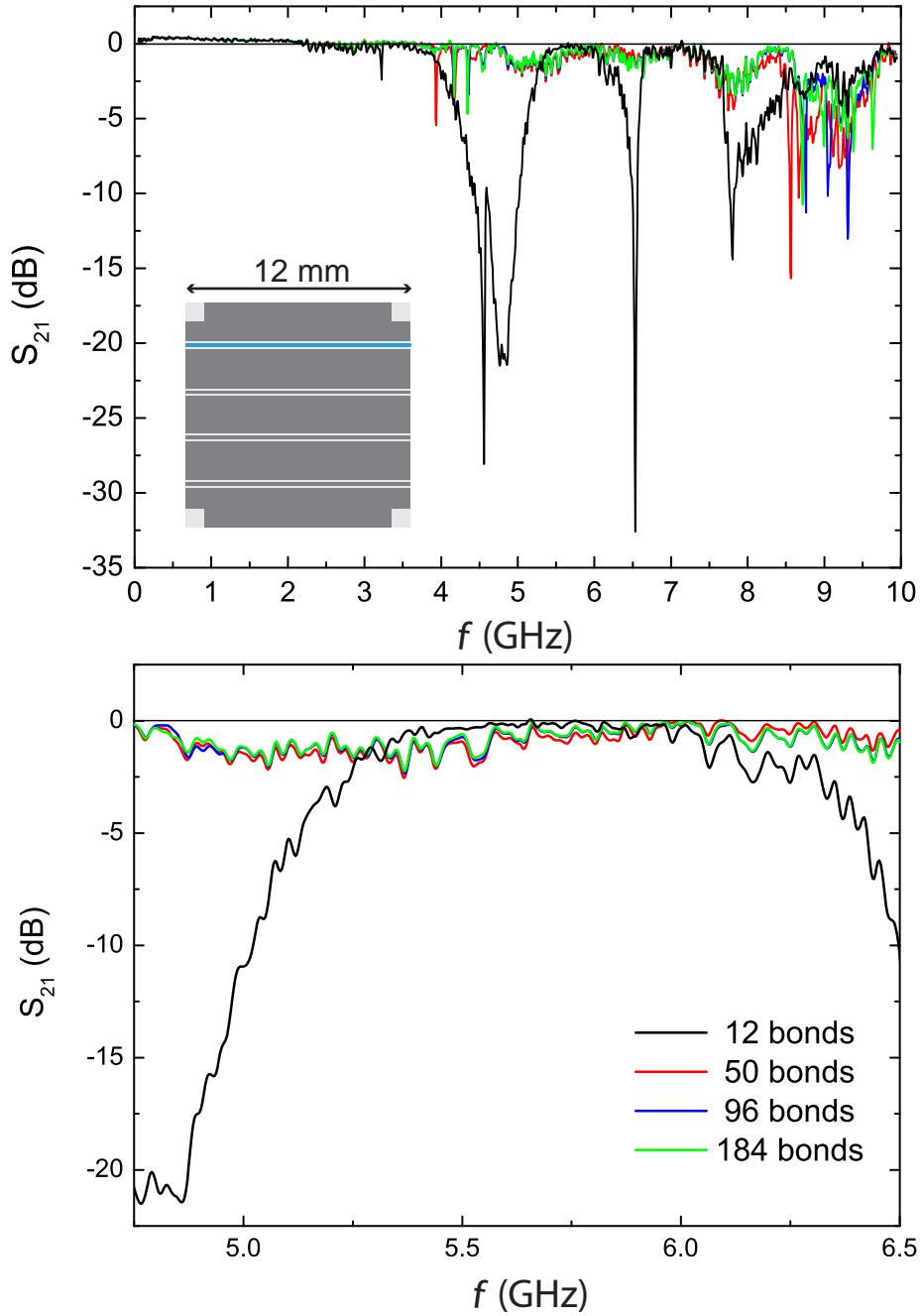


Figure 4.28: VNA data using the setup presented in Fig. 4.26. Transmission of different frequency ranges for S_{21} .

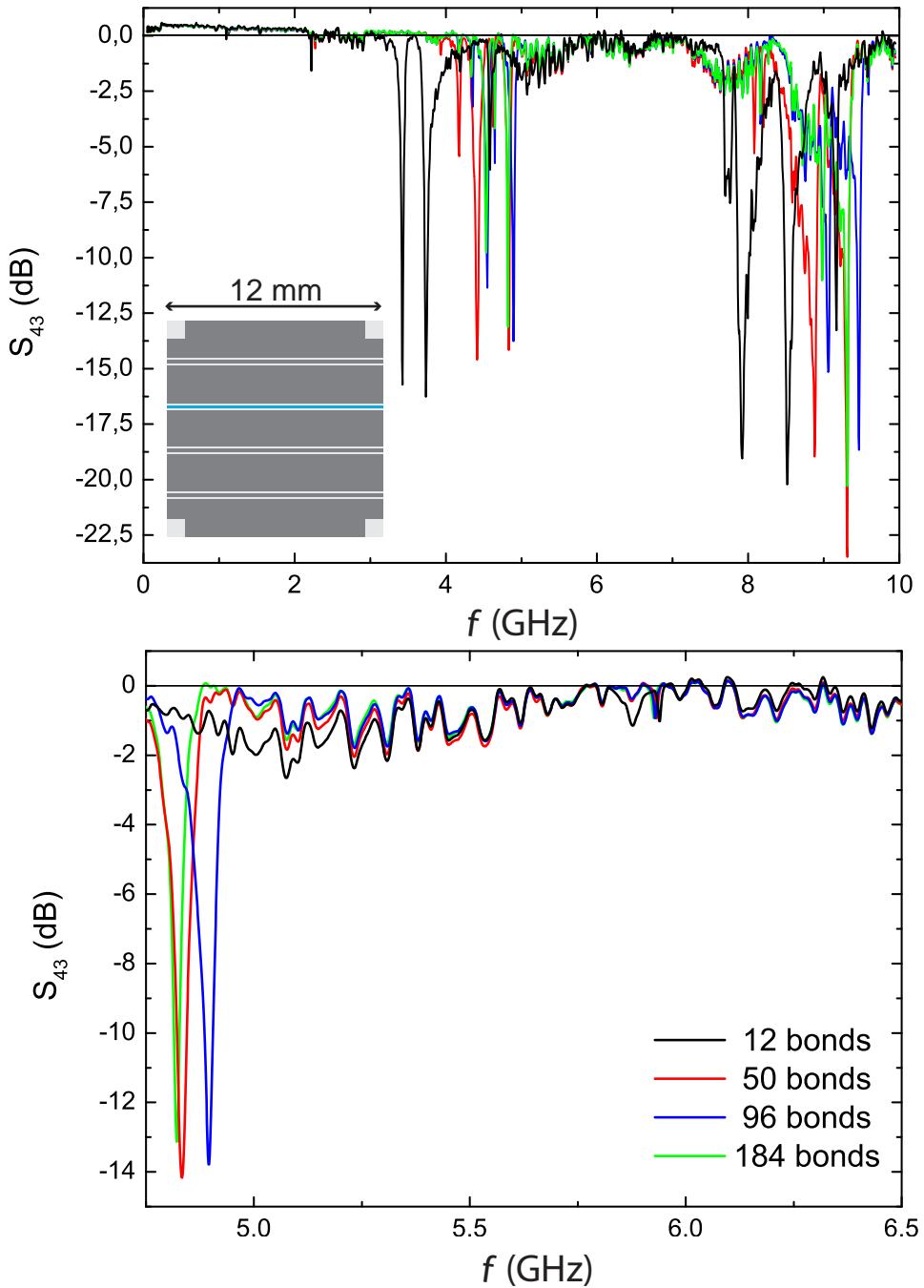


Figure 4.29: VNA data using the setup presented in Fig. 4.26. Transmission of different frequency ranges for S_{43} .

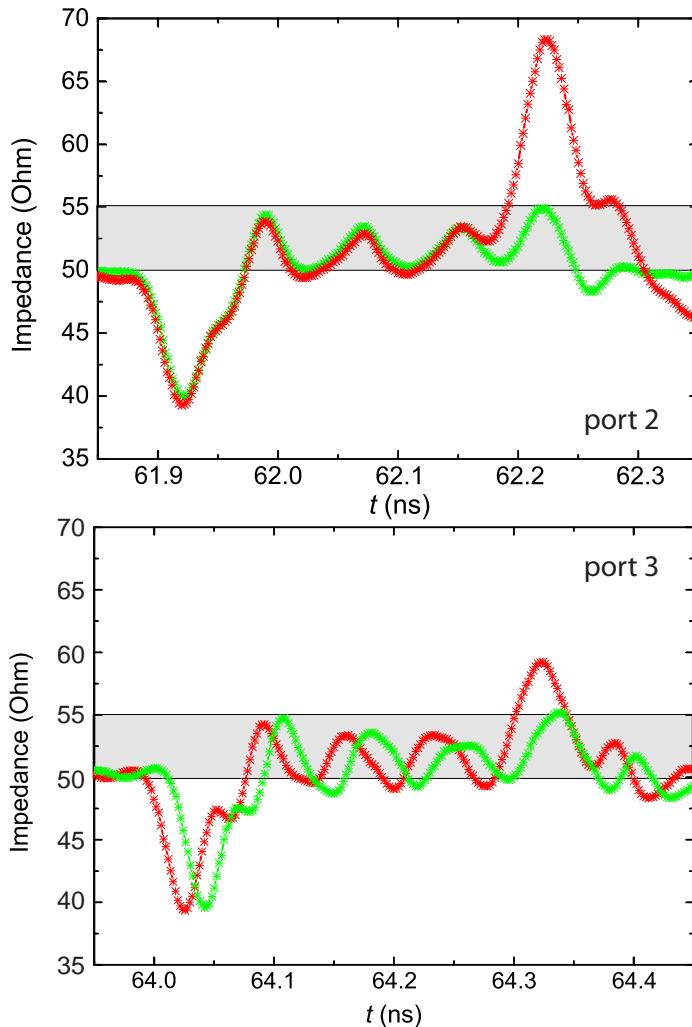


Figure 4.30: Improvement of the TDR signal of the PCB-chip connection via bonding.

critical connection between PCB and chip

1st measurement;
total of 20 bonds



8th measurement;
total of 200 bonds



Figure 4.31: Illustration of this measurement series' first (as seen in Fig. 4.23: '1 bond') and last measurement setup (presented in Fig. 4.27; '184 bonds').

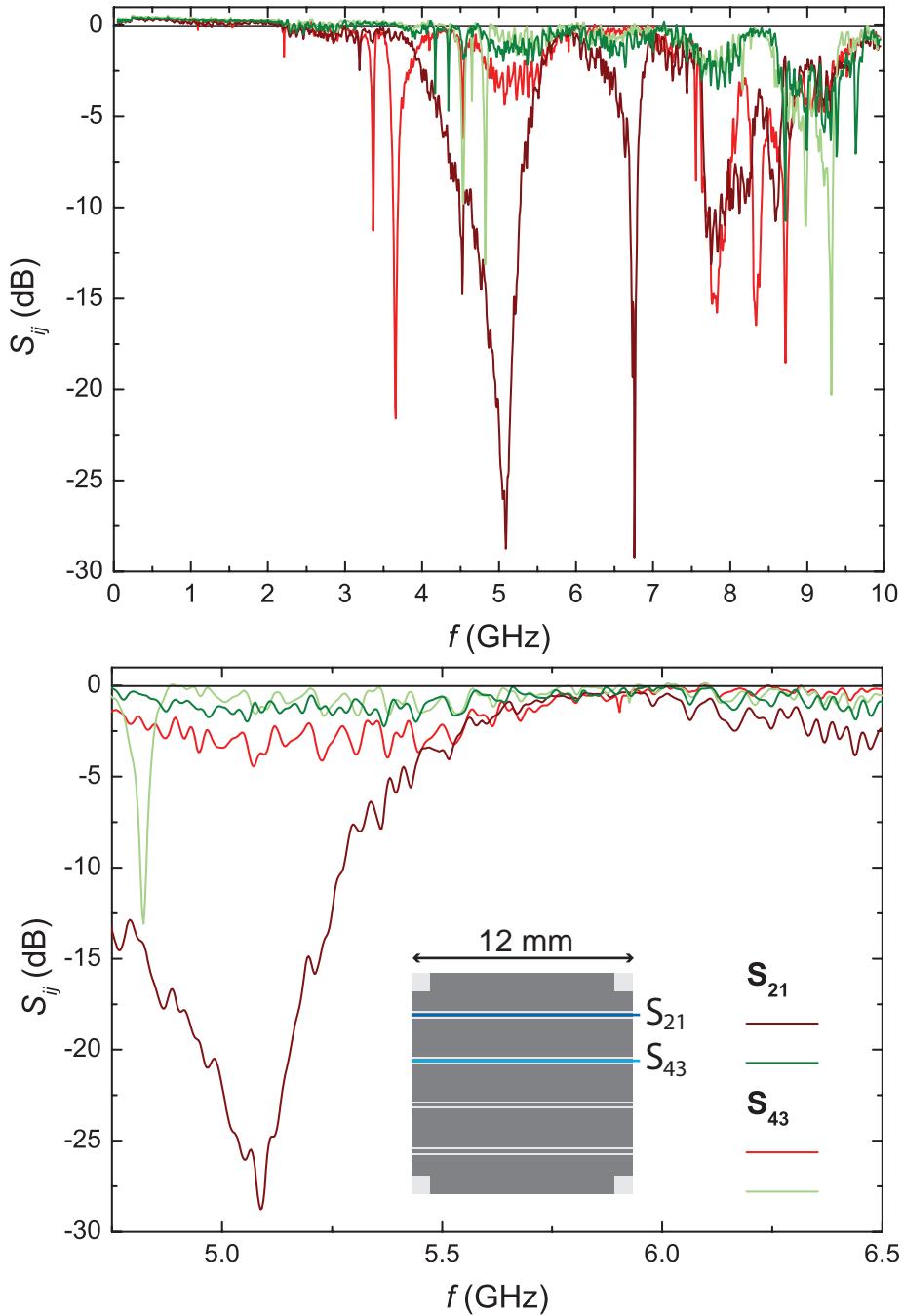


Figure 4.32: Transmission comparison of S_{21} and S_{43} for different frequency spans. Progress between first (red) and last (green) measurement of the series as presented in Fig 4.31 regarding the critical connection between PCB and chip.

Conclusion

The performance analysis of press-contact and surface-mount connectors with the TDR has already been presented in Sec. 4.1.4, where an overall advancement of at

least 15 % in reflection losses could be recognized. In Fig. 4.33, a comparison of the transmission through a calibration chip of the initial setup with press-contact PCBs with the final from Fig. 4.32 (surface-mount connectors and 204 bonds between PCB and chip) is presented. The narrow ripples are artifacts due to reflections in the cables. However, we have improved the performance of the PCB significantly in the relevant frequency band and are now ready to investigate a quadrature hybrid in the optimized sample package.

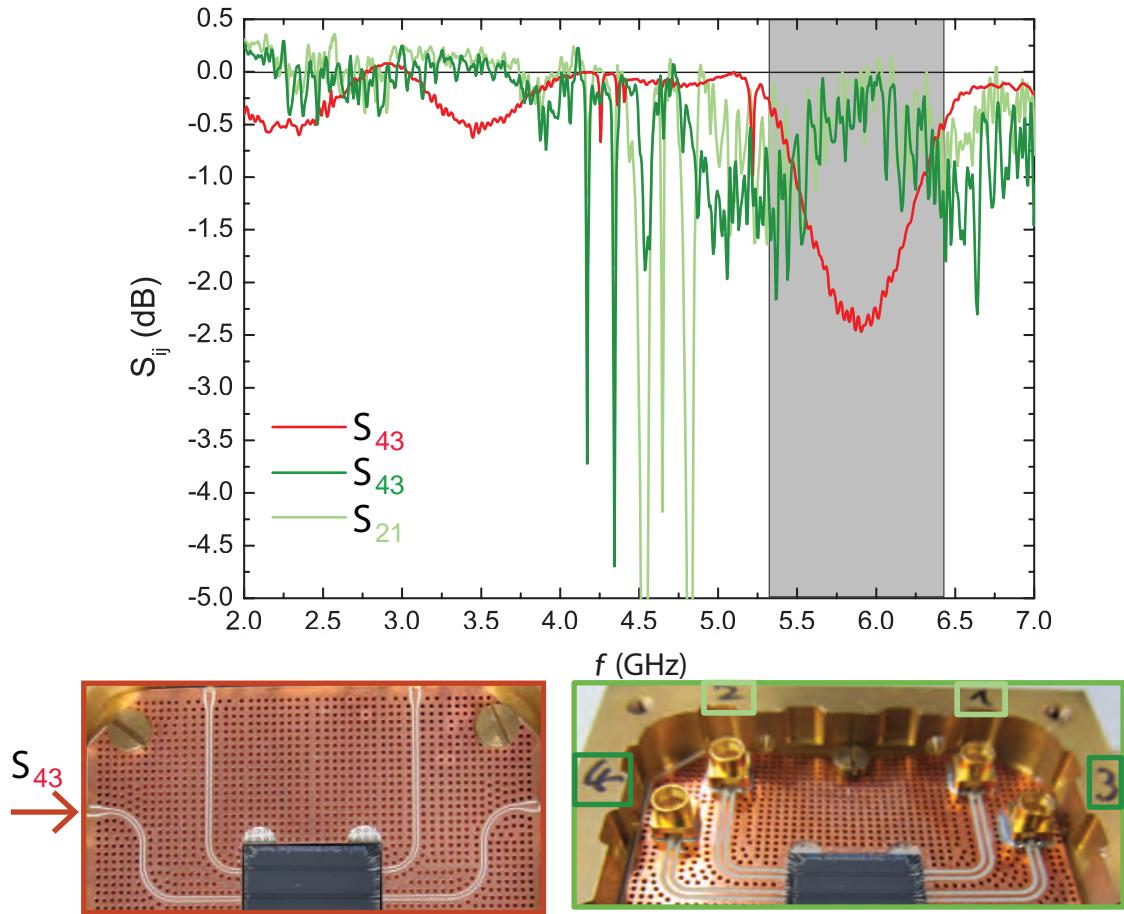


Figure 4.33: Overview of the overall transmission for the initial setup with SMA connectors presented in Fig. 4.3 (Sec. 4.1.1) and the results from the final measurements using the surface-mount mini-SMP connectors for S_{21} and S_{43} as seen in Fig. 4.32.

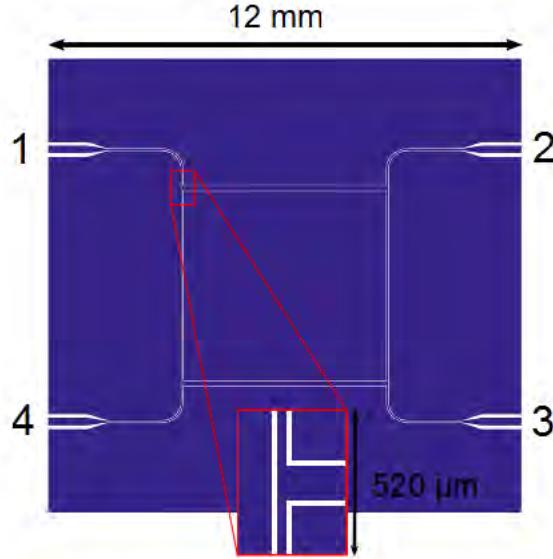


Figure 4.34: Design of the quadrature hybrid ring. With friendly permission from Michael Fischer [37].

Table 4.3: Design parameters of the measured quadrature hybrid seen in Fig. 4.34.

characteristic impedance (Ω)	Width (μm)	Gap (μm)
$Z_0 = 50$	34.4	20
$Z_0/\sqrt{2} = 35.4$	125.2	20

4.2 The 90° hybrid ring

This section discusses the actual quadrature (90°) hybrid which is in general a beam splitter as described in Sec. 2.3⁷. Figure 4.34 shows the layout used for optical lithography (as explained in App. A) which is designed accordingly to the underlying design properties that are also shown in Fig. 2.5 and Tab. 4.3. One notable feature is the broadened waveguide towards the edges. The additional space gained by this enlargement allows the placement of further bonds for an improved connection to the PCB. With a width of 200 μm (gap = 100 μm), up to three bonds in close proximity can be achieved. Utilizing the full length of this wider area, additional bonds can be fitted onto the chip up to a total of at least five. Additionally, a surface-mount PCB with a characteristic impedance of approximately 50 Ω is utilized in agreement with Sec. 4.1.2 (the same PCB in fact). At transitions between waveguides of different dimensions [11], width and gap are narrowed or widened consistently over a length of 0.5 mm. This approach is also called tapering. In total, 150 bonds link PCB and chip with five bonds used for each measured conductor and a total of 12 bonds to connect the isolated section in the center of the hybrid ring structure with the other ground planes of the chip, equally distributed to the (four) ground planes outside.

⁷A single quantum of light, the photon, has a 50 %-chance to appear on either side of the device.

As described in Sec. 2.3, the central structure can be divided into two separate sections with different characteristic impedances: Z_0 and $Z_0/\sqrt{2}$. Each track has the same length $\lambda/4 = 5.172 \pm 0.002$ mm that is dependent on the working frequency⁸. They are related through [40]:

$$\lambda = \frac{v_{\text{ph}}}{f} \quad (4.1)$$

The variation of λ is a consequence of the different parameters for width and gap in the two sections. They are listed in Tab. 4.3. However, a main problem is the determination of exact permittivity values for *Rogers 3010* as discussed in Sec. 4.1.3. Furthermore, the exact behaviour at the T-junctions is unknown. This leaves it unclear, if λ is measured from the center of these junctions of conductors or equals the length of the gap. The resulting minor variation is ignored at this point but has to be remembered when judging the performance of the beam splitter.

Figure 4.36 shows the analysis of a hybrid ring at low temperatures conducted with the four port VNA *ZVA 24* and corresponding calibration measurements [41]. The VNA is connected with the cryostat through 2 m long coaxial cables. To achieve a good resolution, the frequency range of 9.99 GHz comprises 10.000 measurement points with 500 Hz measurement bandwidth of the IF-filter and an average number of cycles 2. The power of the input signal is 10 dBm.

To calibrate the VNA for the analysis of the hybrid ring, certain cable pairs have to be connected and measured. Three of these pairs are necessary in order to obtain a calibration for the three scattering parameters. Since no adaptors are available to connect the *SMA/GPPO* adapter cables directly⁹, the question if the addition of a sample package is necessary at this point does not arise. The setup for these measurements is therefore equivalent to the one for the hybrid ring as seen in Fig. 4.35 but with other chip designs. Corresponding calibration chips are shown with their measurements.

⁸The length, and therefore λ , is derived from design file; the possibility of an additional variation has to be considered due to the uncertainty of the lithography process as described in App. A.

⁹The lack of components is a major disadvantage of mini-SMP connectors.

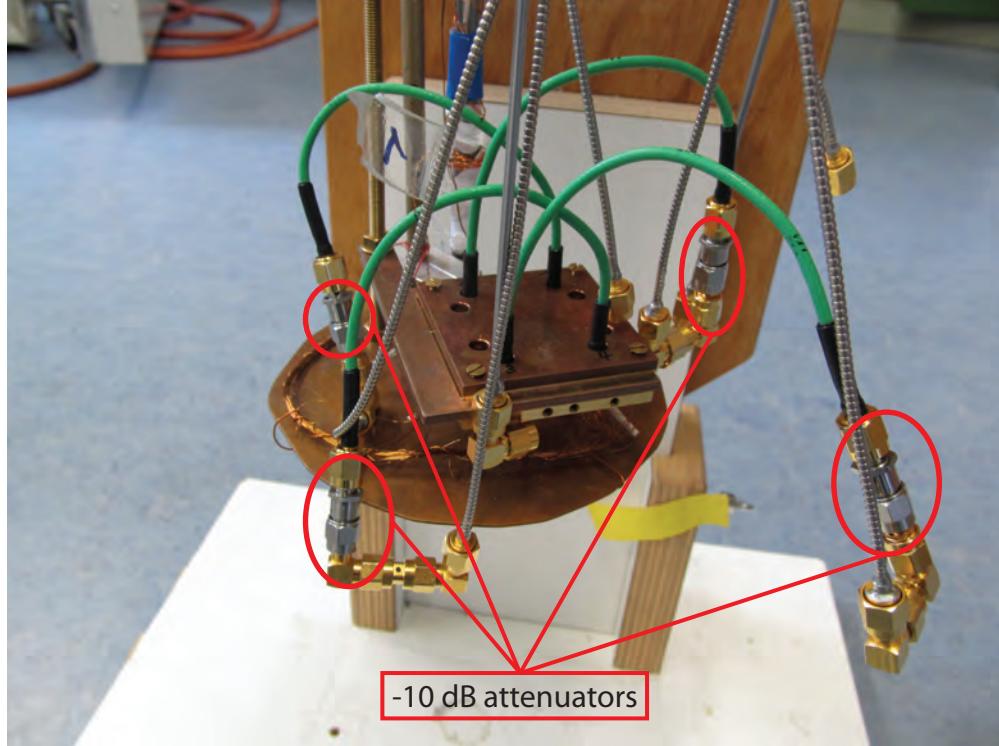


Figure 4.35: Picture of the sample package in sample holder assembled in the cryostat insertion with four *GPPO* adaptors, each combined with a -10 dB attenuator.

As already mentioned, the low-loss copper-clad cables of the cryostat are utilized. Because they do not damp reflections well (see App. C), extra attenuators (*IN-MET 18AH-10dB*) are added to each adaptor. Nevertheless, the calibration data still contains resonances due to the structure of the calibration chip itself [see Fig. 4.36 a)]. These features are relatively narrow and differ between calibration chip and sample chip. Hence, a simple subtraction of the calibration data yields artifacts in these regions. Fortunately, the relevant features of the quadrature hybrid are in a region where these artifacts are unimportant, so we use the calibration anyways.

In Fig. 4.36 b) and Fig. 4.37 we can see that our device exhibits the expected behavior in the frequency window between 4.9 GHz and 5.8 GHz. In this region, the signals of the “direct” and the “coupled” port are close to -3 dB while the isolation is better than 9 dB. At suitable operation points, the latter can even exceed 15 dB. This is particularly true for the region around the designed frequency of 5.7 GHz. We attribute the remaining ripples to calibration issues, the fact that the attenuators are not directly attached to the mini-SMP connectors (see Fig. 4.35), remaining reflection points in the sample package, and our simple chip design (e.g., we have no microstructured metallic air bridges at the T-junctions). We expect that improving some or all of these points will further increase the quality of our beam splitter transmission data. We did not investigate the phase relation due to the un-

kown electric length of the cryostat cables. Nevertheless, our measurements clearly show the current design of our quadrature hybrid is, in principle, already suitable for the construction of an interferometer consisting of two quadrature hybrids in series. When additionally including a suitable Josephson-junction-based circuit, such an interferometer can form the core of an all-optical quantum controlled-phase gate in the microwave regime.

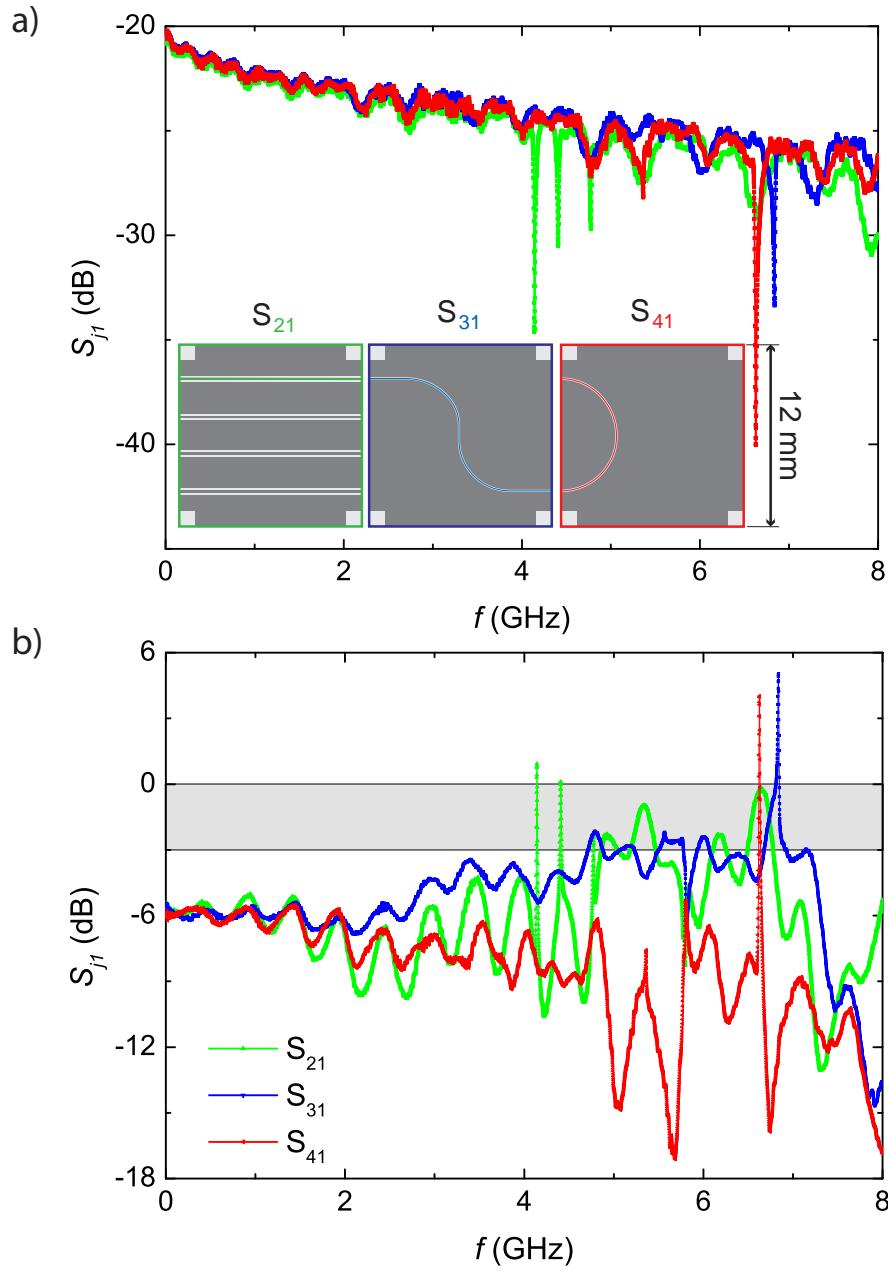


Figure 4.36: a) Calibration measurements of the scattering parameters S_{j1} for the sample package with the mini-SMP connector PCB; chip designs shown in insets. b) Calibrated transmission through the quadrature hybrid (Fig. 4.34). Shaded area to distinguish losses between 0 dB and 3 dB.

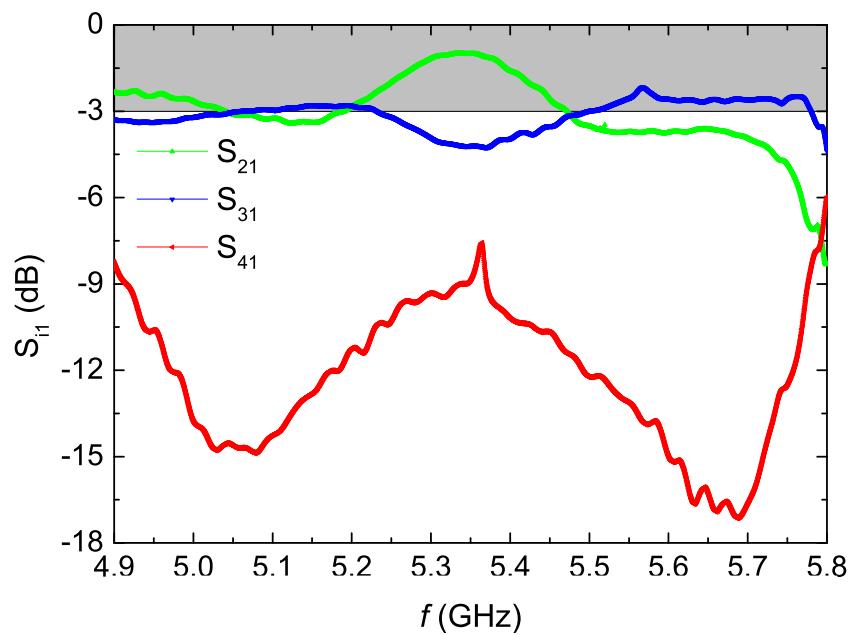


Figure 4.37: Zoom into the relevant frequency range of Fig. 4.36 b).

Chapter 5

Summary & Outlook

In this chapter, an overview of the progress achieved with the measurement setup during this thesis is given. Furthermore, an outlook of future improvement possibilities and applications is included as well.

During the analysis of the original setup with press-contact connectors (*SMA*) conducted in Sec. 4.1.1, several critical aspects of the sample package could be disclosed by examining the behaviour frequency domain measurements. This lead to the examination of critical connections with the goal to reduce reflection losses. Experimenting with different techniques at the transition between PCB and measurement setup (Sec. 4.1.2) resulted in a whole new design approach based on the employment of soldered surface-mount mini-SMP connectors. This step constitutes one of the main achievements of this thesis, since not only reflection losses could be reduced by at least 10 %, but the new connector type also solves the major problem of a reliable connection method and helps retaining a reproducible performance.

In addition, validating the parameters of the substrate *Rogers 3010*, especially the dielectric constant, enabled the compensation of design errors of the PCB and allowed for a matched characteristic impedance of 50Ω with setup (cables) and chip. Furthermore, the design of the waveguides on the PCB was optimized. Therefore, a number of features in transmission measurements can be suppressed. In this part of the thesis, there was also derived the direct dependency of connection quality between the waveguides of PCB and chip (through bond quantity).

One problem encountered in Sec. 4.1.3 concerns the substrate of the PCB. Its dielectric constant determines the characteristic impedance with direct consequences for the design parameters and the accuracy of the employed calculation method. Via TDR analysis, we find that the dielectric constant of the substrate at low temperatures is close to the value extrapolated from the high-temperature dependence.

Finally, we embed a superconducting quadrature hybrid ring into our optimized sample package. Transmission measurements clearly reveal the expected behavior near the designed working frequency. This is a substantial improvement over the work done in Ref. [37], where the same design was measured in the unoptimized sample package. A further increase of the performance could be given through the

application of additional bonds across the gaps at conductor bends (T-junctions) [9, 11]. Eventually, bonds added onto the chip could increase the potential balancing in a way similar to vias and therefore improve the performance as well, since ground planes do effect the overall performance as proven in Sec. 4.1.5.

Based on the results presented in this thesis, the next steps towards a functional interferometer can be taken. Ref [8] suggests a combination of two beam splitters with a nonlinearity in between. This setup can then be utilized as a logic gate in an all optical quantum computation device in the microwave regime.

Appendix A

Chip fabrication

The sample chip is a very flexible component since the characteristic impedance of a CPW Z_0 is dependent on geometry relations. Here, the fabrication process is presented. Figure A.1 gives an overview over the production steps. To avoid contamination, most steps (except for sputtering) take place in the cleanroom.

At the start of the production is the Si wafer ($250\text{ }\mu\text{m}$ of intrinsic silicon coated with 50 nm of thermal oxide) that constitutes the dielectric of the later coplanar waveguide (pre-cut to $12 \times 12\text{ mm}^2$). Before further production steps can be taken, a protective coat applied for transportation of the cutted dies has to be removed as described in Tab. A.1.¹ It is recommended to repeat this process before any production steps are taken to avoid any dirt such as dust on the surface. Careful work is important to avoid scratches on the sensitive surface.

In the next step, a Nb layer of 100 nm thickness is sputtered onto the Si wafer. Figure A.2 shows the custom build sputtering device at the WMI, and the process parameters can be found in Tab. A.2. To avoid contamination, the setup is evacuated to 10^{-9} mbar with separate sections (divided by doors) and a ‘Load Lock’ with, when opened, continuously flowing N_2 gas. Transfers between the sections is possible via a robotic arm.

During the sputtering process, atoms are ejected from the Nb target by ions generated from a magnetron (momentum exchange through collisions; sets off a cascade) if their energy is larger than surface binding energy². In the case of close proximity between chip and target, thermal tensions may occur. This can cause that the metal layer comes off (ultrasonic bath!).

The partial removal of Nb (“gaps”) is achieved through optical lithography and reactive ion etching (RIE). Figure A.3 shows the utilized equipment. At first, a small amount of photoresist *AZ 5214E* [43] (approximately $15\text{ }\mu\text{L}$) is applied to the chip by spin-coating (see Tab. A.3), resulting in a film with a thickness of $1.4\text{ }\mu\text{m}$ [44].

¹Before each bath, the chip is washed with the corresponding solvent of the following step. The reason behind Isopropanol is that it boils away more easily than Aceton, leaving less residues and is therefore better suited for a clean surface.

²The sputtering rate is dependent on beam angle, distance between target and sample as well as ions mass and energy.

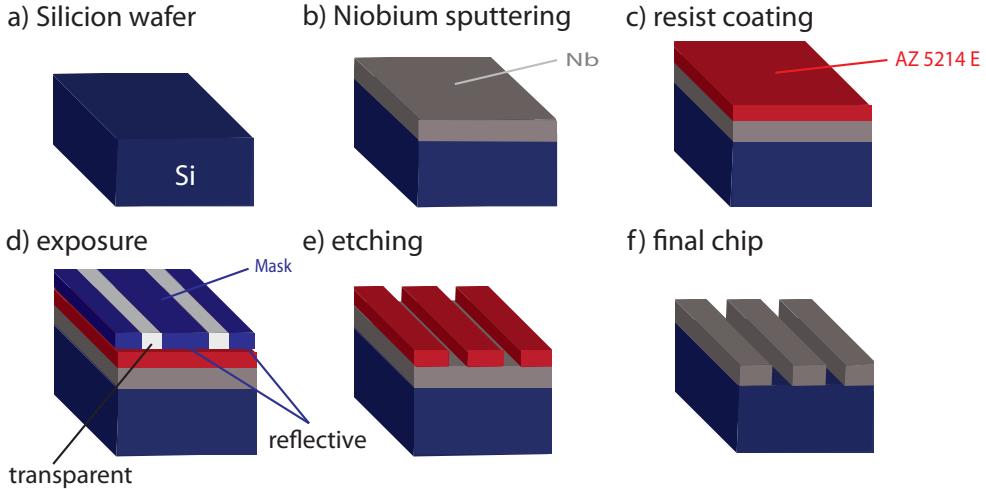


Figure A.1: Production schematic that outlines the different manufacturing steps necessary to produce a structured coplanar waveguide. Fabrication overview: raw Si wafer **a)**, with thin sputtered metal layer on top facing **b)** and applied resist ontop the metal **c)**; with mask **d)**, after etching **e)** and final CPW **f)**. **c)** through **e)** illustrate the process steps of optical lithography.

Table A.1: Cleaning proces

step 1	<i>hotplate; in Aceton technical grade</i>
<i>time</i>	1 h
<i>temperature</i>	70 °C
step 2	<i>ultrasonic baths</i>
<i>time</i>	3 min
<i>setting</i>	<i>level 1; to avoid damage to the chip</i>
<i>solvent 1st bath</i>	<i>Aceton technical grade</i>
<i>solvent 2nd bath</i>	<i>Aceton por analysis</i>
<i>solvent 3rd bath</i>	<i>Isopropanol por analysis</i>
step 3	<i>repeat steps 1 and 2</i>
step 4	<i>dry with gaseous nitrogen (N₂)</i>

However, this layer is not entirely flat but develops edge beads as illustrated in Fig. A.3. The resist then has to be activated through baking: 110 °C for 90 s. During this time, the molecules of the resist form a stable polymeric pattern according to Ref. [45]. In addition, the remaining solvent concentration is reduced, avoiding bubbles and other unwanted features, see Ref. [46] for more information.

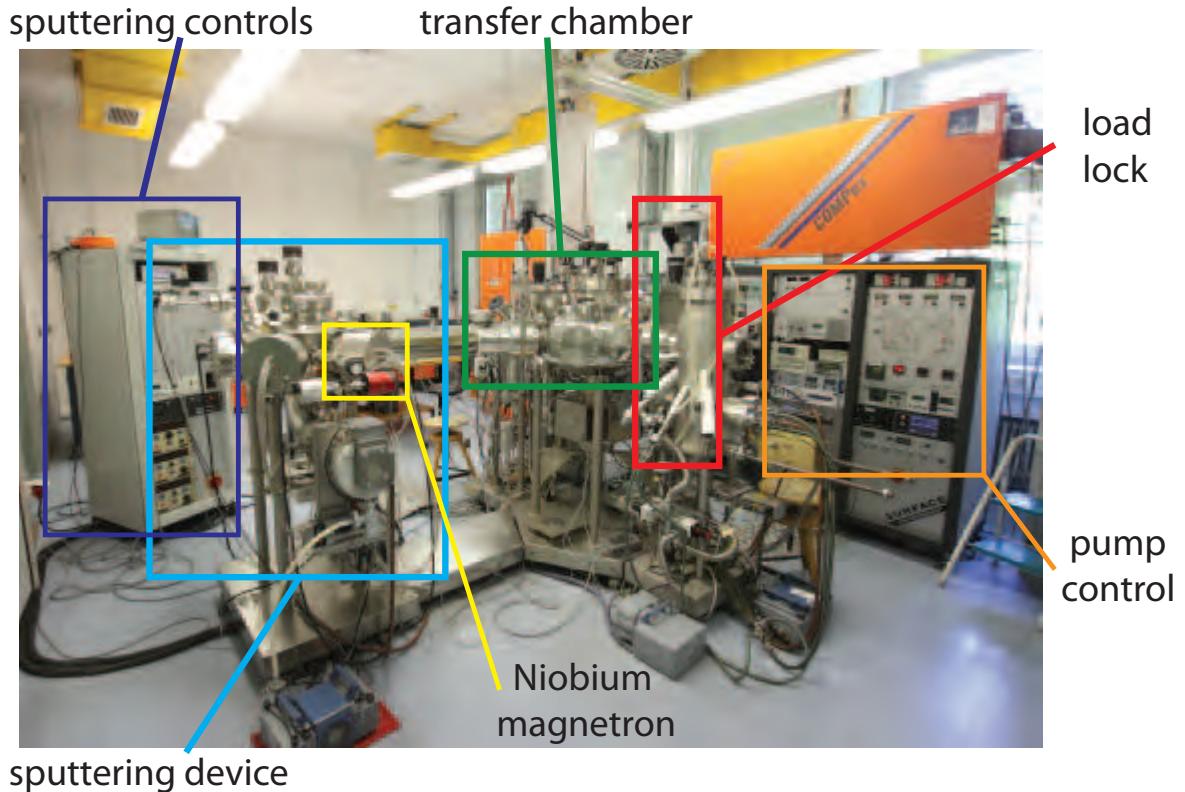


Figure A.2: Picture of sputtering device. With kind permission from Edwar Xie [42]. Please note that the load lock is barely visible behind another device.

Table A.2: Sputtering parameters for a 100 nm thick niobium layer

<i>process pressure</i>	$4 \cdot 10^{-3}$ mbar
<i>magnetron power</i>	200 W
<i>pre – sputtering</i>	300 s
<i>sputtering time</i>	240 s
<i>Argon (process gas) flow</i>	20
<i>distance</i>	<i>maximum</i>
<i>direction</i>	<i>in front of magnetron (auto)</i>

Table A.3: Spin coater settings

step 1	
<i>period</i>	5 s
<i>acceleration</i>	500 rpm in 0.2 s
step 2	
<i>period</i>	55 s
<i>acceleration</i>	8000 rpm in 6 s

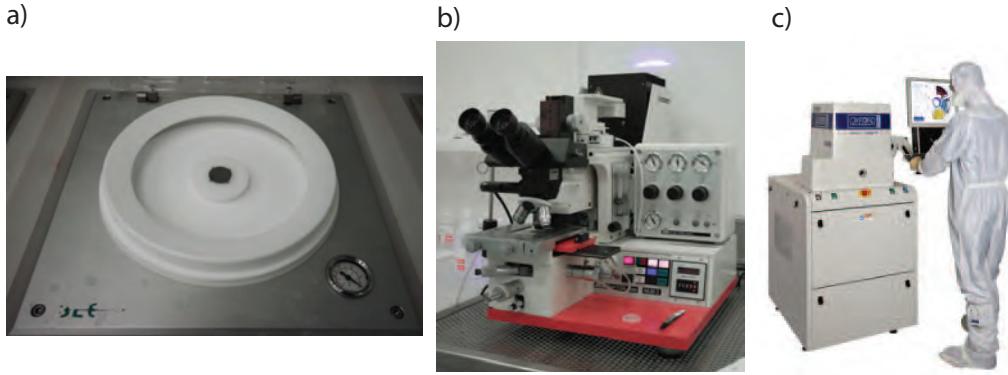


Figure A.3: Spin coater Delta 20 BM from BLE a), mask aligner MJB-3 from Süss b) and Plasmalab 80 Plus reactive ion etcher from Oxford Instruments c).

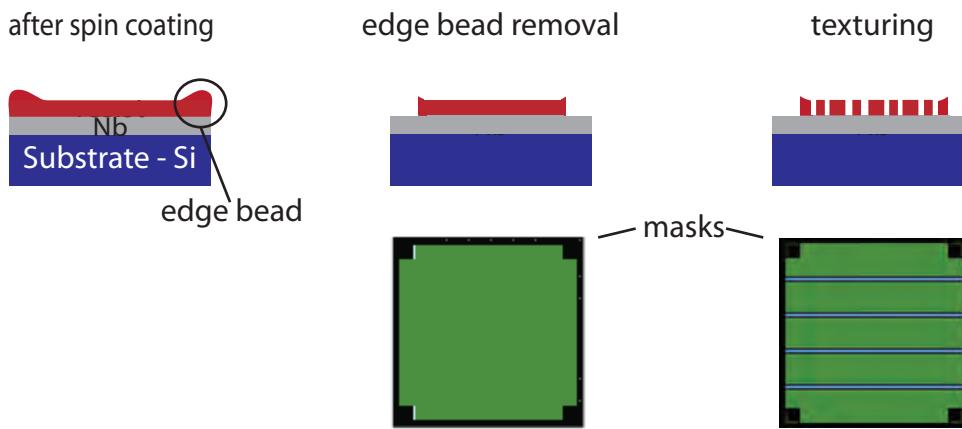


Figure A.4: Schematic overview of all the necessary removal processes with corresponding *masks* that are textured with reflective and permeable areas that let the light pass. During the final production steps, niobium is removed from exposed areas where the resist has been activated.

The resist also contains photoactive compounds, making it sensitive to light. Exposure with ultraviolet light of 400 nm [47] at an intensity of at least 36 mJ/cm^2 breaks the polymer chains of the resist. Since the output of the discharge lamp is subject to variation, the corresponding time span has to be determined with a photodetector. Where overexposure is not problematic (corners and edges), simply the maximum of 99 s is used. The reason for these separate exposures are edge beads (see Fig. A.4 and App. B). The broken parts are then removed with the developer *AZ 726 MIF*, see Tab. A.4. When this additional resist is removed from the edges (after developing), the mask with the actual design for the chip can be employed.³ It should be noted that in order to avoid undercuts due to overdeveloping, the actual structure is developed less.

³This means, that the production for all chip designs is identical with the exception of the utilized mask.

Table A.4: Development

edges and corners (99 s exposure each)	
<i>time shaken in developer</i>	150 s
<i>time shaken in deionized water</i>	30 s
<i>idle period in deionized water</i>	<i>variable; at least 100 s</i>
structure (variable exposure time (36 mJ/cm²))	
<i>time shaken in developer</i>	90 s
<i>time shaken in deionized water</i>	30 s
<i>idle period in deionized water</i>	<i>variable; at least 100 s</i>

Edge beads are not acceptable at this point because of absorption and reflection inside the substrate and possible aggravation of resolution.

For a gap with width b , the angle dependent intensity is given by Ref. [48]:

$$I(\beta) = I_0 \left[\frac{\sin\left(\frac{\pi\beta b}{\lambda}\right)}{\frac{\pi\beta b}{\lambda}} \right]$$

For an estimated tolerance Δx of 1 μm and a gap h between mask and the central surface level of the chip that is according to App. B⁴ approximately 200 μm , $\beta = \sin(\theta) = \sin(\arctan(\Delta x/h)) = 0.013$. The width b is dependent on the utilized mask. For this analysis, the hybrid ring is used with $b = 20 \mu\text{m}$. For the wavelength $\lambda = 400 \text{ nm}$, the calculated value of the intensity at this angle is less than 0.5, so insufficient for the resist to be activated. The corresponding value for $\Delta x = 2 \mu\text{m}$ is 0.6 and again smaller for $\Delta x = 5 \mu\text{m}$.

The second possibility depicts a more direct approach: too much power is absorbed or reflected if the resist layer is too thick. This leaves a thin film after developing. When experimenting with narrower strips for the mask it is observed that the Nb has not been fully removed. A photography of such an event can be found in App. B. In the final step, the metal layer is removed with RIE [49]. The remaining resist acts as a protective coat for the Nb and only areas where the resist has been removed are etched away. For this step, SF₆ serves as a process gas. During etching, a strong electromagnetic field (radio frequency) is applied, ionizing the gas and creating a plasma. The negative ions then drift towards the positive wafer platter, colliding with the sample chip ontop where chemical reactions result in the removal of the metal. After that, the resist is removed. On the one hand, this includes a cleanup process as for the initial wafer, and a second treatment with the RIE called *ashing* with O₂ as a process gas. The chip is now finished.

⁴The measured values appear unrealistically large, almost the height of the chip itself. A possible explanation could be poor resolution for thick objects since the measurement device, the *DEKTAK*, is usually utilized to measure in the *nm* regime.

Appendix B

Resist layer thickness

Here, a side effect of spin coating square samples is examined: the edge bead. During the process, excessive resist is removed through centripetal force. However, this results in an accumulation of resist at corners and, even more so, edges. These areas have to be removed prior to the actual texturing. The consequence of inadequate masks is presented in Fig. B.1, where a width of $0.3\text{ }\mu\text{m}$ proved to be insufficient. A thin niobium strip remains between center conductor and ground plane, shortening the circuit that is removed in a second exposure.

To determine the additional resist height after spin coating, a *Dektak* is used. With it, variations in the surface structure of a sample can be examined. A stylus with a tip radius of $12.5\text{ }\mu\text{m}$ is pressed against the surface with a force of 1 mg mm^{-2} . In order to measure the relative height, the stylus is moved across the sample and the deflection is measured. Figure B.2 shows the utilized device at the *Zentrum für Nanotechnologie und Nanomaterialien (ZNN)*.

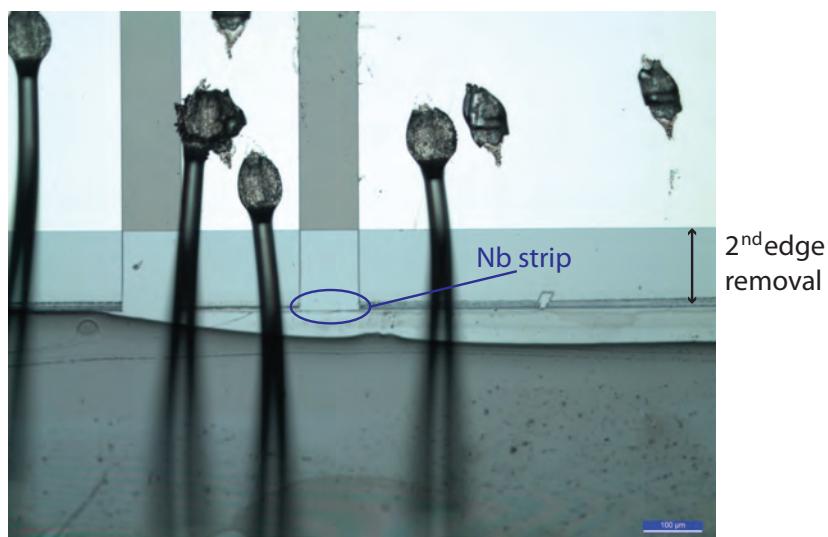


Figure B.1: Photograph of a chip where the edge bead removal had to be repeated on an already textured chip. The discontinuous dark grey area at the bottom is resist that flew over while adhering chip and PCB.

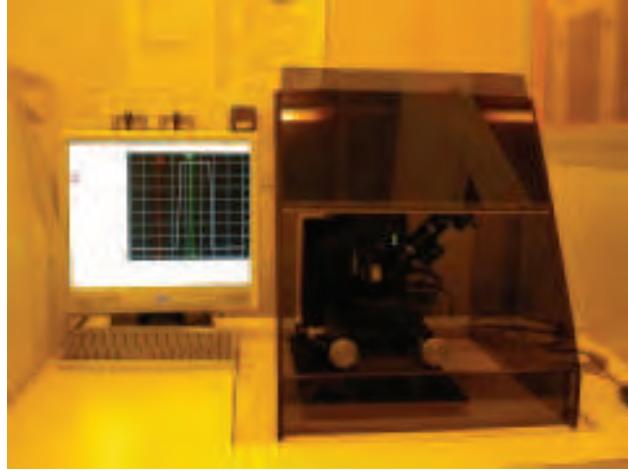


Figure B.2: Picture of *Dektak* at the ZNN.

In the following, the effect of different accelerations during spin coating are analyzed. The goal is to reduce the resist edge bead width and height in order to minimize the necessary lift-off of niobium. If successful, a simple option is available to modify the frequency of resonators on calibration chips (see Fig. 4.3). Therefore, the initial step of the standard spin coater program is varied, compared to higher settings and the difference δz then measured with the *Dektak*. The data for edges and corners is presented in Fig. B.3.

Although the fitting is not perfect (central area should be flat), it is clear that the desired effect does not occur. For an increased initial acceleration period, the peak is assumed to shrink. However, the diagonal measurement from center to corner unexpectedly shows the highest peak for the longest acceleration period of 400 ms and a total speed of 1000 rpm. In the analysis of a horizontal line towards the edge gives the medium setting as the largest result. Therefore, it can be summarized that the plan of reduction failed since the expectations were not fulfilled. Other factors seem to be more important in comparison. As expected, the additional resist height at the edges lies fully within the exposed area of 0.5 mm (width), the extension of the currently used mask¹. It should be noted that since the resist thickness is the highest at the corners, the smallest peak is expected to be at the measured center of the edge.

For the diagonal measurement, the removed niobium is not sufficient in comparison with the extensiveness of the corner edge bead. Since no texturing takes place at this particular spot, this can be disregarded as the resist can be pressed flat so that the mask has no additional distance to the surface.

The reduction of edge bead extension with varied acceleration settings failed, and with the effects seen in Fig. B.1, no change of the mask design is possible.

¹This magnitude seems unrealistic. A resist thickness of up to four times the chip height is probably a calibration error. However, substitution of μm in favour of nm does not affect the conclusion of this measurement series (only the effect on exposure intensity is less drastic).

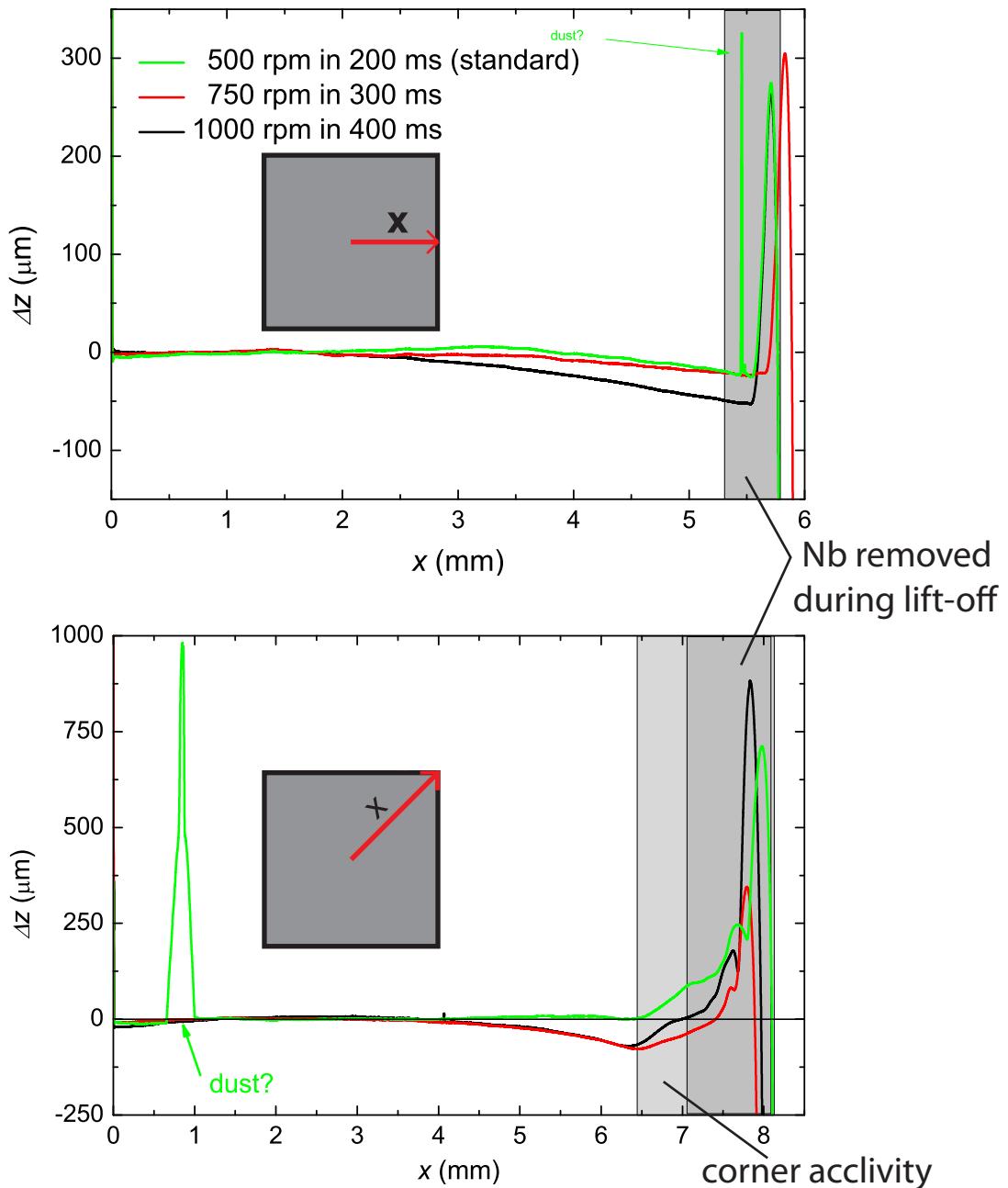


Figure B.3: Relative edge bead height at corners and edges measured with *Dektak*.

Appendix C

Internal cryostat cables

In the cryostat, two different sets of coaxial semi-rigid cables are contained: copper-clad stainless steel (six) and stainless steel (two, numbered 5 and 6). The mini-bend copper-clad stainless steel cables, *Astro-Cobra-Flex 31086S* [35], have an outer conductor that is composed of 2 layers (each 0.0762 mm thick; inner oxygen-free high thermal conductivity (OFHC) copper and type *304L* stainless steel as the outer layer) and a center conductor of copper clad steel [50] with a velocity of $0.7 c$ and an optionally extended temperature range of up to -269°C . For the other cable type, stainless steel constitutes the inner and outer layer. Further information is not available.

Since all cables end in a male jack, sets of corresponding cables are linked for this analysis via a female/female SMA adapter for calibration measurements. For this comparison, the setup is cooled and the transmission measured. Before another cool down, the connection between the cables is disengaged and then reconnected to simulate the exchange of the sample package. An overview of the deviating performance properties is presented in Fig. C.1. An overall change in the transmission can be observed of up to 0.4 dB which has to be taken into account with regards to consistency. The first thing that appears when comparing both cable types is that it is obvious that the steel cables have a higher attenuation of -10 dB to -20 dB across the whole frequency range of 10 GHz. These additional losses result in the effect that reflected signals provoke since these waves are further attenuated. As a result, oscillations that overlay the original data experience a partial reduction as can be seen in the direct comparison between 5 and 6 GHz within a 4 dB spectrum. Another effect that can be observed is that there is a slight deviance of 0.2 dB between consecutive measurements, a general problem of the utilized setup that reduces reproducibility of measurements.

Additionaly, an actual sample is assembled inside the cryostat, cooled to 4 K and connected with the different sets of the aforementioned cable types and the transmission between the corresponding ports i and j is measured. Utilized is a press-contact PCB that also includes a calibration chip of the design shown in Fig. 4.2 b), linked with the PCB through bonds. The data is presented in Fig. C.2. A shift towards

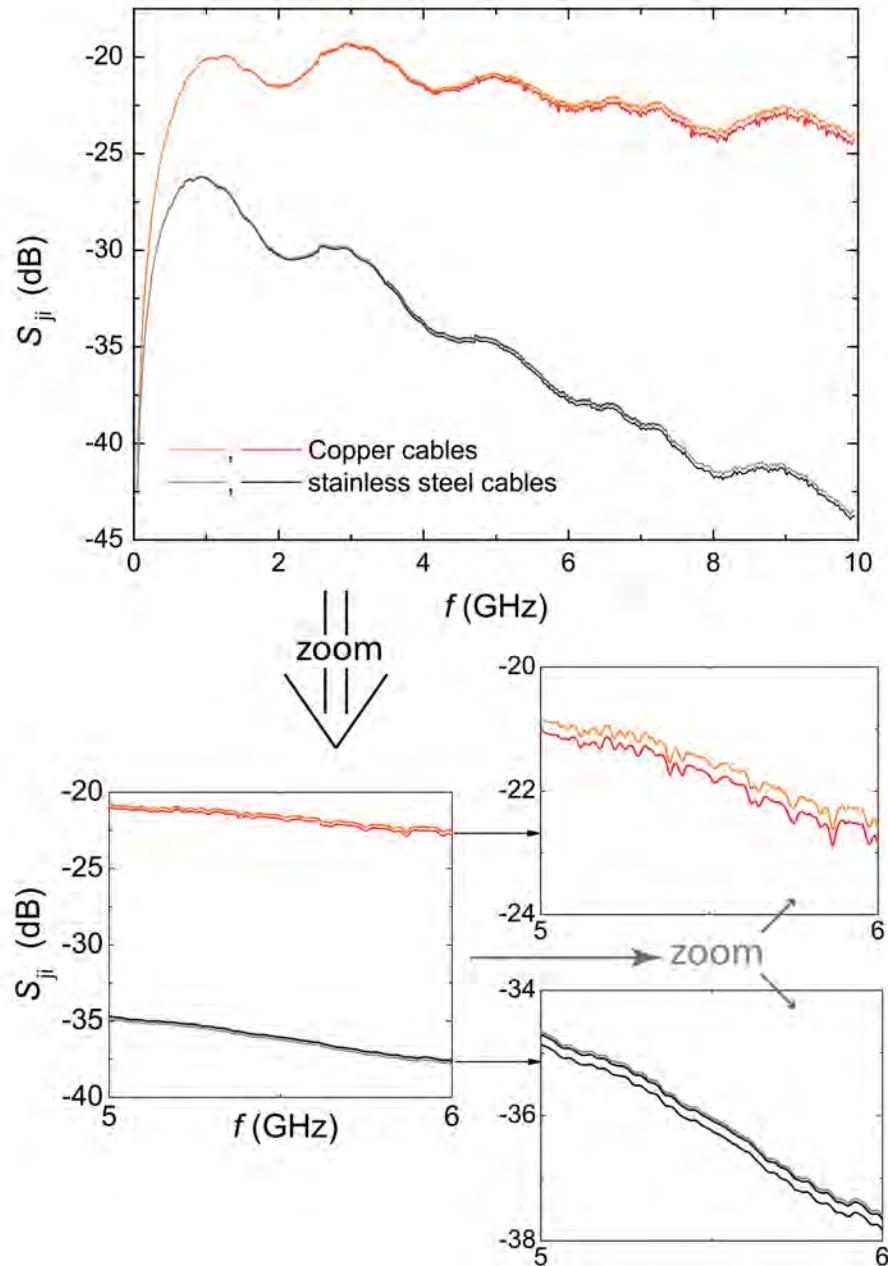


Figure C.1: Transmission performance of copper and steel cables; measured data without calibration.

lower frequencies can be observed for the copper-clad stainless steel cables and also ripples due to the reduced damping of reflections. Furthermore, measured dips have increased in magnitude. This comparison illustrates directly the influence of cables on measurement performance.

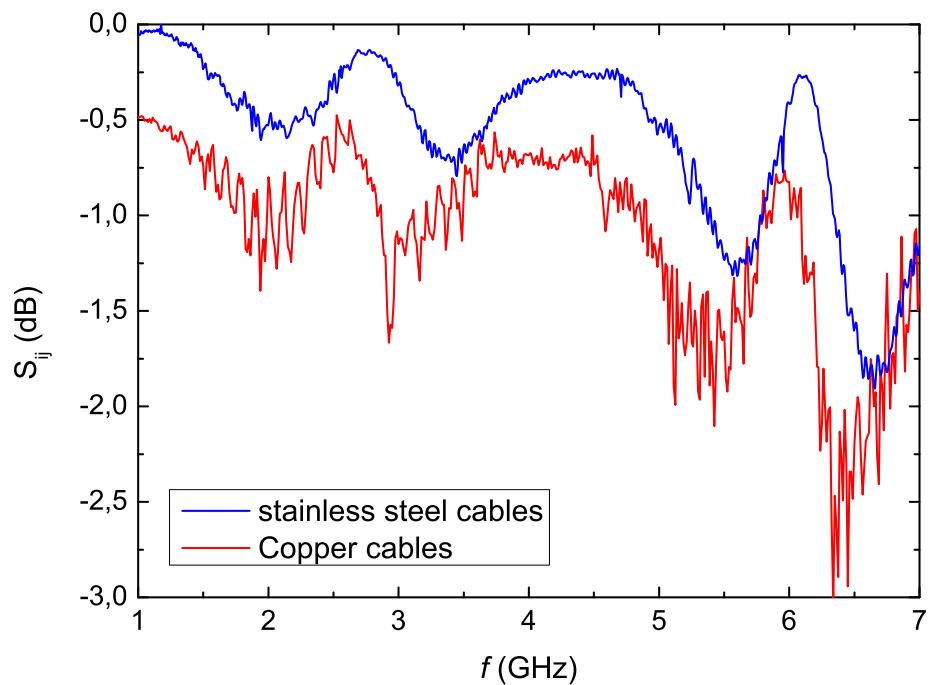


Figure C.2: Calibrated transmission between two ports for Copper and steel cables using a press-contact PCB with calibration chip. See Fig. 4.5 for reference.

Appendix D

Box top metal covers and air modes

Here, the effects of a varying air volumes are analysed with a press-contact PCB assembled in a box. The top cover of the box is utilized to modify the available space with $\epsilon_r = 1$. Therefore, the original cover, an elevated metal plate, is compared to the adapted version for the surface-mount design. A photograph can be found in Fig. D.1. Please note that the necessary holes are not taken into account. An additional metal plate, filling the space between the screw and the cover, is added. Furthermore, the PCB is measured without a box cover.

As indicated during the analysis in Sec. 4.1.3, the effect for all volumes is negligible.

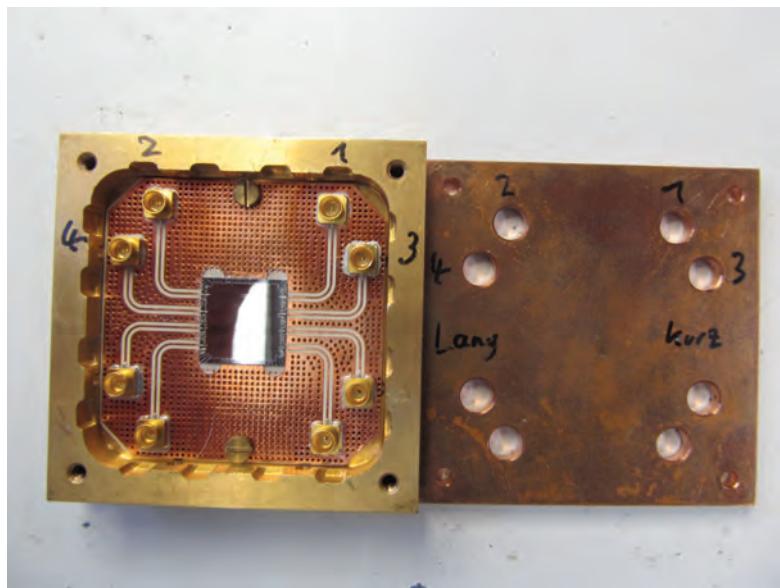
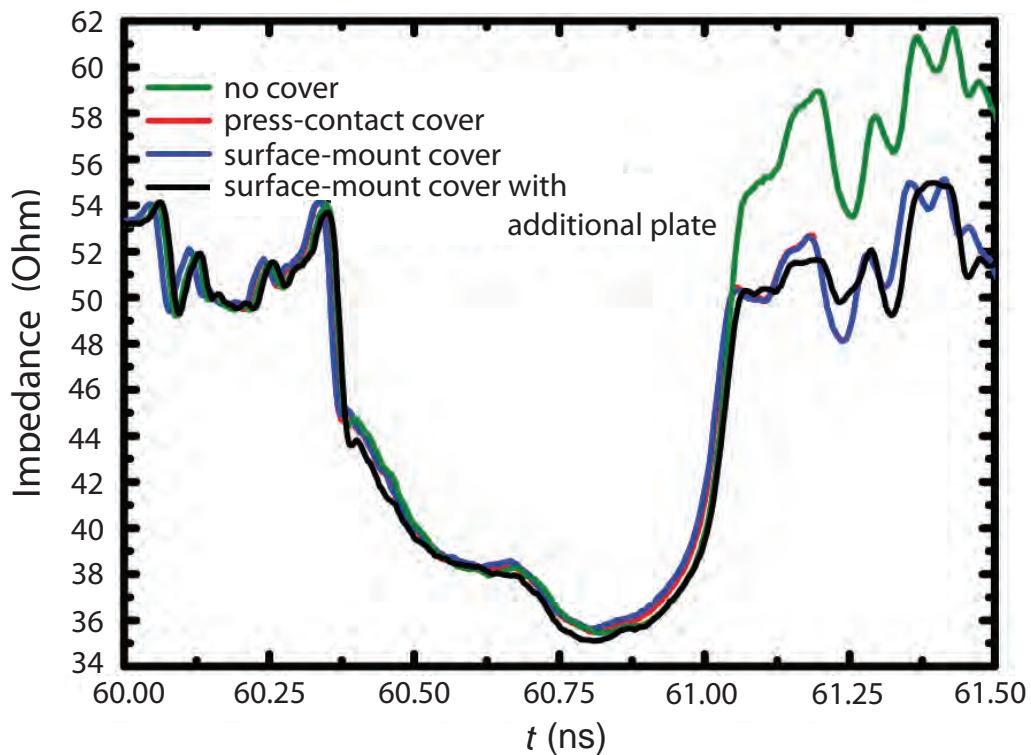


Figure D.1: Picture of top cover for a box that contains a surface-mount PCB with holes for the adapter cables.



covers

press-contact cover



surface-mount covers
(invisible: holes for adapter cables)



additional plate

lower box half



Figure D.2: Effect of air volume variation on TDR performance by modification of top metal covers.

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