

A1=0 A0=0, LSB I2C Slave Address

When LDACis permanently tied low, the LDAC mask bits are ignored.

Asynchronous Reset Input. The RESET input is falling edge sensitive. When RESET is low, all LDAC pulses are ignored. When RESET is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin.

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IPE

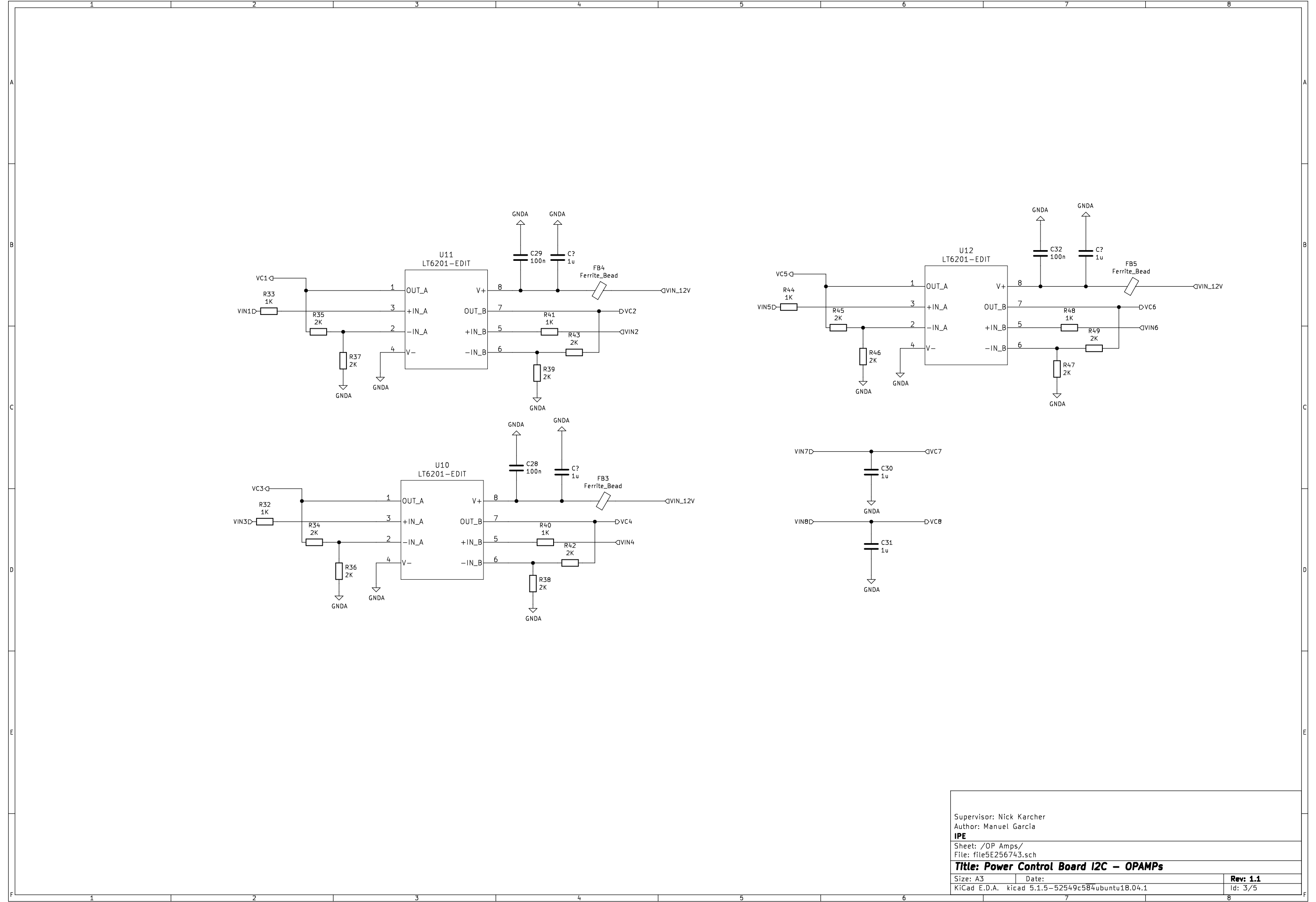
Sheet: /DAC/
File: file5E25670C.sch

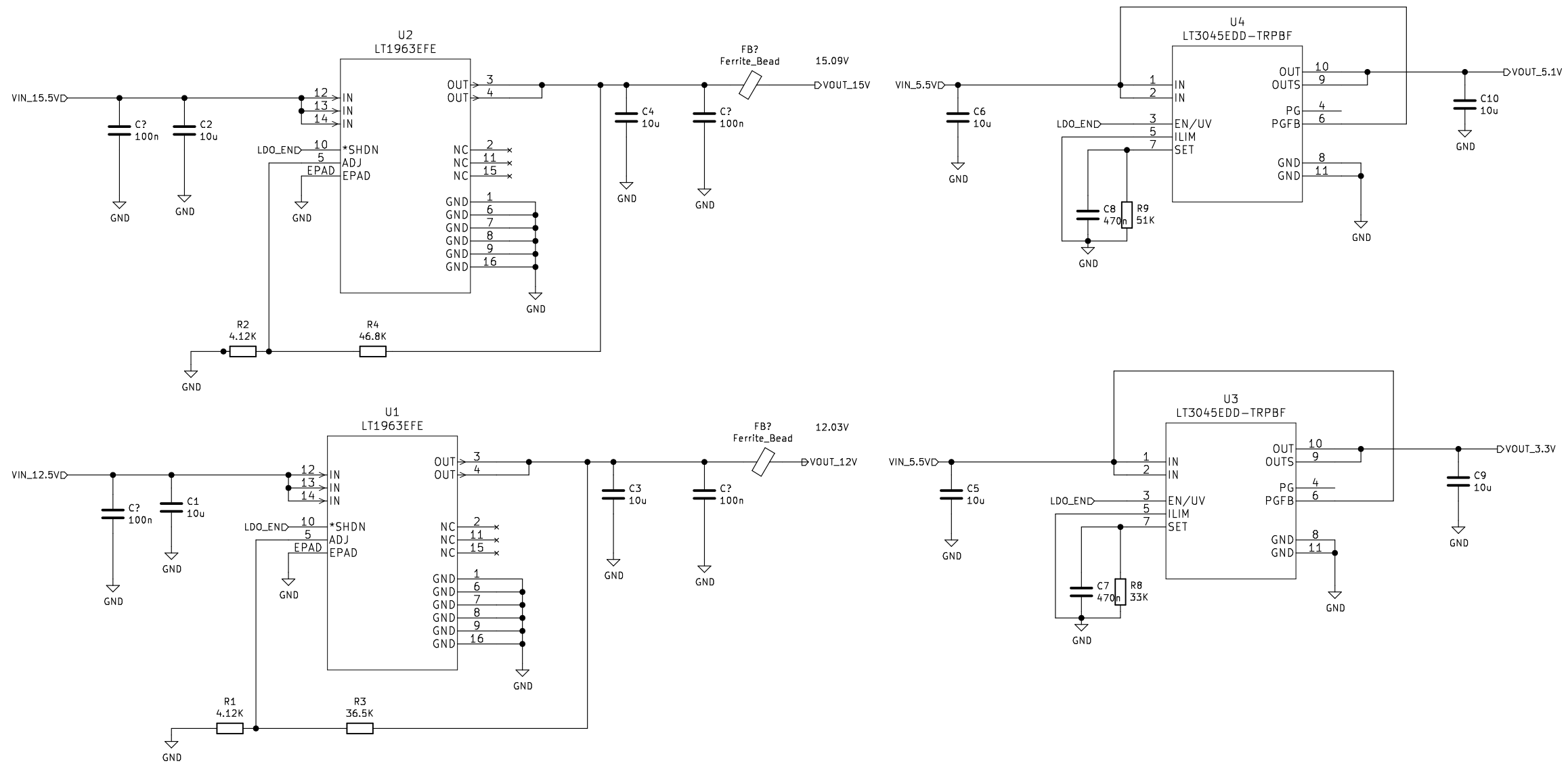
Title: Power Control Board I2C – Octal ADC

Size: A3	Date: 2019-11-24
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Sheet: /LDO Regulators/
File: file5E2566DF.sch

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