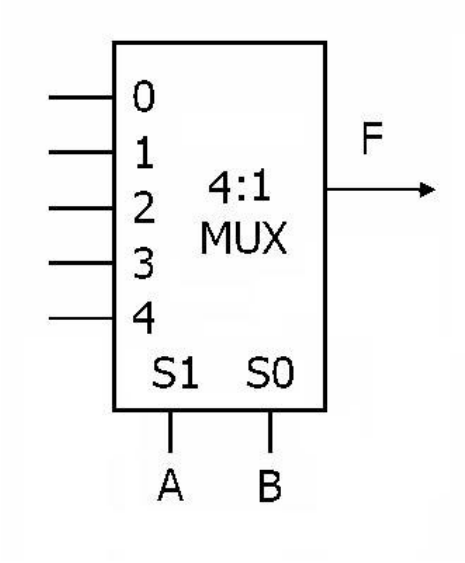
1. **(10 points)**
   Iimplement the function F using the 4:1 multiplexor shown below.
   $F(A,B,C,D) = \Sigma\ m(5, 6, 7, 8, 11, 12, 13) + d(2, 15)$
   Use minimum number of gates to implement the function. Show all the gates you use.



Solution:

This is the correct implementation with minimum number of logic gates.

A	B	Function
0	0	0
0	1	C+D
1	0	C'D'+CD
1	1	C'

2. **(20 points)**

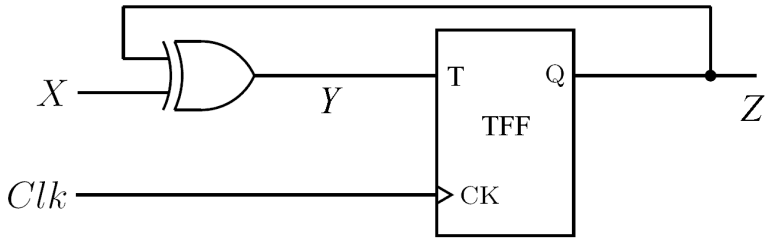
Given the observed output Z below of the circuit given above, determine what the inputs Clk and X must be.

If the value must be a 1, write 1. If the value must be 0, write 0. If the value can either be 0 or 1, write X.

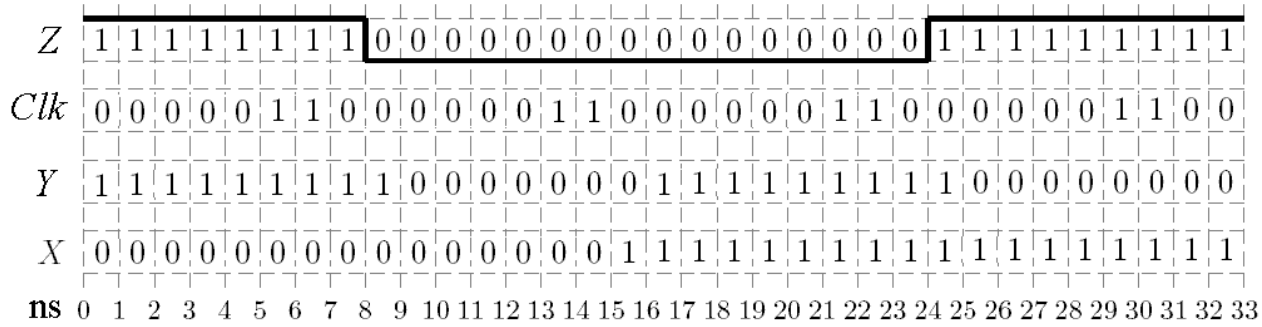
You may make the following assumptions:

- The clock has a period of 8 nanoseconds (ns) and a 25% duty cycle.
- The positive edge-triggered T flip-flop has a setup time T_{su} of 2 ns, a hold time T_h of 1 ns, and a propagation delay T_{pd} of 3 ns.
- The delay of the XOR gate T_{XOR} is 1 ns.

If the value must be a 1, write 1. If the value must be 0, write 0. If the value can either be 0 or



Solution:



(15 points)
A sequential circuit has two inputs w1 and w2, and an output, z. Its function is to compare the input sequences on the two inputs. If w1=w2 during any four consecutive clock cycles, the circuit produces z=1; otherwise, z=0.

For example

W1:0110111000110
W2:1110101000111
Z:0000100001110
Draw the state diagram using at most 5 states.

Solution: