PART II

Tools you need

&

Concrete Design Example

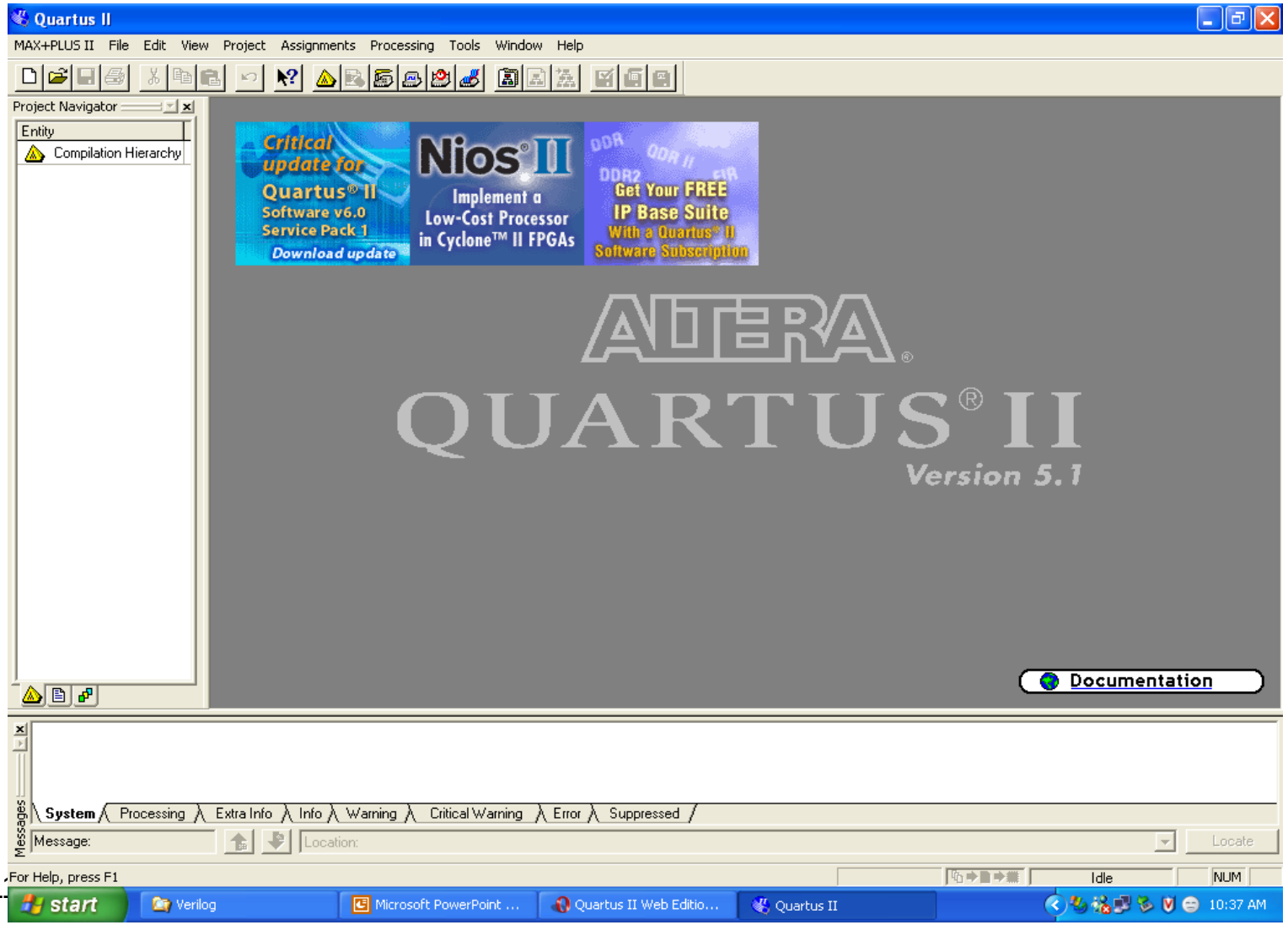
Tools

- You need two things

1. **Editor**
   - Quartus II 5.1sp2 Web Edition Full
2. **Simulators**
   - Quartus II 5.1sp2 Web Edition Full

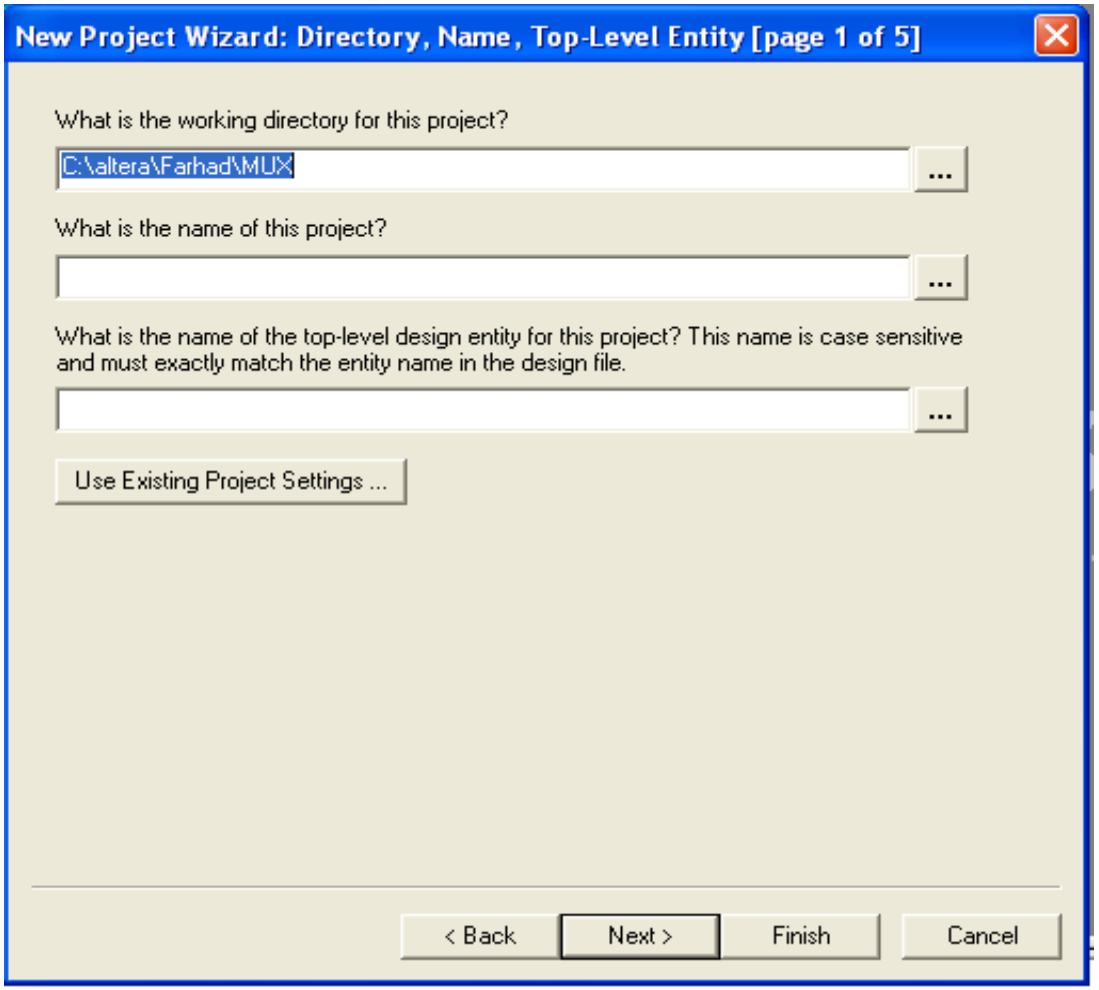
Quartus IDE

Download it from Here:
https://www.altera.com/support/software/download/altera_design/quartus_we/dnl-quartus_we.jsp

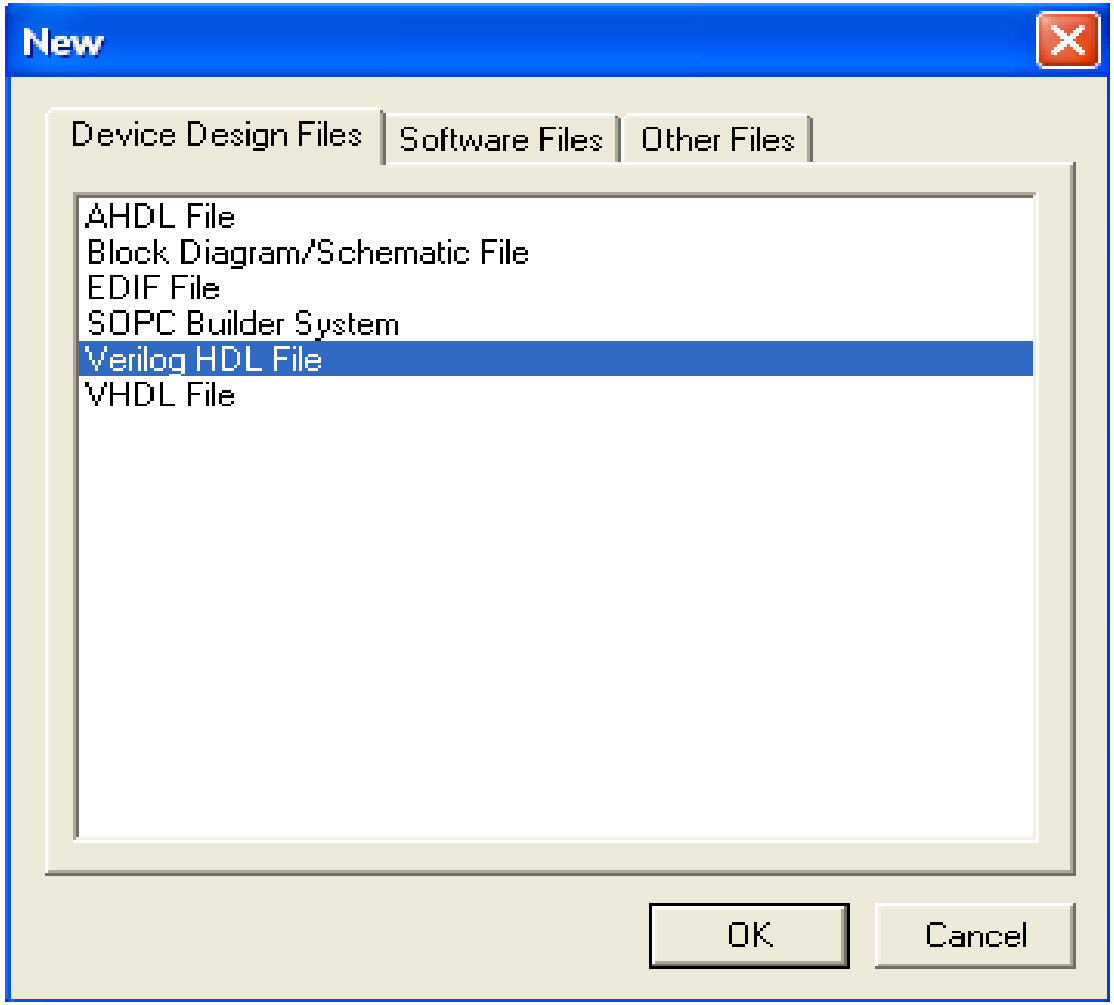


Example of MUX 2/1

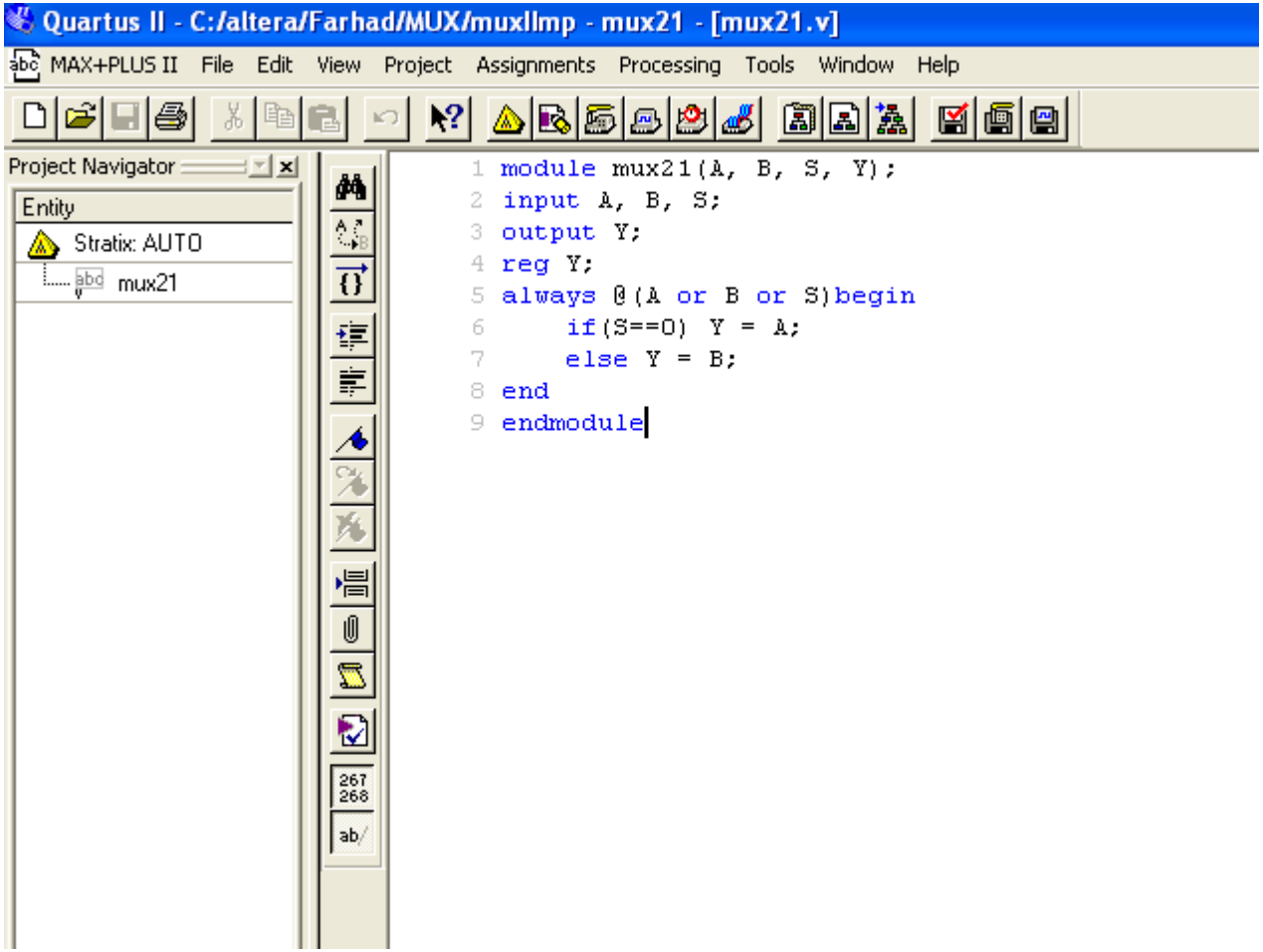
- Create a project



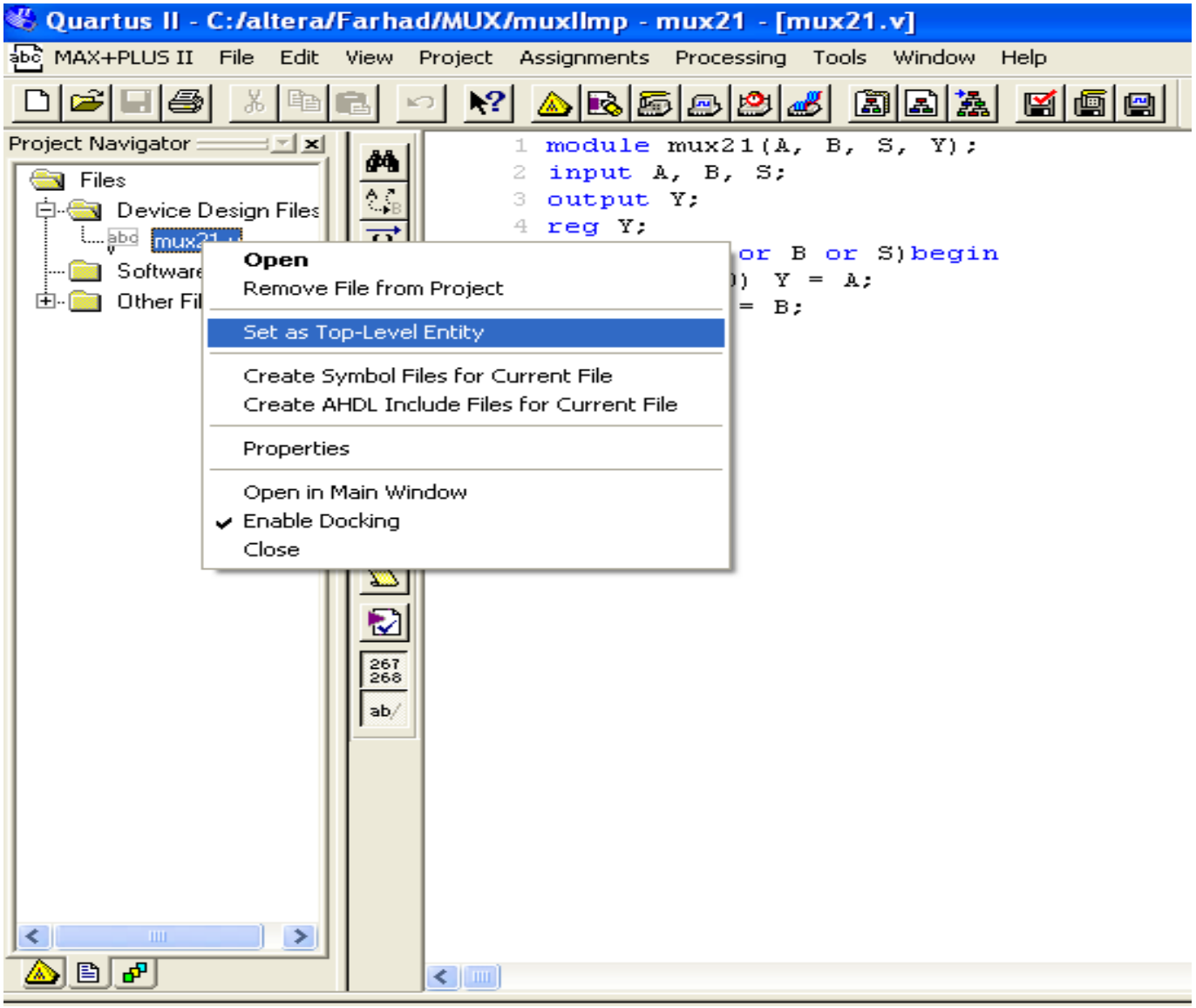
Create or add verilog file to the project



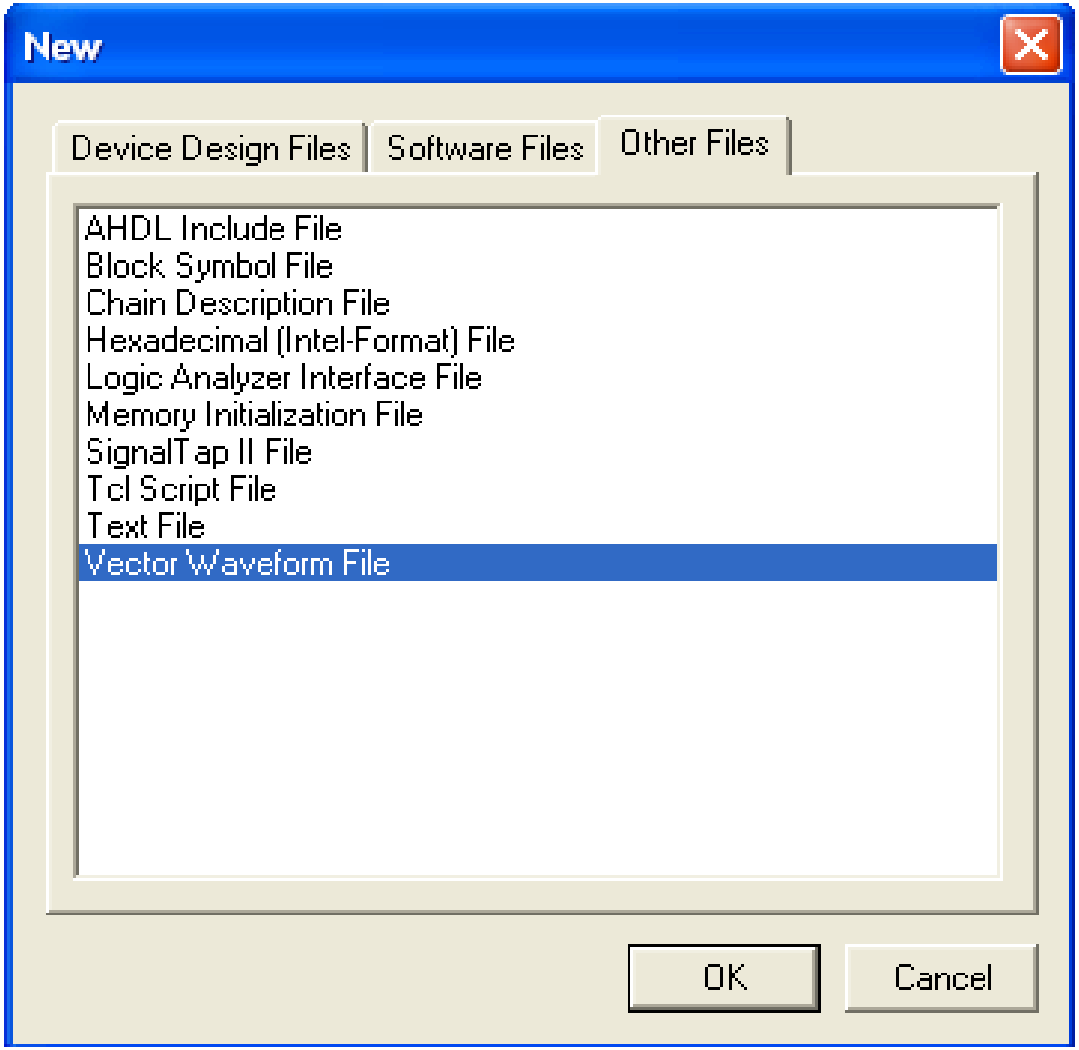
The file is written and saved and add to the project

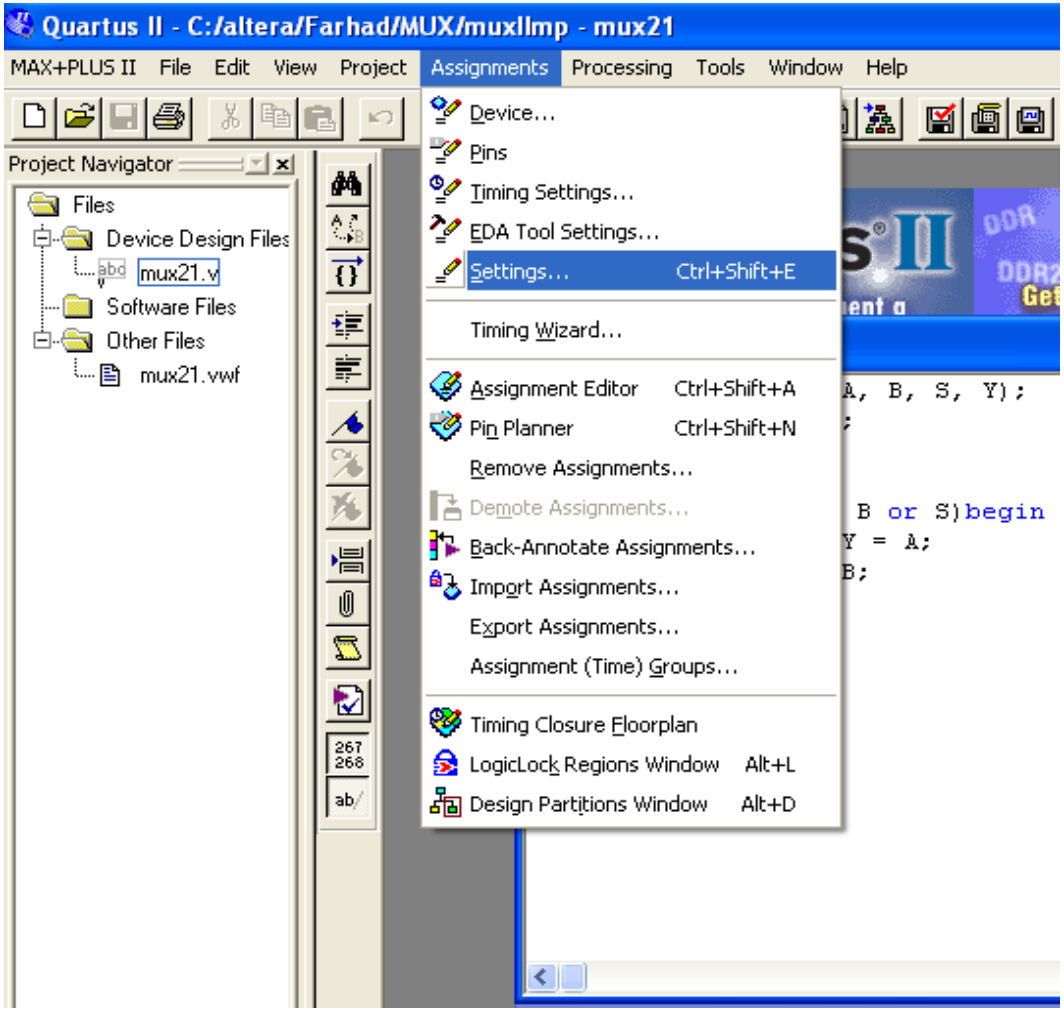


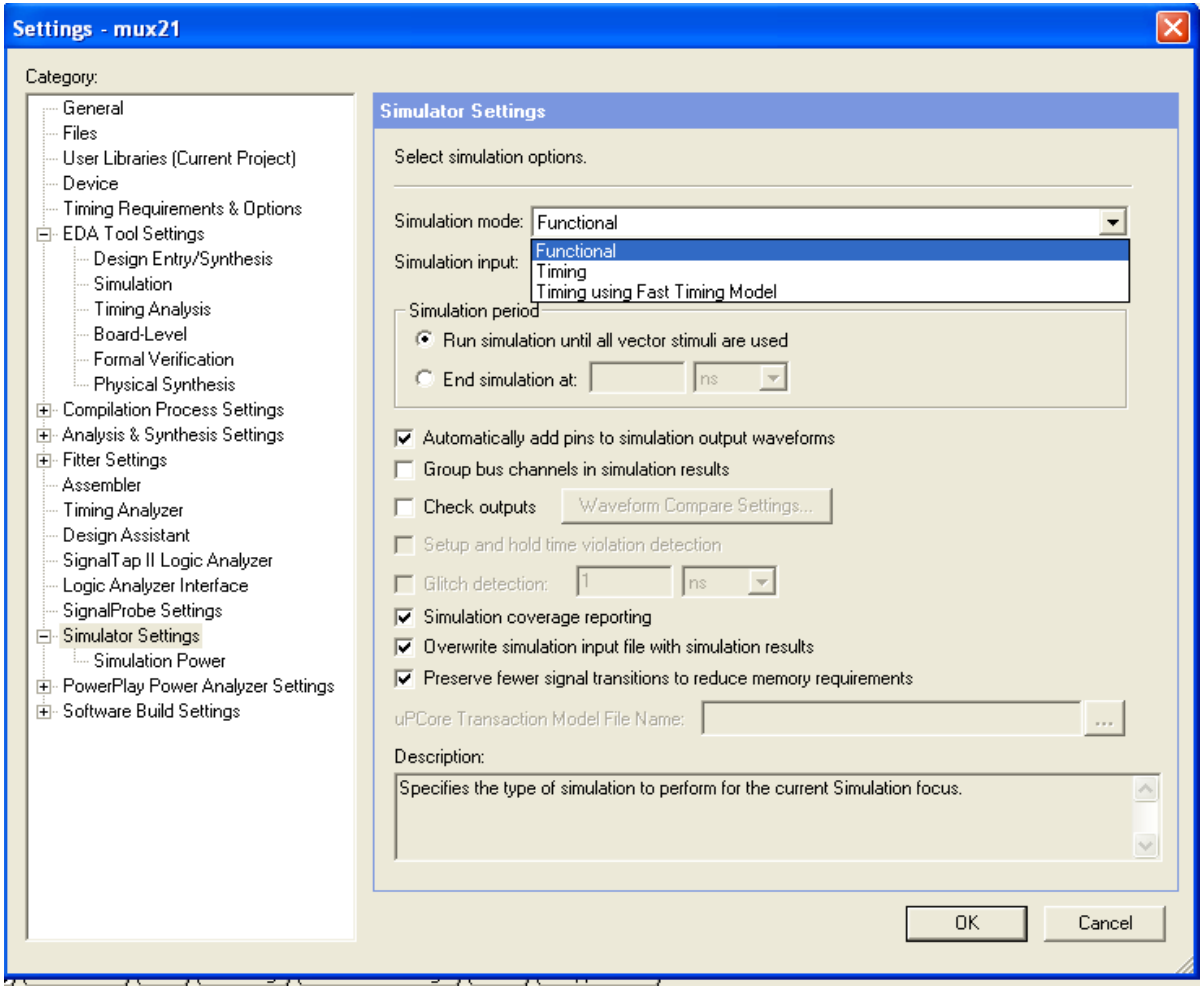
Set the file as top level entity

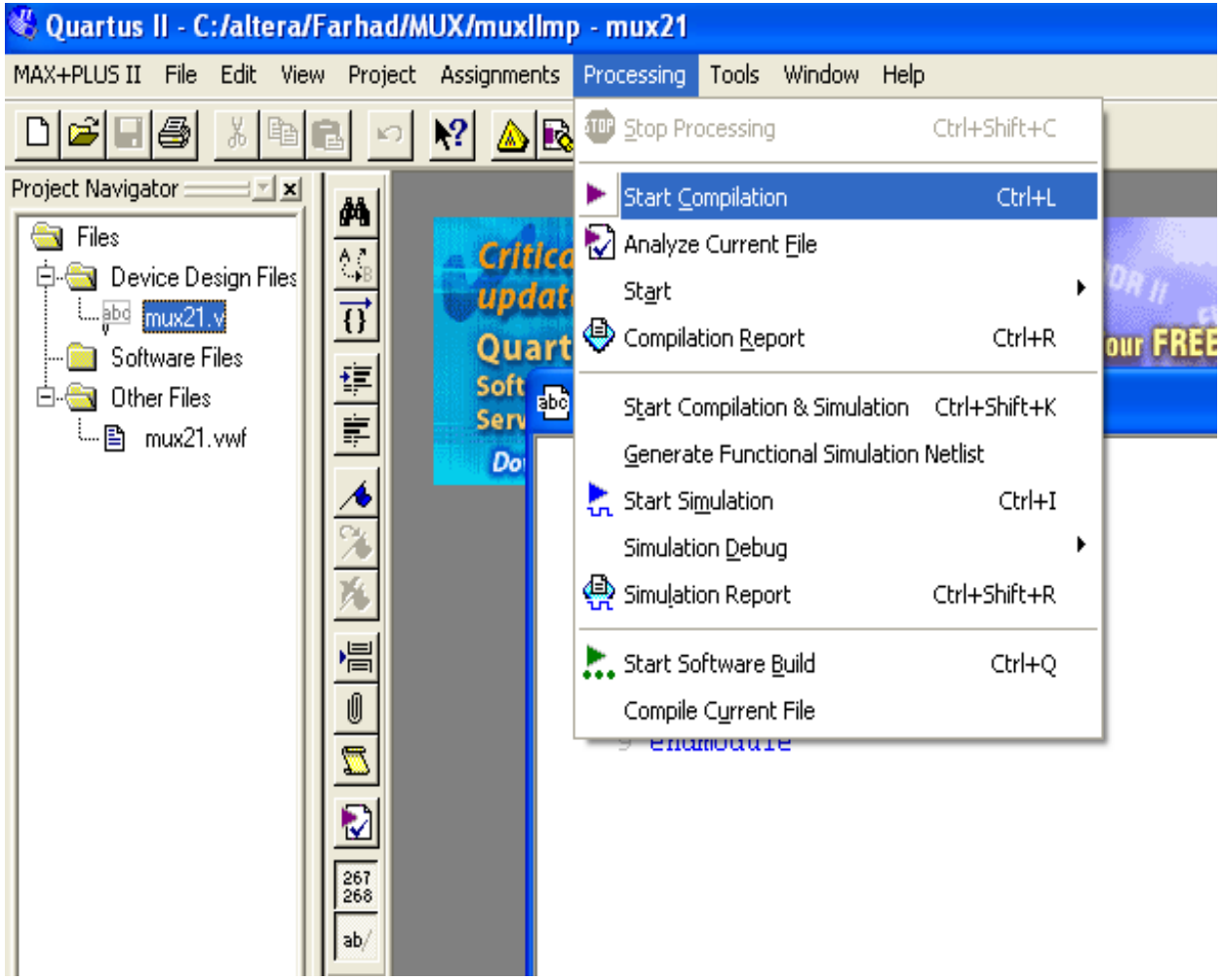


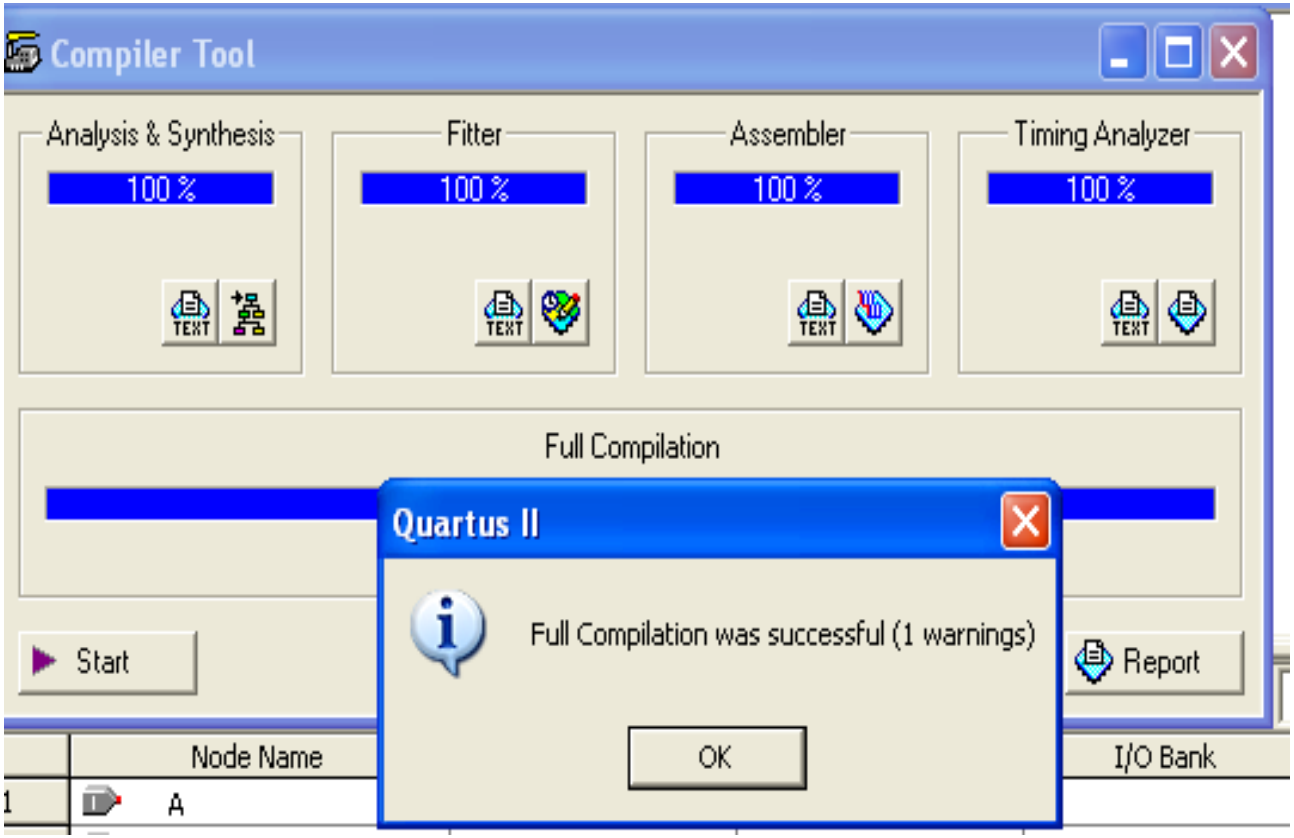
Create a vector waveform file to synthesize and add to the project

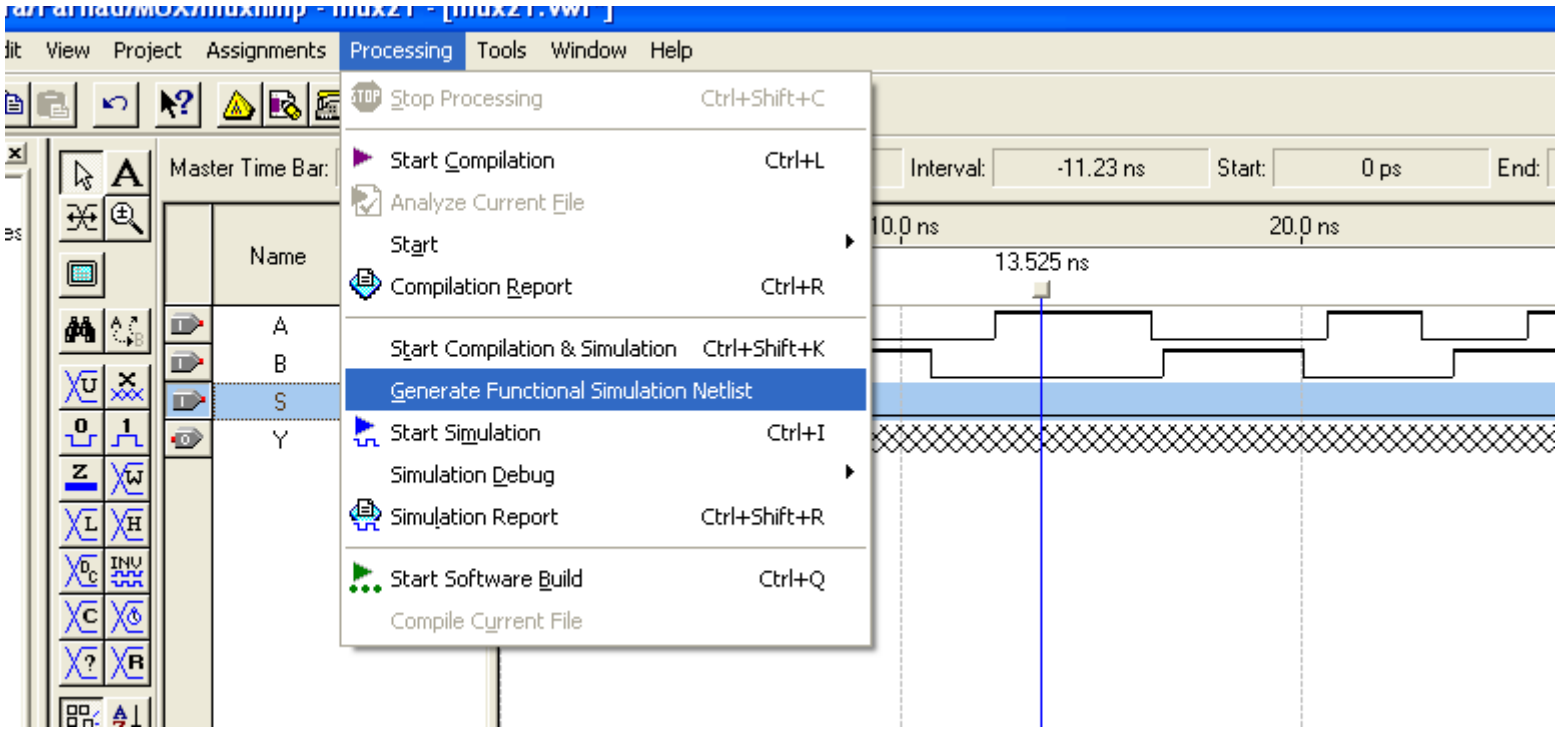


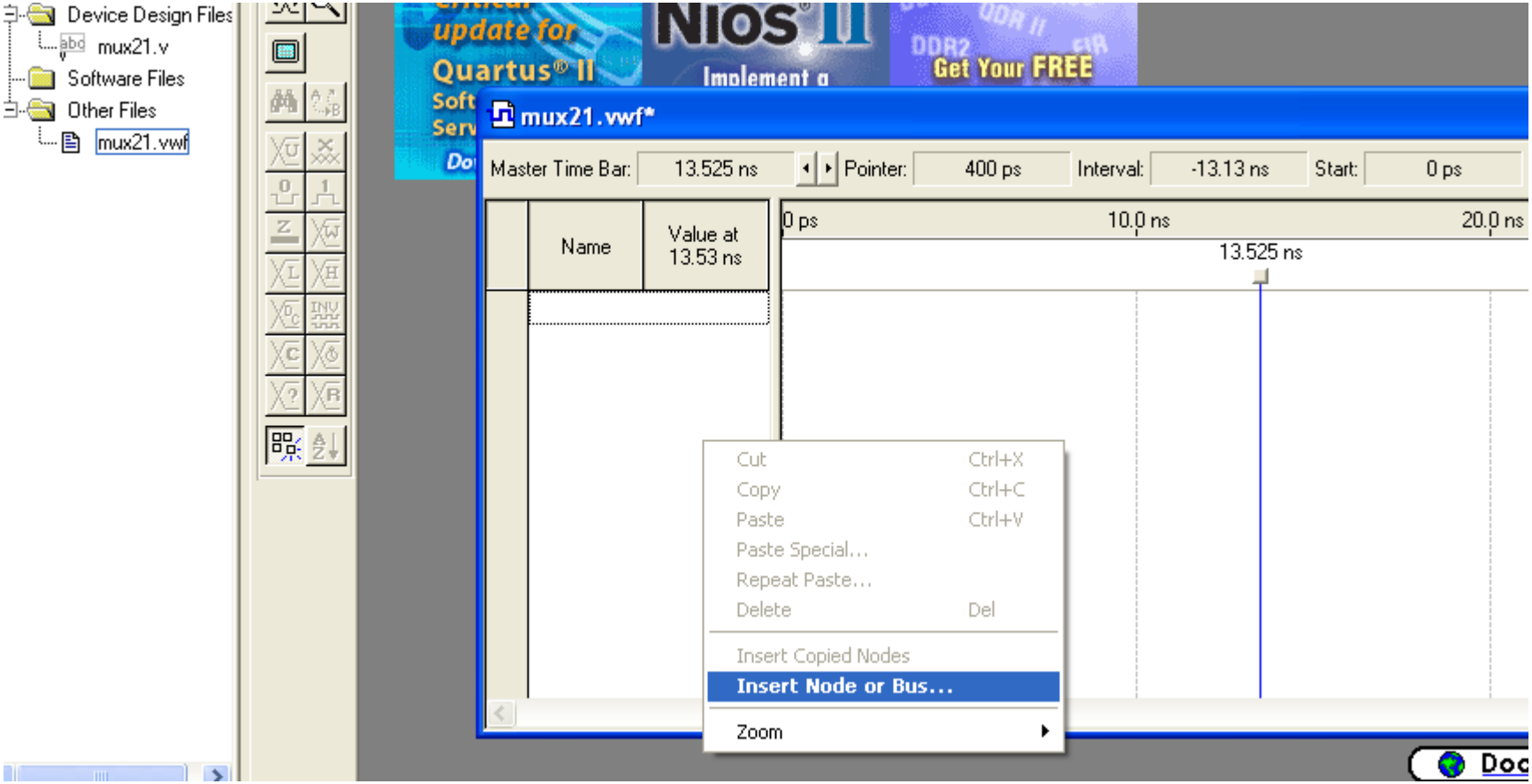

Quartus II - C:/altera/Farhad/MUX/muxIImp - mux21
MAX+PLUS II File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Files
Device Design Files
mux21.v
Software Files
Other Files
mux21.vwf
Device...
Pins
Timing Settings...
EDA Tool Settings...
Settings... Ctrl+Shift+E
Timing Wizard...
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Demote Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment (Time) Groups...
Timing Closure Floorplan
LogicLock Regions Window Alt+L
Design Partitions Window Alt+D
A, B, S, Y);
B or S)begin
Y = A;
B;

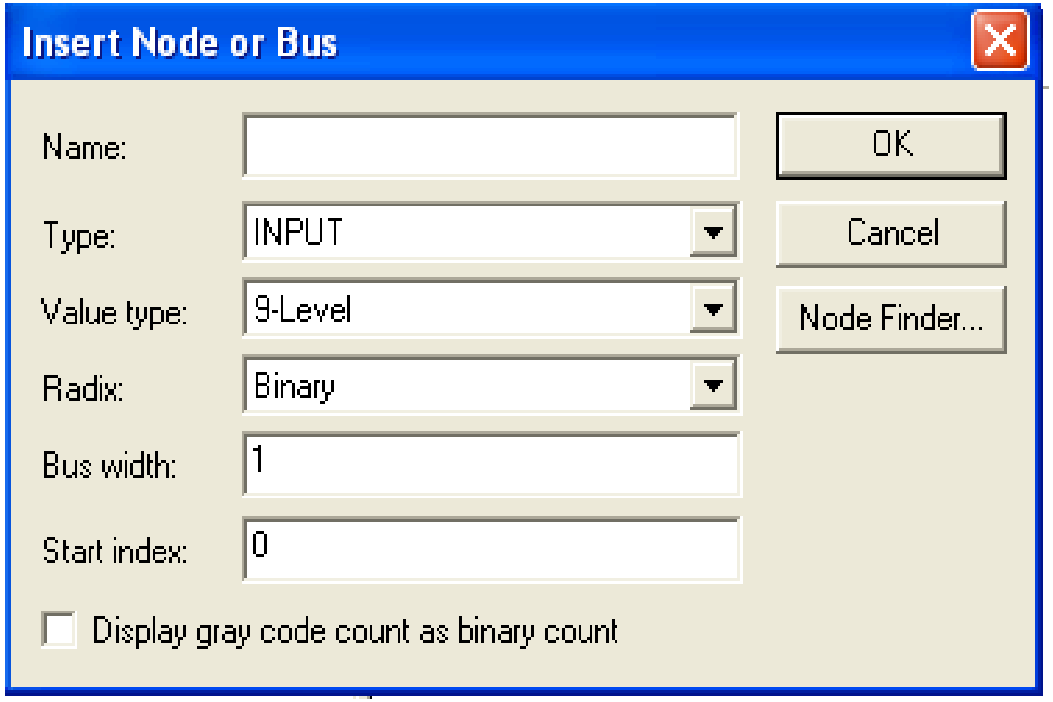

Settings - mux21
Category:
General
Files
User Libraries (Current Project)
Device
Timing Requirements & Options
EDA Tool Settings
Design Entry/Synthesis
Simulation
Timing Analysis
Board-Level
Formal Verification
Physical Synthesis
Compilation Process Settings
Analysis & Synthesis Settings
Fitter Settings
Assembler
Timing Analyzer
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
SignalProbe Settings
Simulator Settings
Simulation Power
PowerPlay Power Analyzer Settings
Software Build Settings
Simulator Settings
Select simulation options.
Simulation mode: Functional
Functional
Timing
Timing using Fast Timing Model
Simulation input:
Simulation period
Run simulation until all vector stimuli are used
End simulation at:
ns
Automatically add pins to simulation output waveforms
Group bus channels in simulation results
Check outputs
Waveform Compare Settings...
Setup and hold time violation detection
Glitch detection:
1
ns
Simulation coverage reporting
Overwrite simulation input file with simulation results
Preserve fewer signal transitions to reduce memory requirements
uPCore Transaction Model File Name:
...
Description:
Specifies the type of simulation to perform for the current Simulation focus.
OK
Cancel

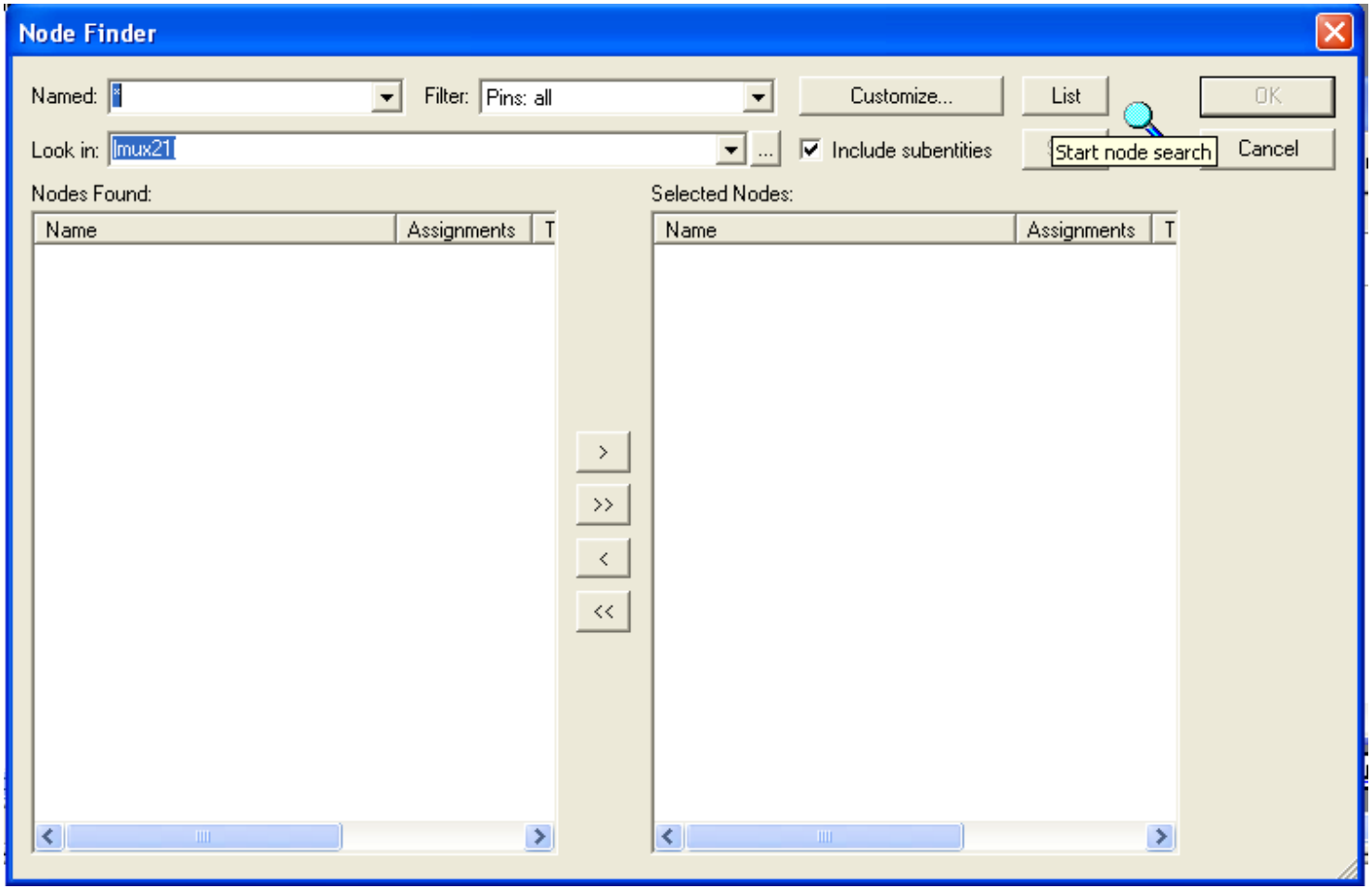

Quartus II - C:/altera/Farhad/MUX/muxIImp - mux21
MAX+PLUS II
File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
Project Navigator
Files
Device Design Files
mux21.v
Software Files
Other Files
mux21.vwf
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Compilation Report Ctrl+R
Start Compilation & Simulation Ctrl+Shift+K
Generate Functional Simulation Netlist
Start Simulation Ctrl+I
Simulation Debug
Simulation Report Ctrl+Shift+R
Start Software Build Ctrl+Q
Compile Current File

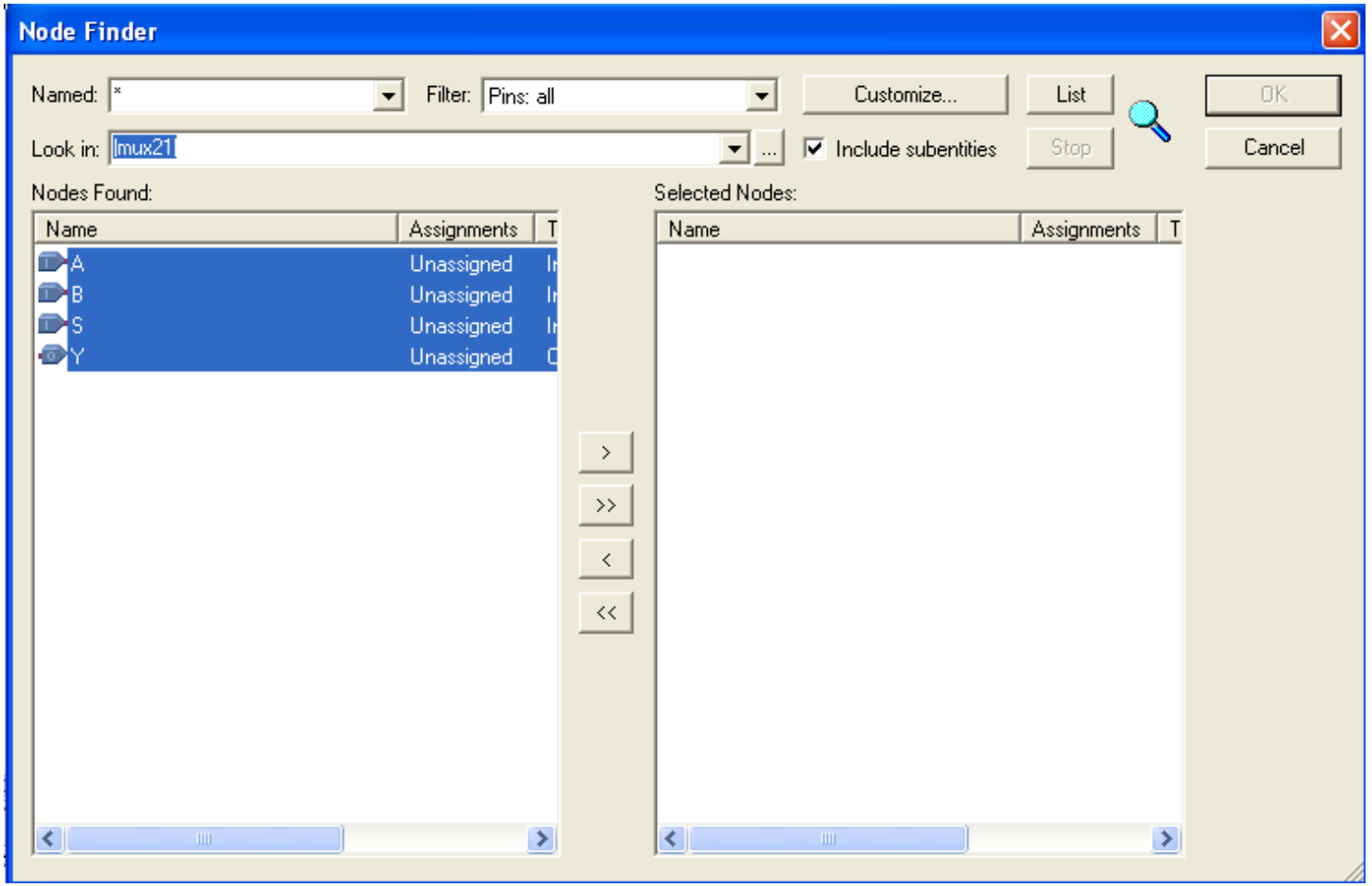

Compiler Tool
Analysis & Synthesis
100 %
Fitter
100 %
Assembler
100 %
Timing Analyzer
100 %
Full Compilation
Start
Report
Node Name
I/O Bank
A
Quartus II
Full Compilation was successful (1 warnings)
OK

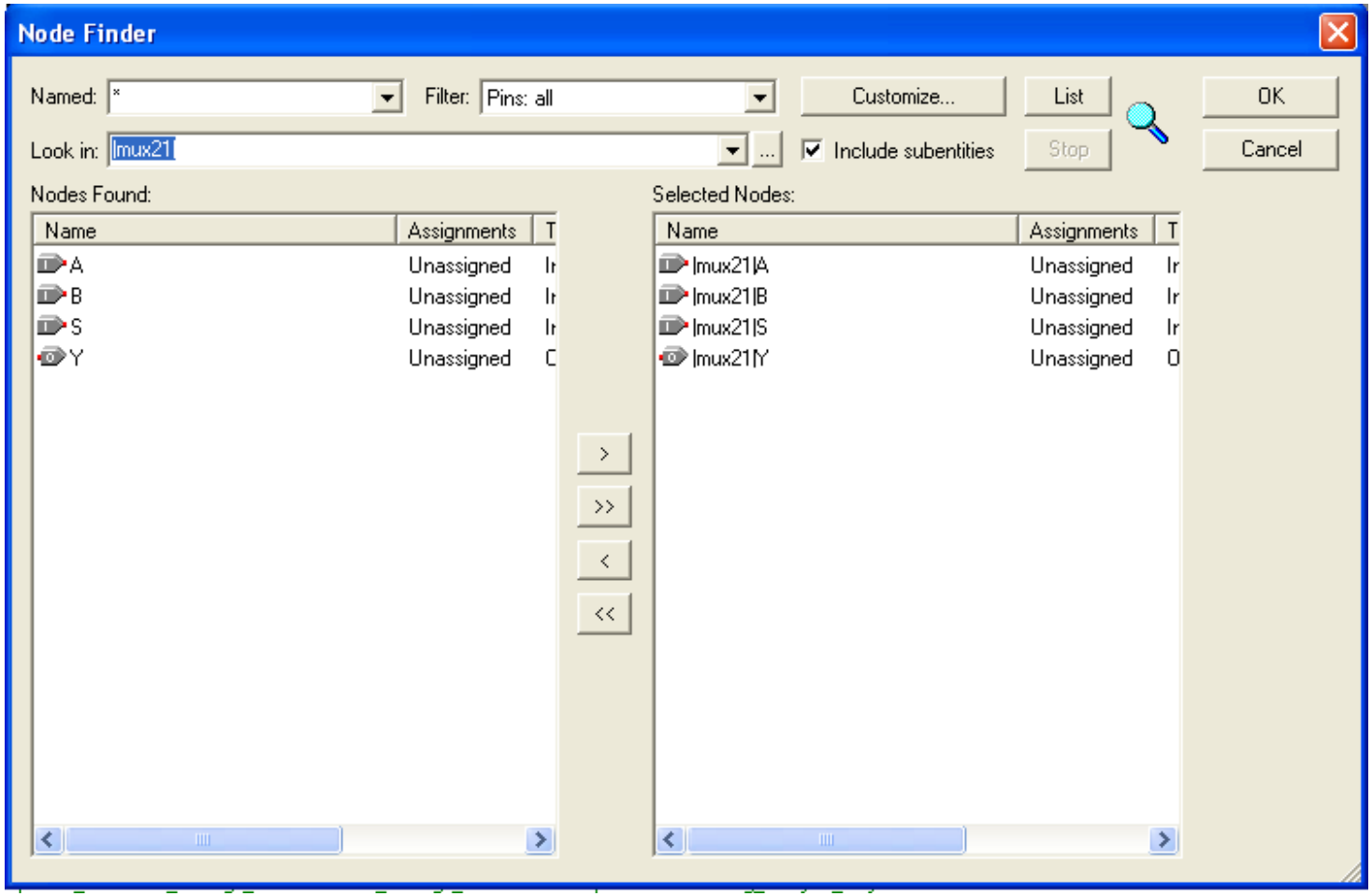

View
Project
Assignments
Processing
Tools
Window
Help
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Compilation Report Ctrl+R
Start Compilation & Simulation Ctrl+Shift+K
Generate Functional Simulation Netlist
Start Simulation Ctrl+I
Simulation Debug
Simulation Report Ctrl+Shift+R
Start Software Build Ctrl+Q
Compile Current File
Master Time Bar:
Interval: -11.23 ns
Start: 0 ps
End:
Name
A
B
S
Y
10.0 ns
20.0 ns
13.525 ns

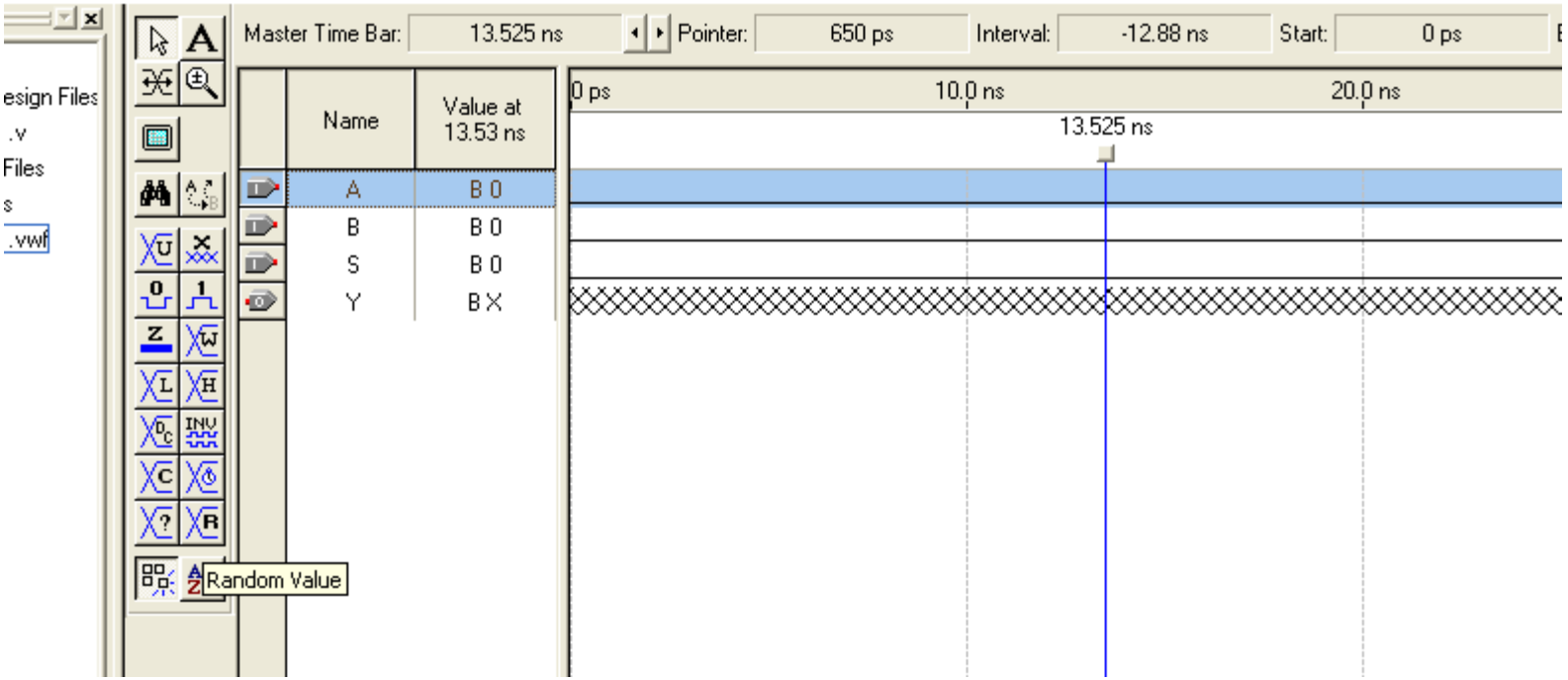

Device Design Files
mux21.v
Software Files
Other Files
mux21.vwf
update for
Quartus® II
NIOS II
Get Your FREE
mux21.vwf*
Master Time Bar: 13.525 ns
Pointer: 400 ps
Interval: -13.13 ns
Start: 0 ps
Name
Value at 13.53 ns
0 ps
10.0 ns
20.0 ns
13.525 ns
Cut Ctrl+X
Copy Ctrl+C
Paste Ctrl+V
Paste Special...
Repeat Paste...
Delete Del
Insert Copied Nodes
Insert Node or Bus...
Zoom

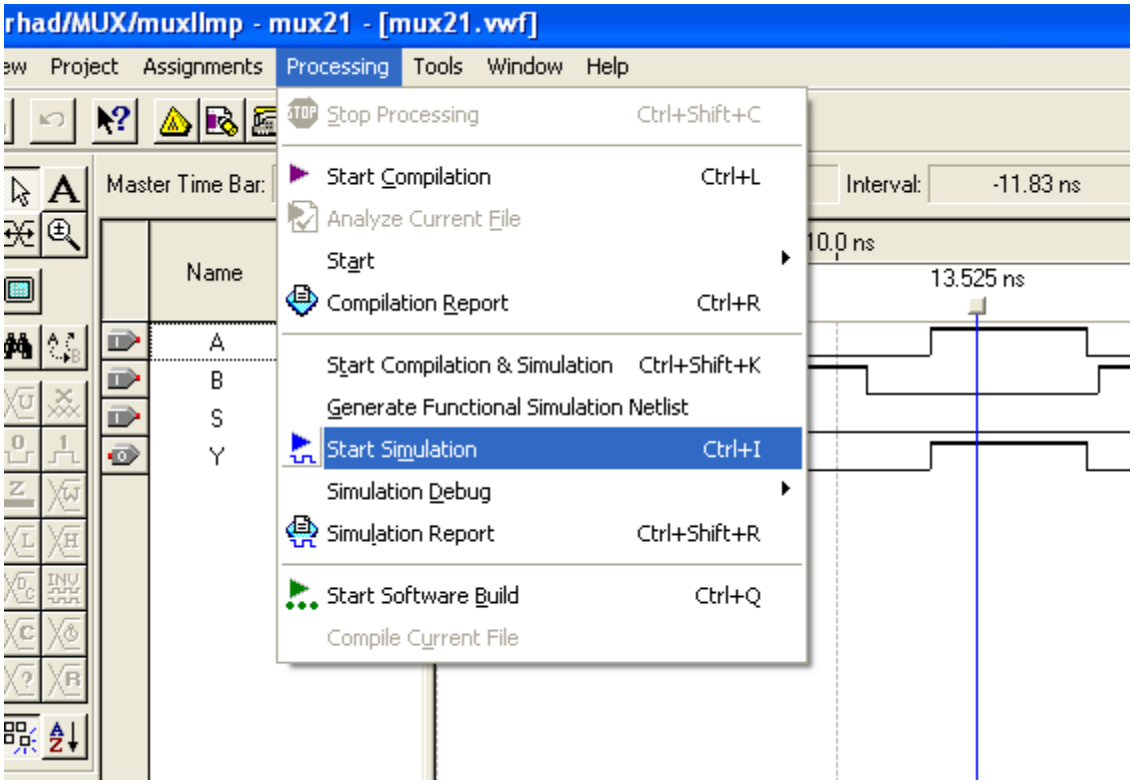

Insert Node or Bus
Name:
Type:
INPUT
Value type:
9-Level
Radix:
Binary
Bus width:
1
Start index:
0
Display gray code count as binary count
OK
Cancel
Node Finder...

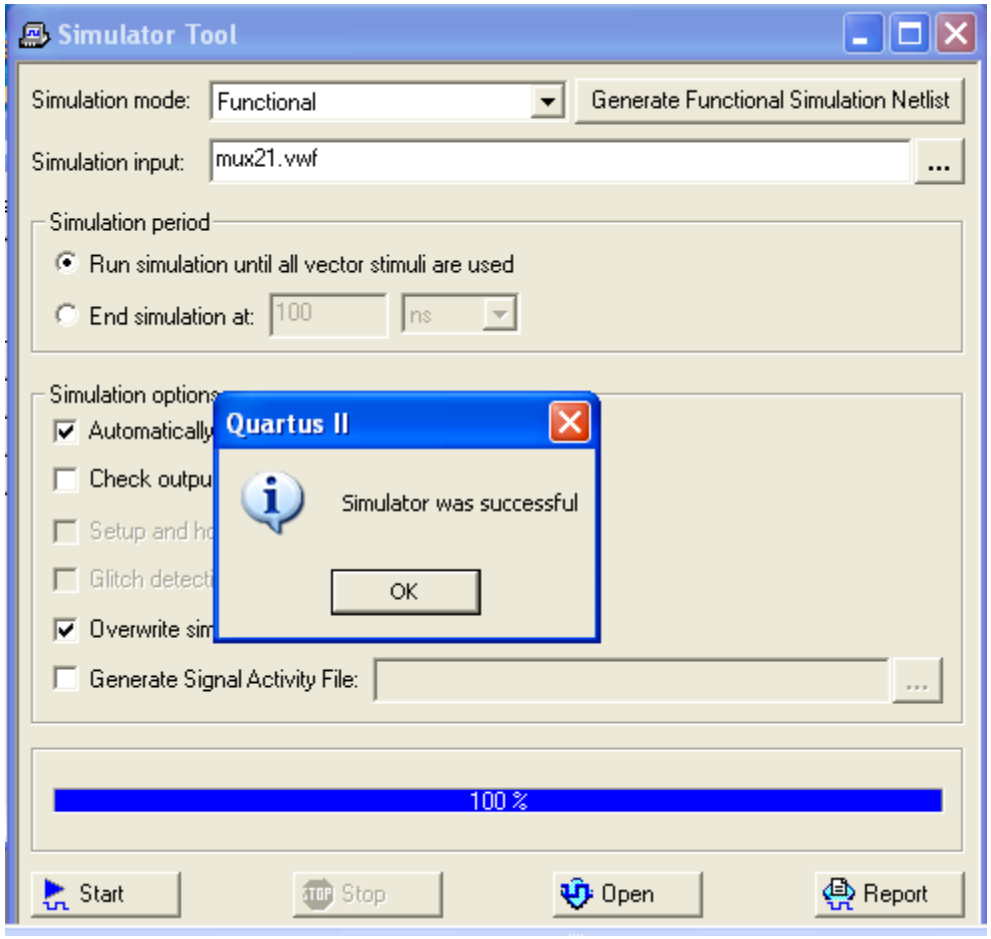

Node Finder
Named:
*
Filter:
Pins: all
Customize...
List
OK
Look in:
lmux21
...
Include subentities
Start node search
Cancel
Nodes Found:
Name
Assignments
T
Selected Nodes:
Name
Assignments
T
>
>>
<
<<

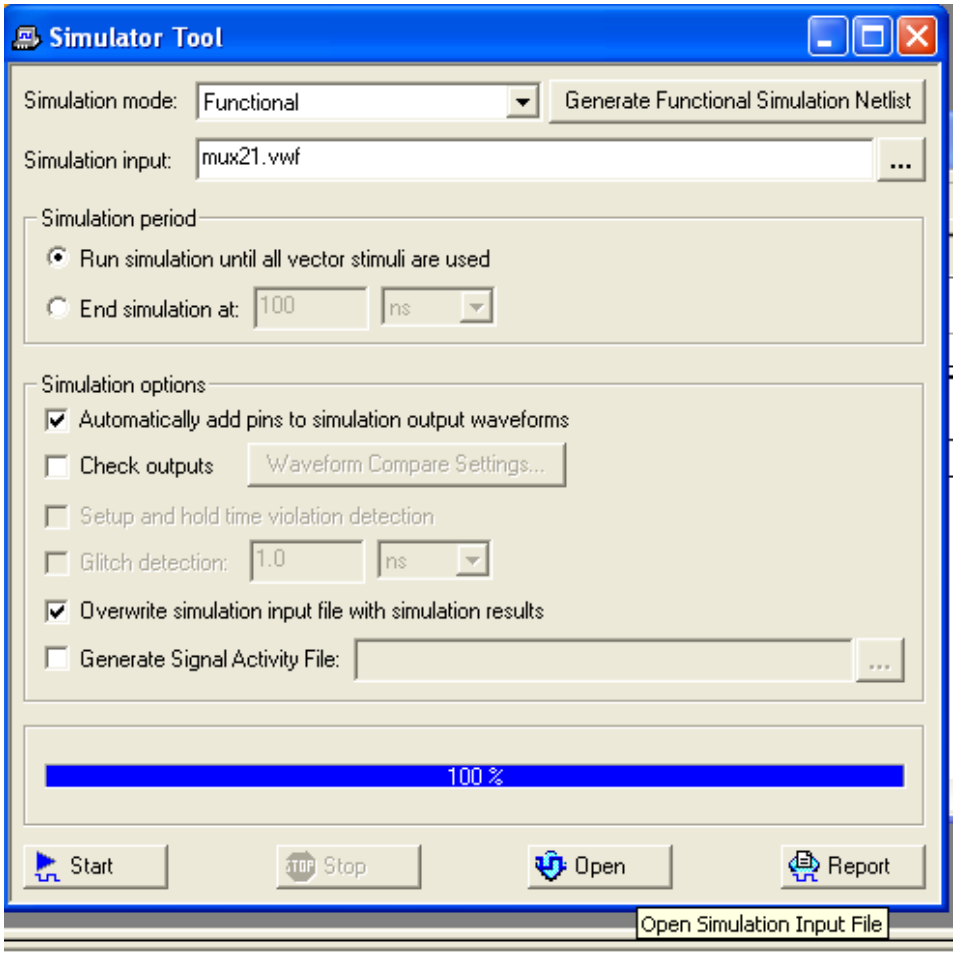

Node Finder
Named: *
Filter: Pins: all
Customize...
List
OK
Look in: lmux21
Include subentities
Stop
Cancel
Nodes Found:
Name
Assignments
A
Unassigned
B
Unassigned
S
Unassigned
Y
Unassigned
Selected Nodes:
Name
Assignments

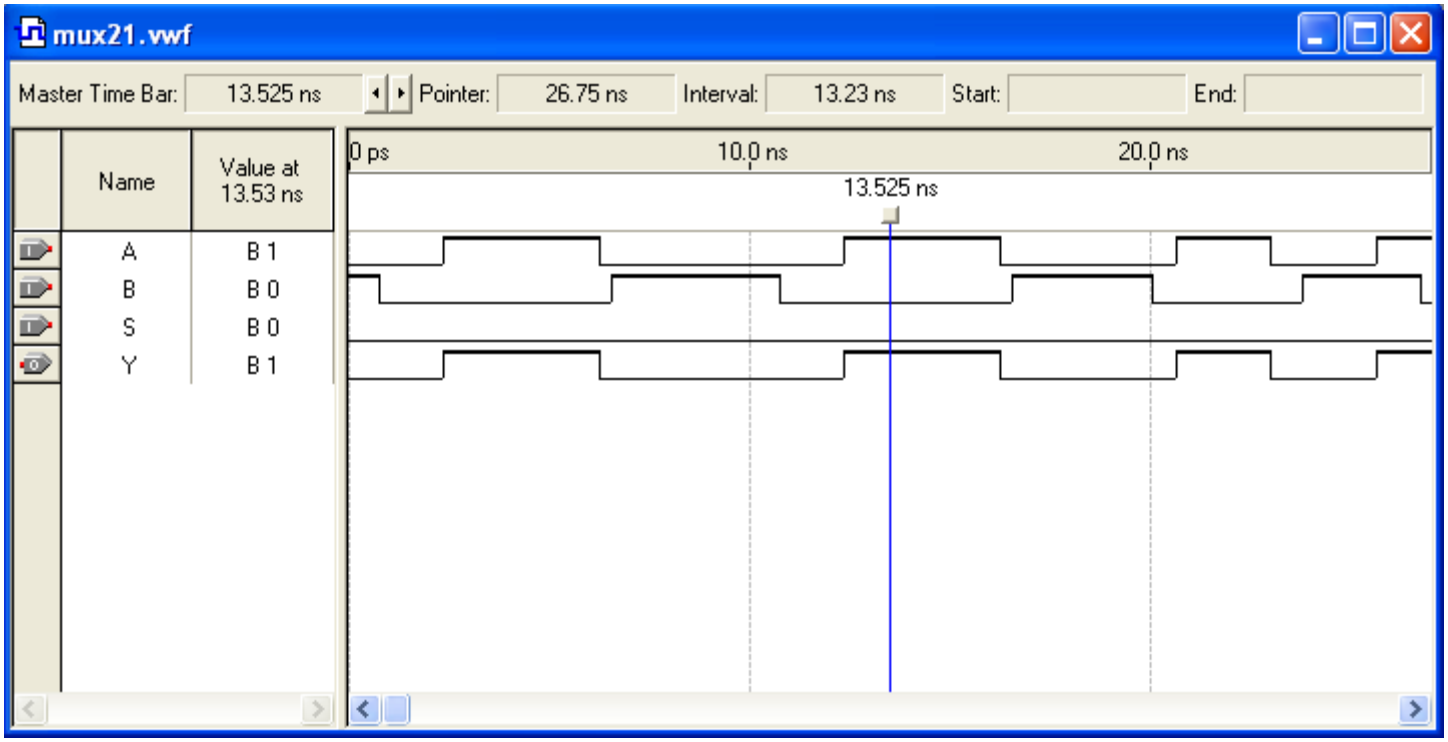

Node Finder
Named: *
Filter: Pins: all
Customize...
List
OK
Look in: |mux21
Include subentities
Stop
Cancel
Nodes Found:
Name
Assignments
A
Unassigned
B
Unassigned
S
Unassigned
Y
Unassigned
Selected Nodes:
Name
Assignments
|mux21|A
Unassigned
|mux21|B
Unassigned
|mux21|S
Unassigned
|mux21|Y
Unassigned


Master Time Bar:
13.525 ns
Pointer:
650 ps
Interval:
-12.88 ns
Start:
0 ps
Name
Value at
13.53 ns
A
B 0
B
B 0
S
B 0
Y
B X
0 ps
10.0 ns
20.0 ns
13.525 ns
Random Value


rhad/MUX/muxIImp - mux21 - [mux21.vwf]
ew Project Assignments Processing Tools Window Help
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Compilation Report Ctrl+R
Start Compilation & Simulation Ctrl+Shift+K
Generate Functional Simulation Netlist
Start Simulation Ctrl+I
Simulation Debug
Simulation Report Ctrl+Shift+R
Start Software Build Ctrl+Q
Compile Current File
Master Time Bar:
Interval: -11.83 ns
Name
A
B
S
Y
10.0 ns
13.525 ns


Simulator Tool
Simulation mode:
Functional
Generate Functional Simulation Netlist
Simulation input:
mux21.vwf
...
Simulation period
Run simulation until all vector stimuli are used
End simulation at:
100
ns
Simulation options
Automatically
Check outpu
Setup and ho
Glitch detect
Overwrite sim
Generate Signal Activity File:
Quartus II
Simulator was successful
OK
100 %
Start
Stop
Open
Report


Simulator Tool
Simulation mode:
Functional
Generate Functional Simulation Netlist
Simulation input:
mux21.vwf
...
Simulation period
Run simulation until all vector stimuli are used
End simulation at:
100
ns
Simulation options
Automatically add pins to simulation output waveforms
Check outputs
Waveform Compare Settings...
Setup and hold time violation detection
Glitch detection:
1.0
ns
Overwrite simulation input file with simulation results
Generate Signal Activity File:
...
100 %
Start
Stop
Open
Report
Open Simulation Input File


mux21.vwf
Master Time Bar: 13.525 ns
Pointer: 26.75 ns
Interval: 13.23 ns
Start:
End:
Name
Value at 13.53 ns
0 ps
10.0 ns
20.0 ns
13.525 ns
A
B 1
B
B 0
S
B 0
Y
B 1

The End