Brac University

EEE 412/ ECE 412/ CSE 460

VLSI Design Laboratory

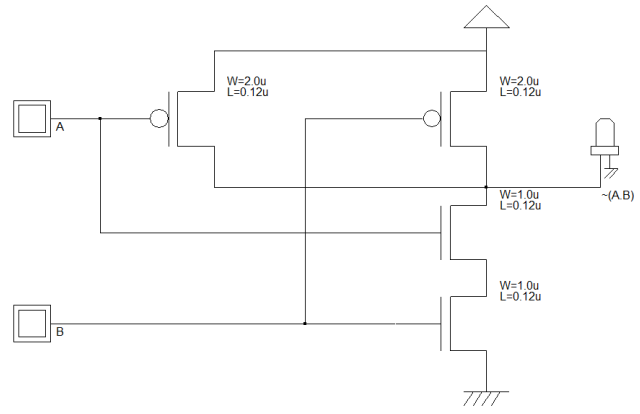
Experiment Title: Simulation of sequential circuits using DSCH2 Software

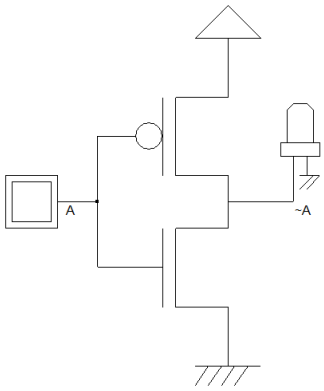
Theory:

A sequential circuit is a logical circuit, where the output depends on the present value of the input signal as well as the sequence of past inputs. While a combinational circuit is a function of present input only. A sequential circuit is a combination of combinational circuit and a storage element.

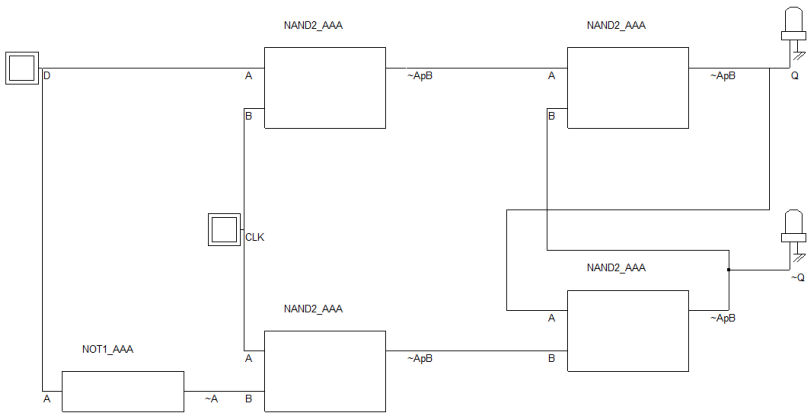
The basic elements of sequential circuits are Latch and Flip-flops. They are the memory/storage elements. The basic difference between latch and flipflops are that latch are level triggered and flipflops are edge triggered. In case of D-latch, when the clock is high, the data in the input is sent to the output and when clock is low, the output holds its previous value. In case of D-Flipflop, the data from the input moves to the output only at the positive edge or negative edge of clock. For all other time, the output stores its previous value.

First task before we make a latch or flipflop is to make a NAND and NOT gate using CMOS technology.

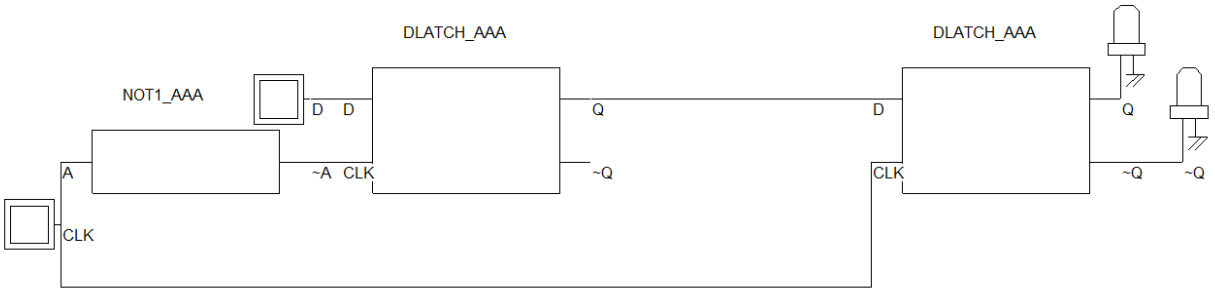




We then build a block of the gates and make the latch using the following circuit connection:



We can observe that the circuit is working as a level triggered latch. We then make a block out of the circuit. Then combining two latches, we build an edge-triggered D-Flipflop.

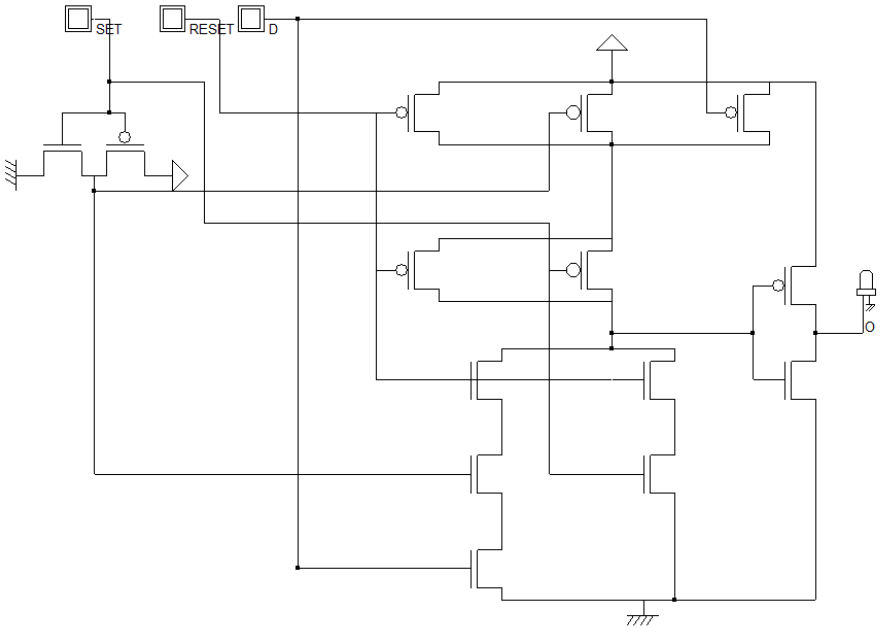


We now want to add set and reset operation to our flipflop. We can design a controller and add to the block to perform the task of set and reset.

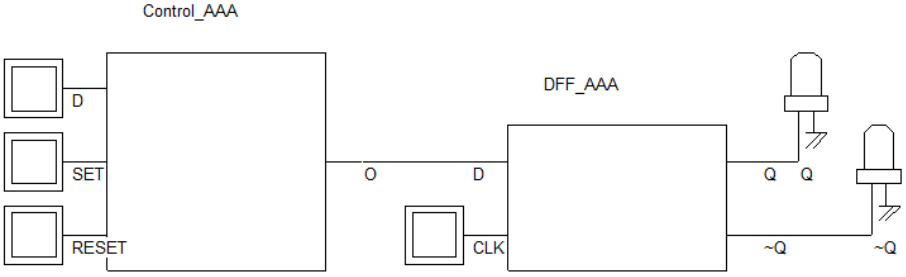
The controller will give highest priority to reset. When reset=0, output=0. Second most priority will be given to set. When Reset=0 and set=1, output=1. At all other times, output=data. So the truth table and CMOS implementation look like the following:

Reset	Set	D	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

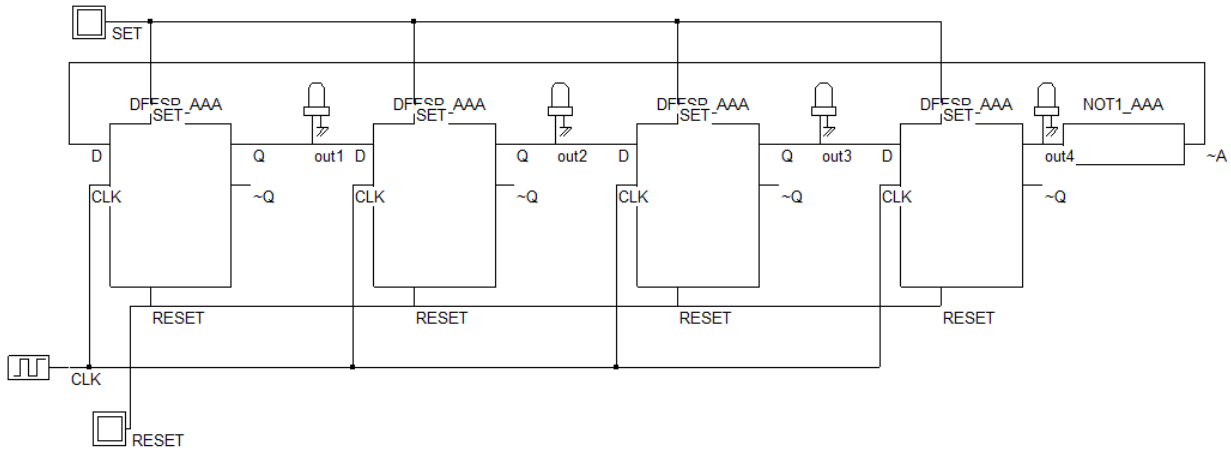
O=$Reset.\overline{Set}.D + Reset.Set$



We then from a block of the controller and connect with the flipflop as follows to make a D flipflop with set-reset operations:



We can now make this into a block and make a Johnson counter by using the following connection:



Labwork:

1. Design NAND and NOT gate using CMOS.
2. Design a DLatch.
3. Design a D Flip-flop with set and reset operations
4. Design a Johnson counter

Homework:

1. Design an end round shift register.
2. Design a 4 bit counter.
3. Design a 2 to 10 counter.