Experiment 5

CSE460: VLSI Design Lab

Submitted To

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Submitted By

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Task 01:

AND Gate -

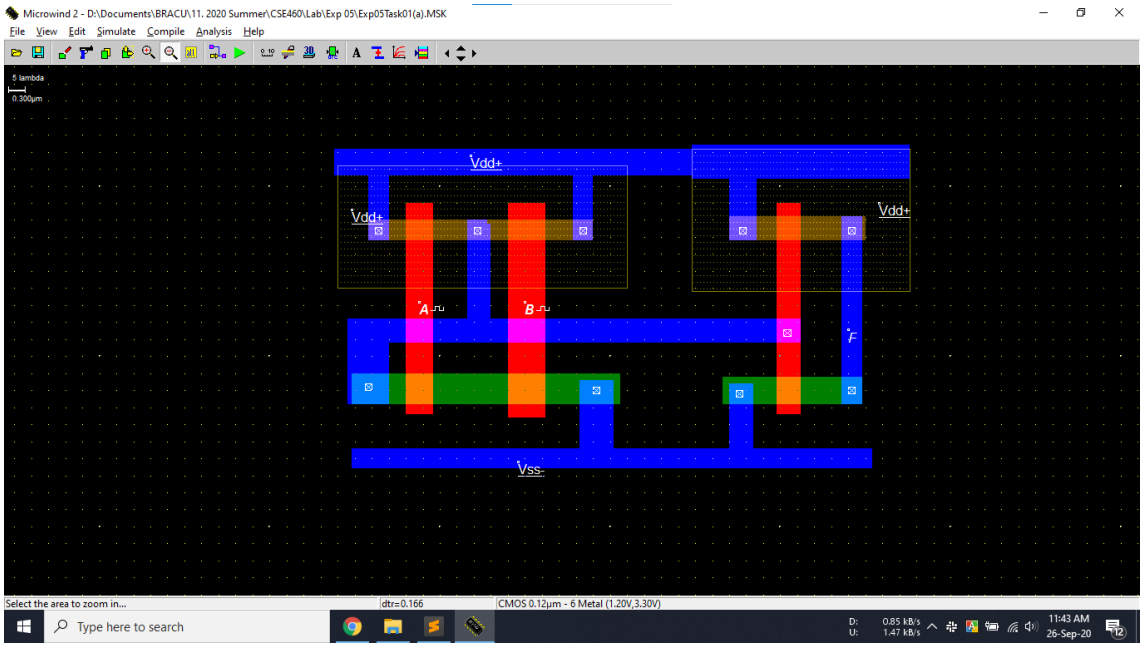

Figure 1: AND Gate layout using CMOS

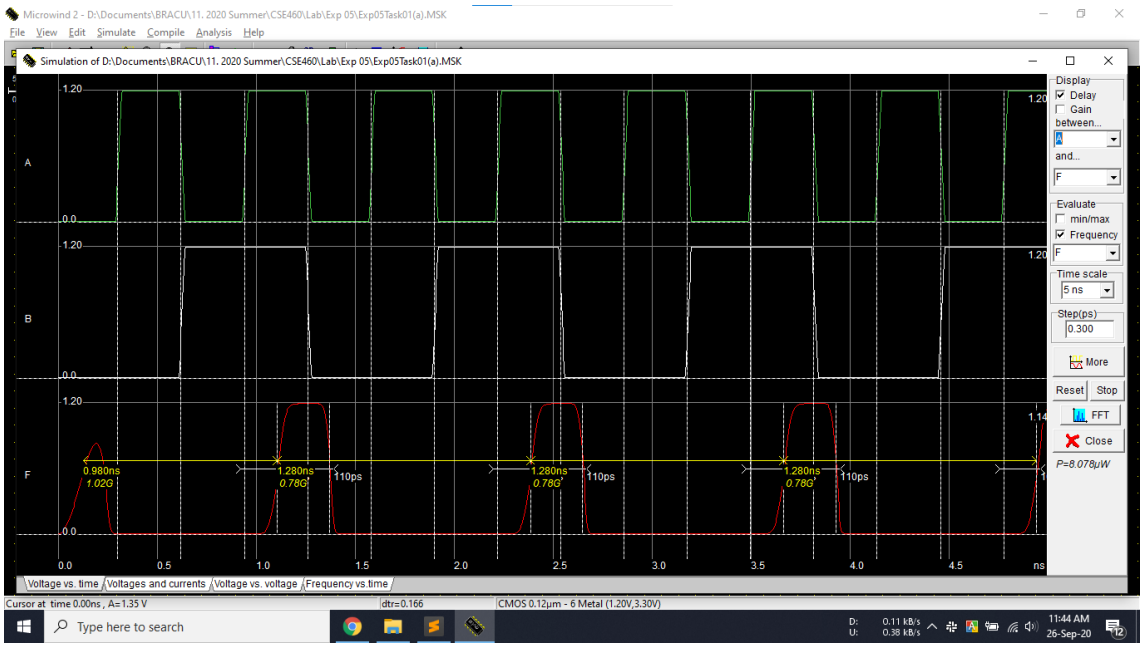

Figure 2: Simulation of AND Gate using CMOS

OR Gate -

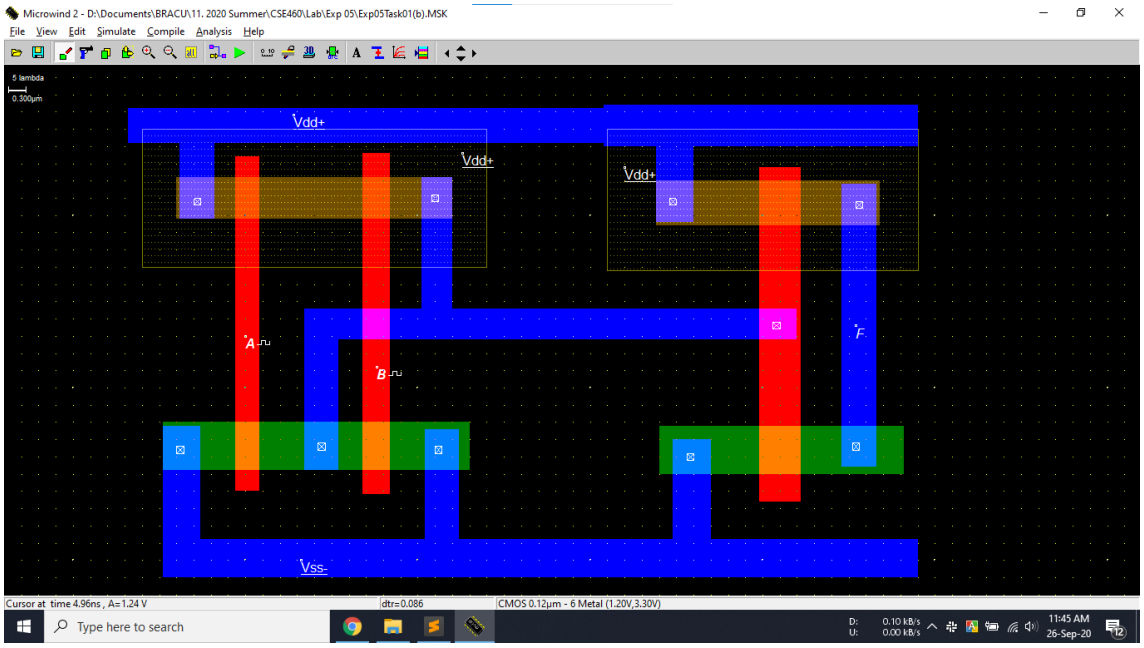

Figure 3: OR Gate layout using CMOS

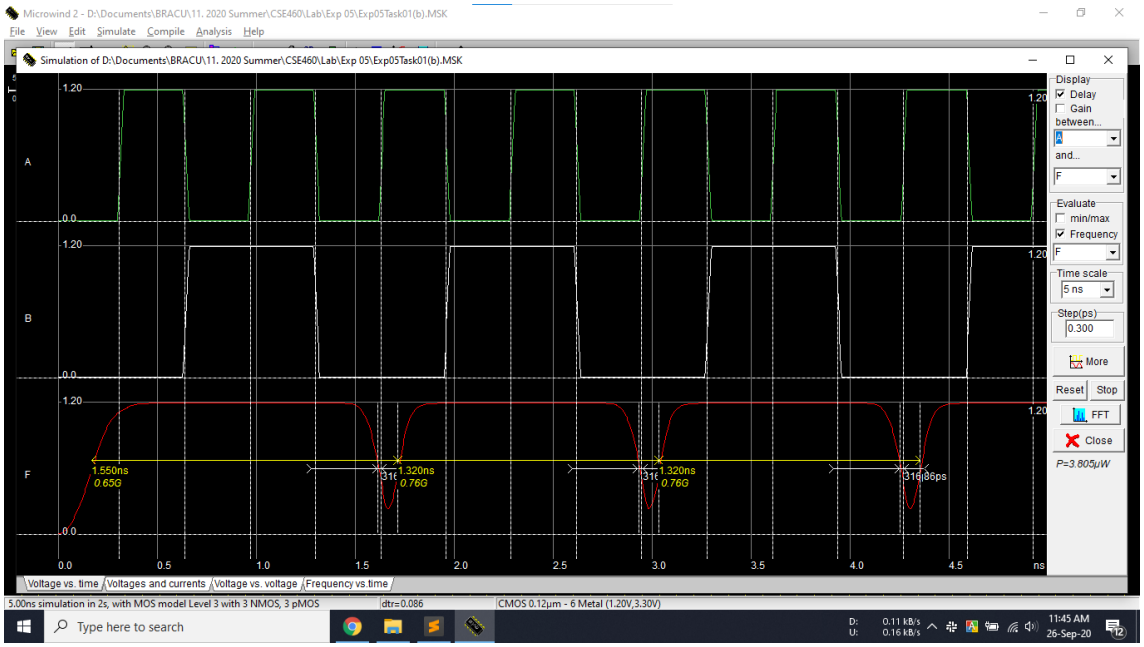

Figure 4: Simulation of OR Gate using CMOS

XOR Gate -

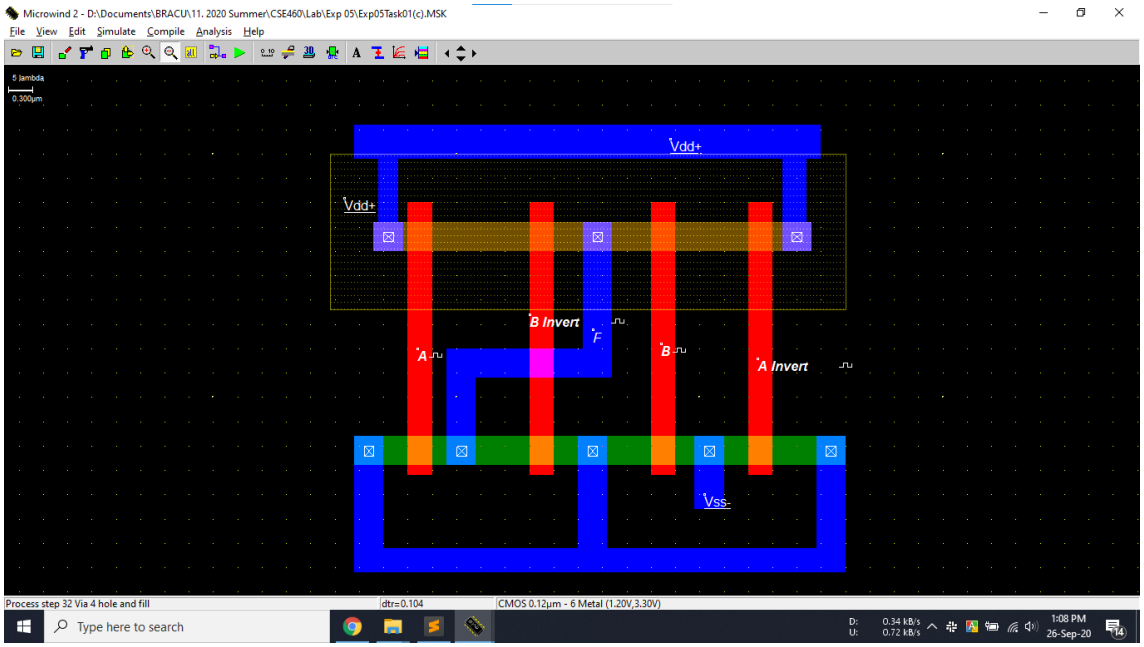

Figure 5: OR Gate layout using CMOS

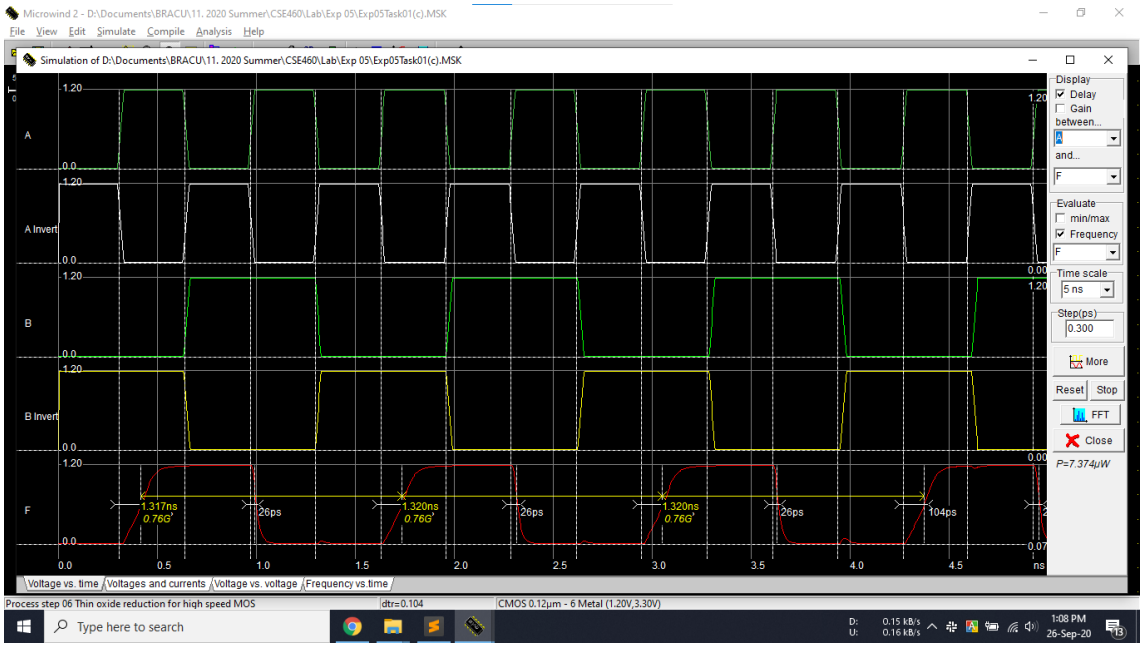

Figure 6: Simulation of XOR Gate using CMOS

Discussion: In Microwind the layout of AND, OR, and XOR gate was drawn following all the design rule. In the N Well, P+ diffusion layer was placed with VDD. In the P-MOS all the VDD connection was given based on the circuit requirement. In the N-MOS groud connection was also provided on the appropriate nodes of N-MOS. Between P-MOS and N-MOS polysilicon was placed and cross connection was provided with metal using N+ / P+ contact. For input clock was used and for XOR as it required inverted input as well. So, the high and low level was inverted which make the output inverted.

Task 02:

2 to 1 MUX -

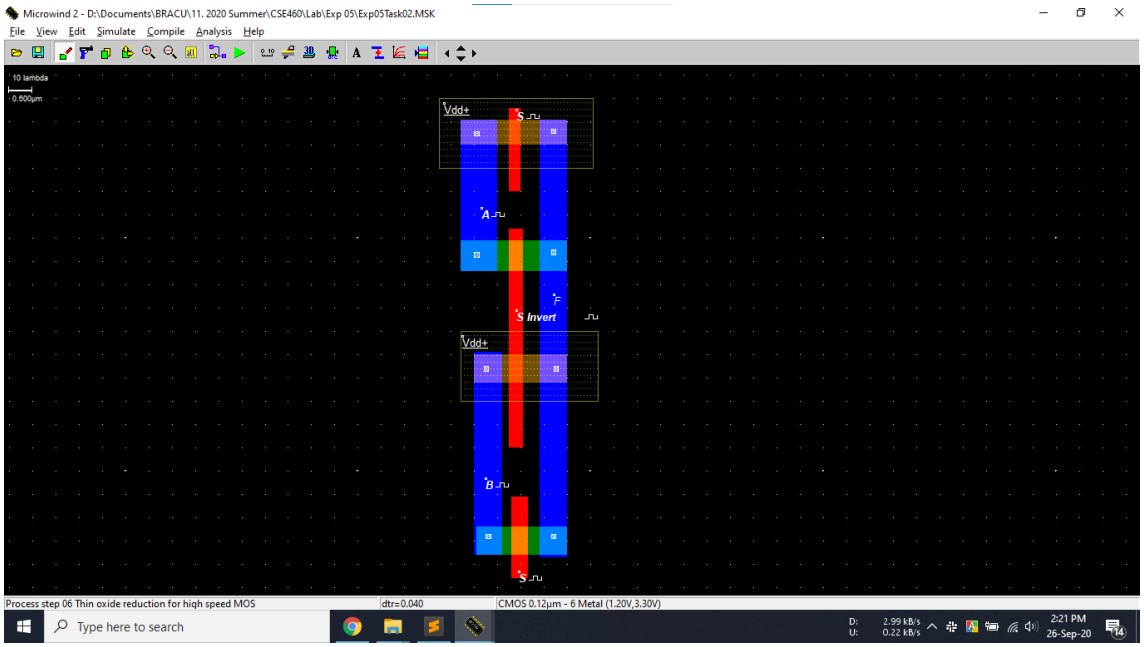

Figure 7: 2 to 1 MUX using CMOS

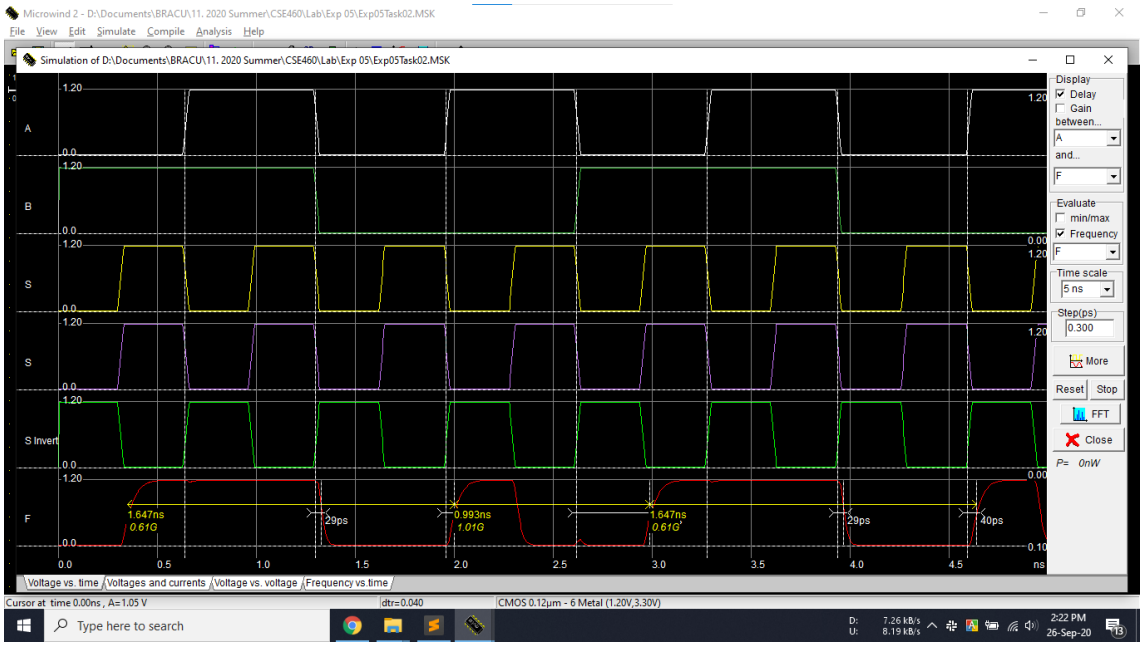

Figure 8: Simulation of 2 to 1 MUX using CMOS

Discussion: MUX is a combinational logic circuit that is used to switch between different inputs. 2 to 1 MUX equation is F = $\bar{S}A+SB$.As it is a 2 to 1 MUX it will require 2 CMOS stacked top of one another. S is the selector pin, A and B is the input and F is the output. Source and drains of the PMOS and CMOS are connected using the metal and the PMOS are situated in the N-Well. We get the output F from the middel of the two CMOS that are internally connected wih source and drain using the Metal. The selector pin is situated on the gates using polysilicon. The output is visualised using the simulation graph.

Task 03:

Given combinational circuit f = (A + B) C

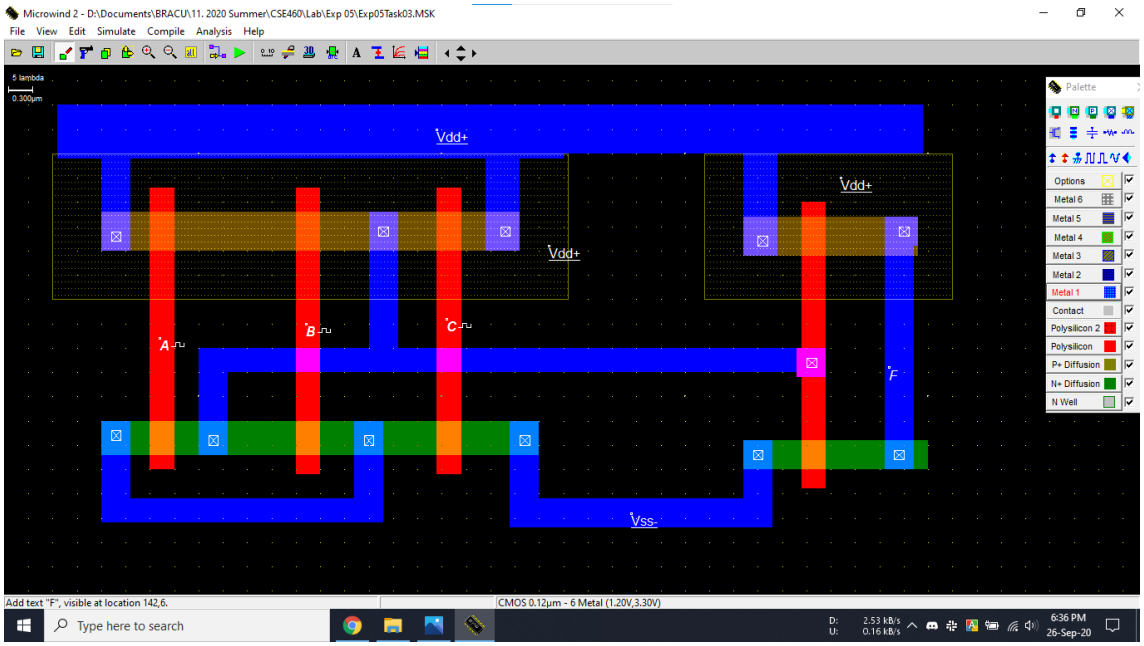

Figure 9: Layout of the combinational circuit

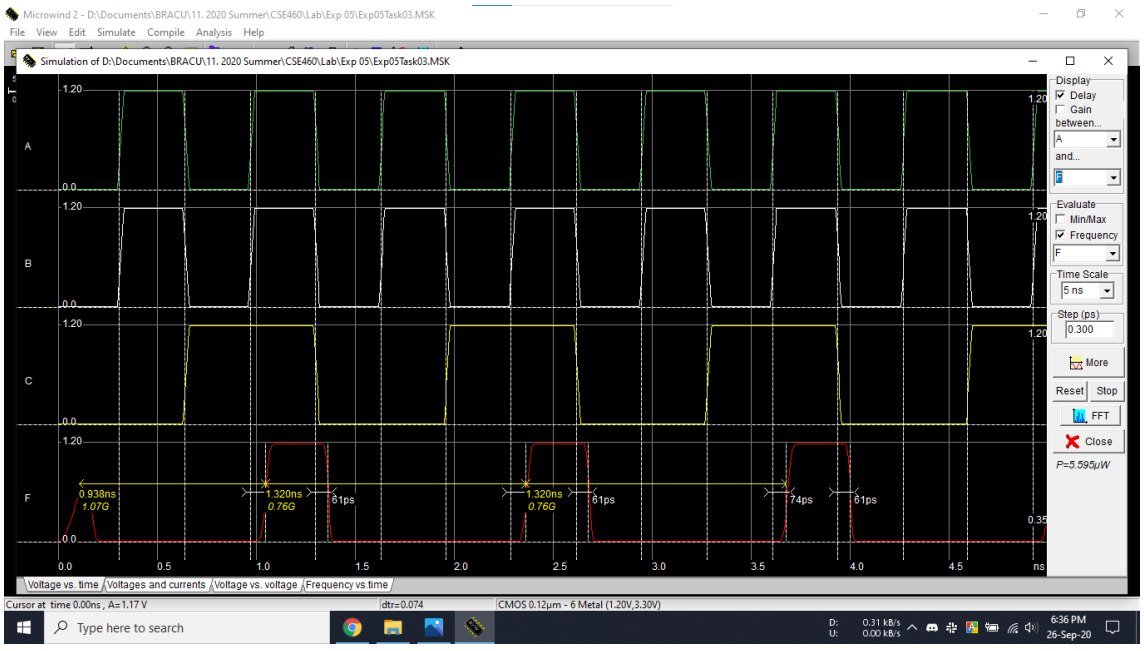

Figure 10: Simulation of the combinational circuit

Discussion: Given combinational circuit was f = (A + B)C was implemented using CMOS. In the N-Well, P-MOS part is situated above the N-MOS. Gates are connected with polysilicon. Cross connection are done using metals with N+ or P+ connectors. As CMOS gives inverted output so the output was passed through a inverter.