Experiment 3

CSE460: VLSI Design Lab

Submitted To

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Submitted By

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Task 01:

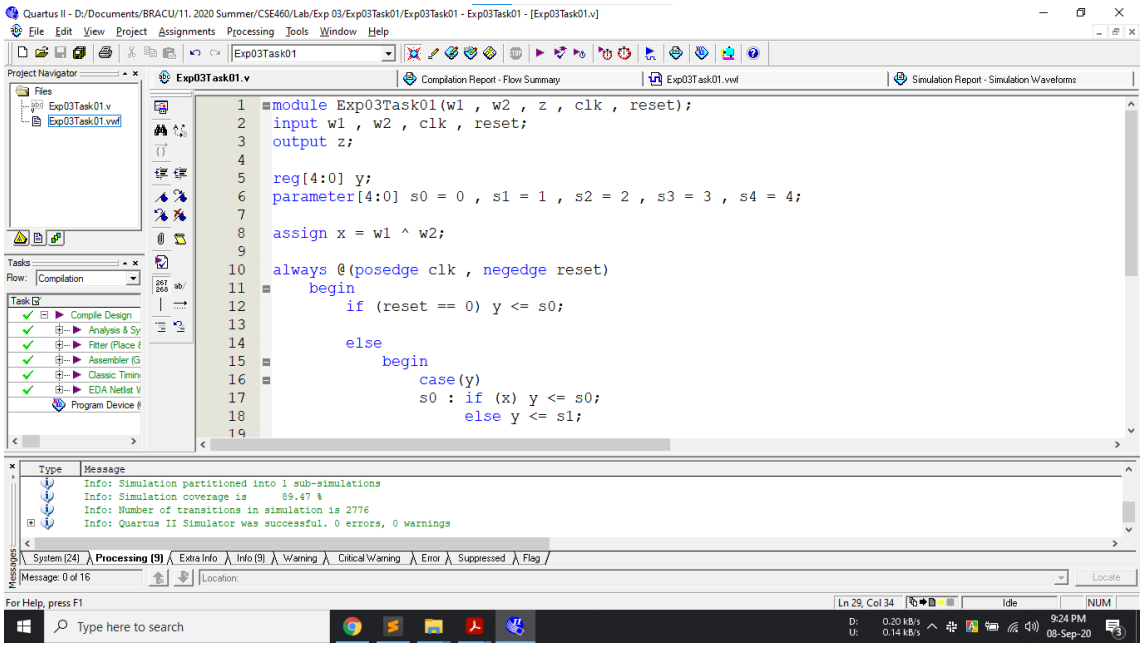

Figure 1: Task 01 Verilog HDL Code [Part 01]

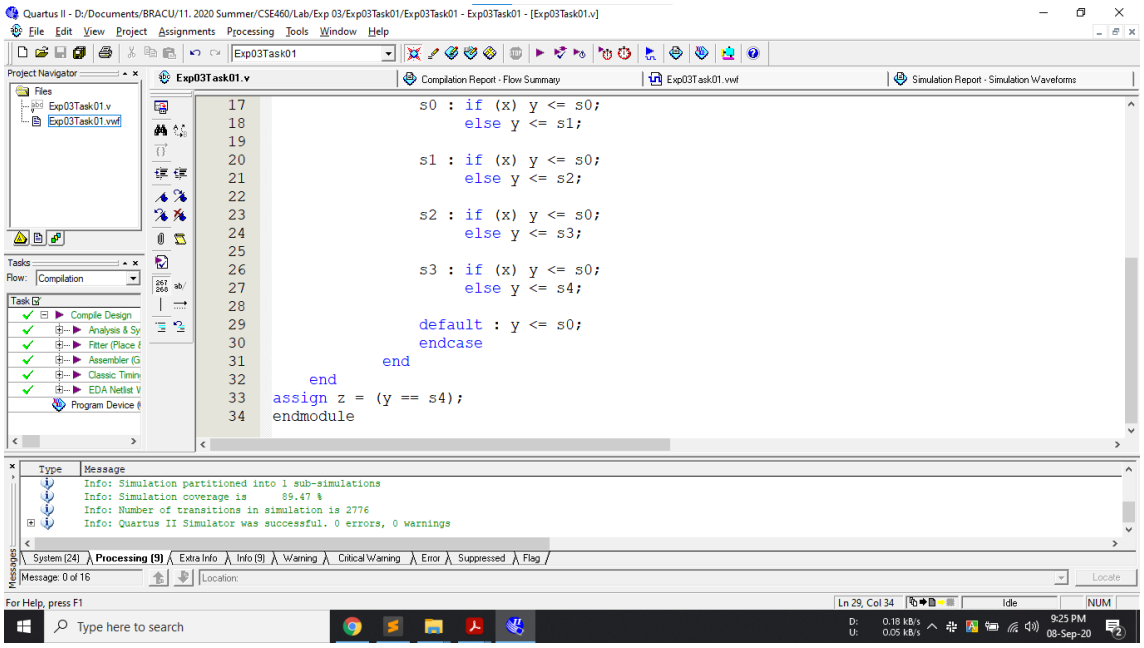

Figure 2: Task 01 Verilog HDL Code [Part 02]

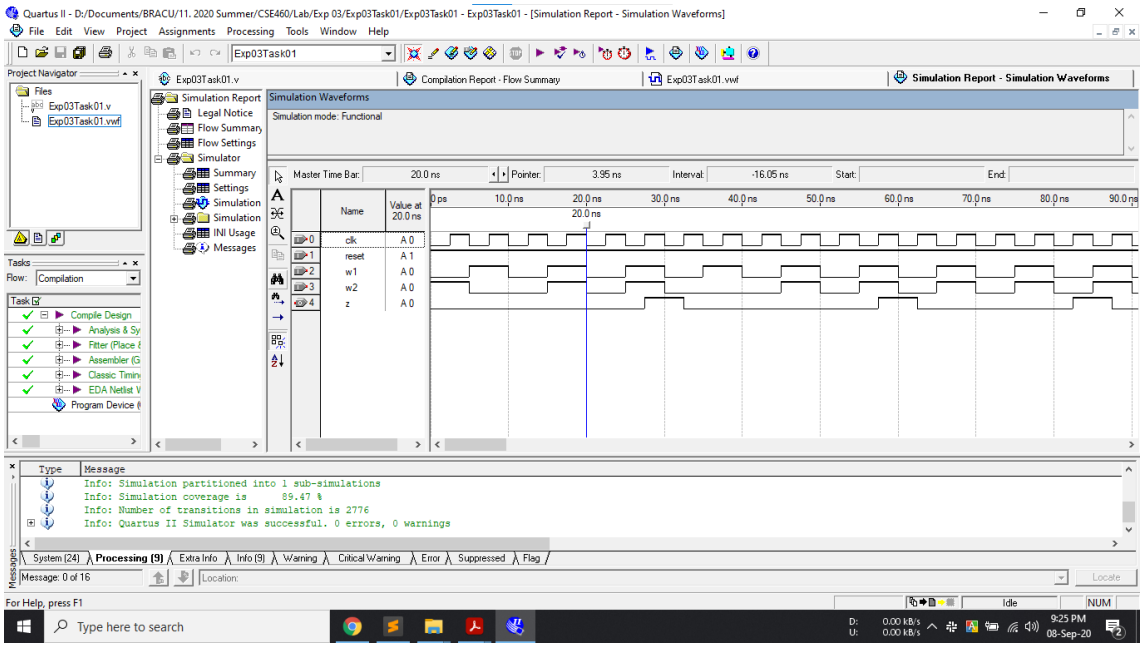

Figure 3: Task 01 Vector Waveform Simulation

Here,
X = w1 XOR w2
z = output

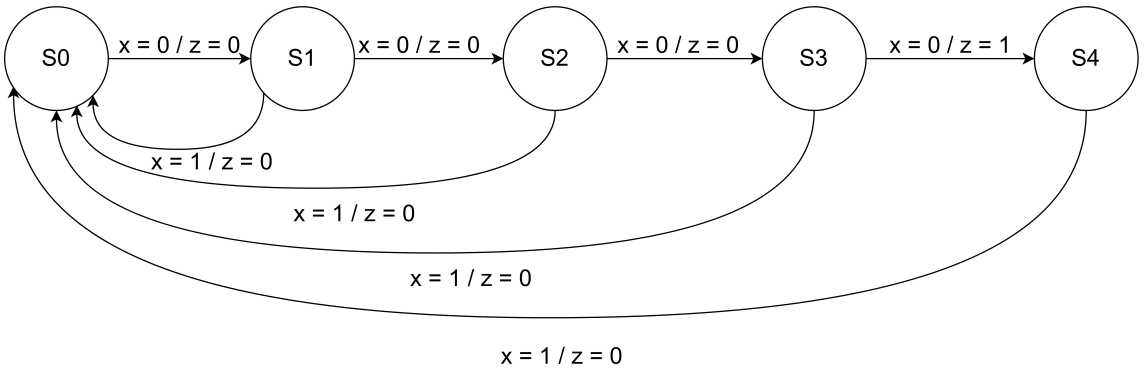

Figure 4: Task 01 State Diagram

Discussion: Given task is a sequential circuit which takes two inputs (w1, w2) and for four clock cycle if the both inputs match then it outputs high on the same clock cycle, which makes it a Mealy type FSM. For exmaple-

w1 : 0 1 1 0 1 1 1 0 0 0 1 1 0
w2 : 1 1 1 0 1 0 1 0 0 0 1 1 1
z : 0 0 0 0 1 0 0 0 0 1 1 1 0

To do this task, at first both the inputs are XOR with each other and as we know from XOR truth table if the input match it will output a zero. So, in the positive clock cycle if the output is zero we go to the next state and if its one revert to the first state. In the if else block we have to check this condition using case statement. If the XOR results (x) zero we change the present state (y) to next state. At the end if its reaches the final state which is S4, then we assign z as high (1). So S0 to S4 in the four clock cycle if the input matches the output will be one otherwise zero.

Task 02:

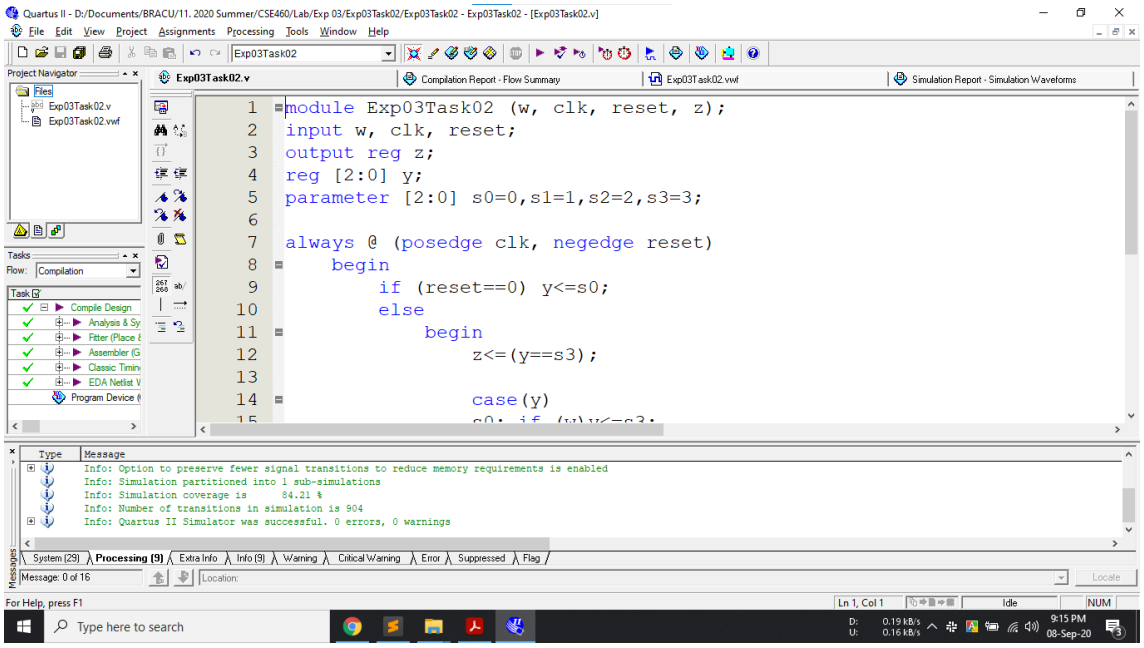

Figure 5: Task 02 Verilog HDL Code [Part 01]

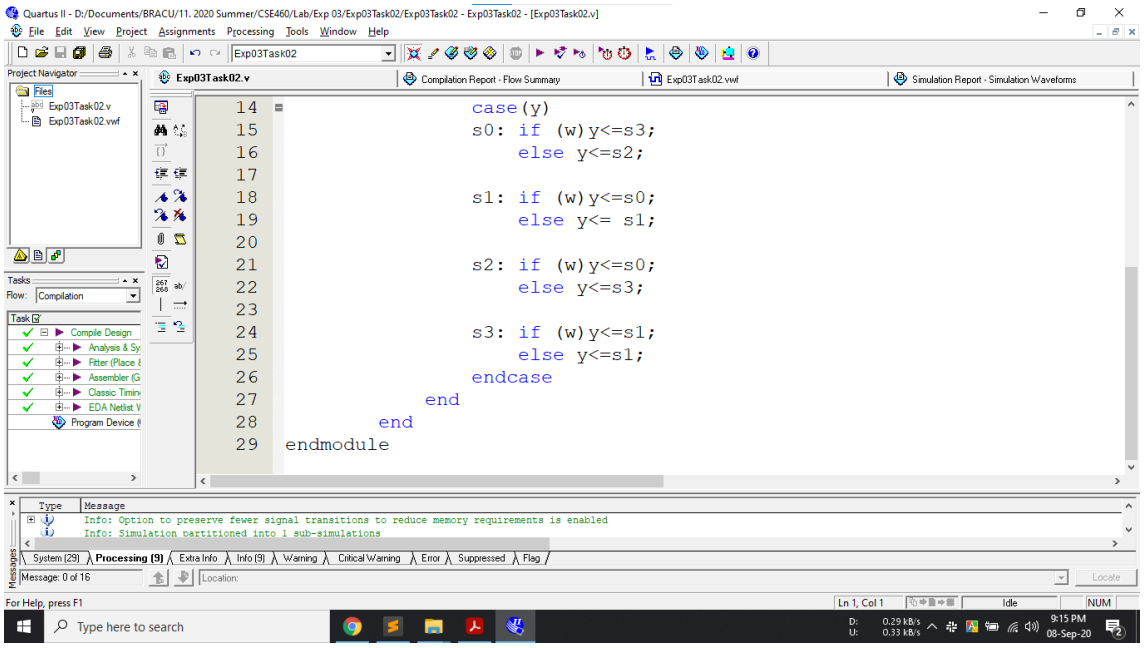

Figure 6: Task 02 Verilog HDL Code [Part 02]

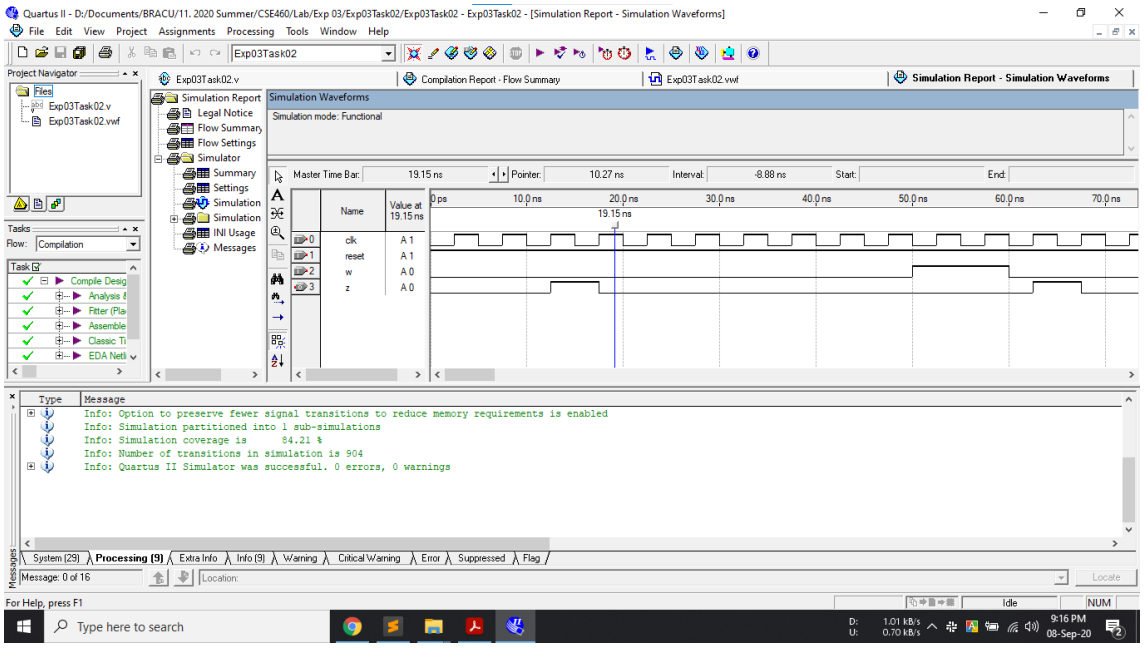

Figure 7: Task 02 Vector Waveform Simulation

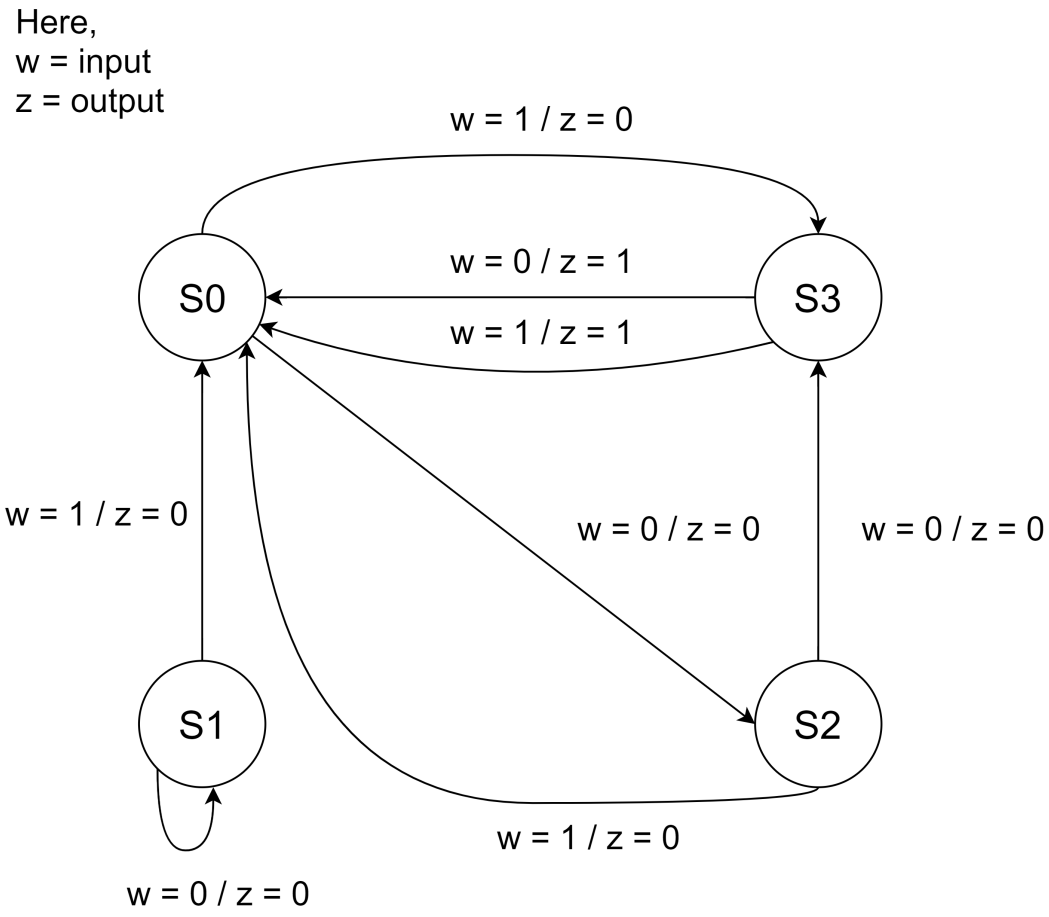

Figure 8: Task 02 State Diagram

Discussion: The task gave an FSM denoted by a state-assigned table and asked implement the system using Verilog HDL code.
In the always block the system works on postive edge clock or resets and negative edge of reset pin. At fist in the if-else we check whether its reset 0 or not otherwise we proceed with the state table. According to table the system outputs high when it reaches state S3. So, we output (z) to high if the present state is S3. If not we forward using case and check the states accordingly. And based on the input (w) we change the present state (y) values.