Brac University

EEE 412/ ECE 412/ CSE 460

VLSI Design Laboratory

Experiment Title: Designing layout of basic logic gates and combinational circuits using microwind.

Theory:

Integrated circuit layout, also known IC layout, IC mask layout, or mask design, is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. Layout design is how each component in an integrated circuit is fabricated in a chip. There are some basic rules that need to be followed while designing layout. Design rules are based on MOSIS rules. The main term of MOSIS rules is parameter λ.

There is several levels of design rules:

- well rules;
- transistor rules;
- contact rules;
- metal rules;
- via rules;

Well rules:

N-well is deeper mounted than any other transistor implants. Clearance between n-well edges and n+ diffusion should be good enough. This clearance is usually determined by the oxide transition time across the well boundary. The other rule is grounding n-well, providing sufficient number of well taps. This will prevent significant voltage drops due to well current.

Transistor rules:

Transistor is designed with at least for masks:

- Active mask – defines where p- or n-diffusion type or gates will be placed;
- n-implant mask – defines areas where n-type diffusion is required; n-type diffusion in p-wells define nMOS transistors; p-type diffusion in n-wells defines pMOS transistors;
- p-implant mask – defines where p-type diffusion is required; p-type diffusion in n-wells define n-type contacts.; p-type diffusion in p-wells define p-well contacts
- polysilicon mask – crossing of polysilicon and diffusion mask defines the gates of transistor. Polysilicon mask should cover active mask and extend beyond that area, otherwise transistor will be shorted with the diffusion path between source and drain. Crossing of polisilicon and active mask create gate of transistors. Polysilicon and active masks that does not form a transistor should be kept separately.

Contacts rules:

Types of contacts:

- metal to p-active (p-diffusion)

- metal to n-active (n-diffusion)
- metal to polysilicon
- metal to well or substrate

Metal rules:

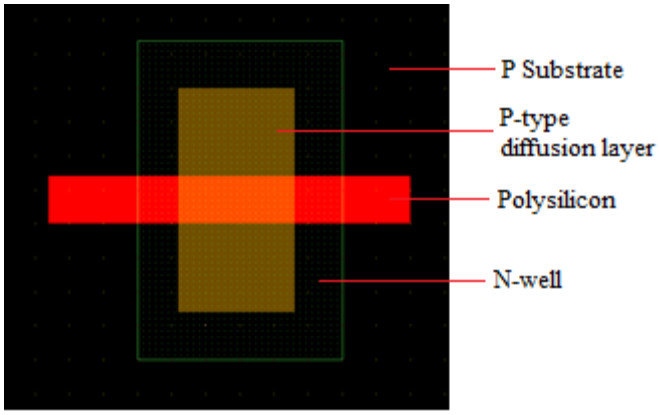
Metal spacing can be different depending on the metal line. But there is certain width applied to small and thick wires. So if there is a need of wider wires, they can be made of several small wires connected together. Spacing rules can be applied to a long parallel wires.

Via (vertical interconnect access) rules:

Modern planar technology allows stacked vias.

Example: Designing a CMOS inverter.

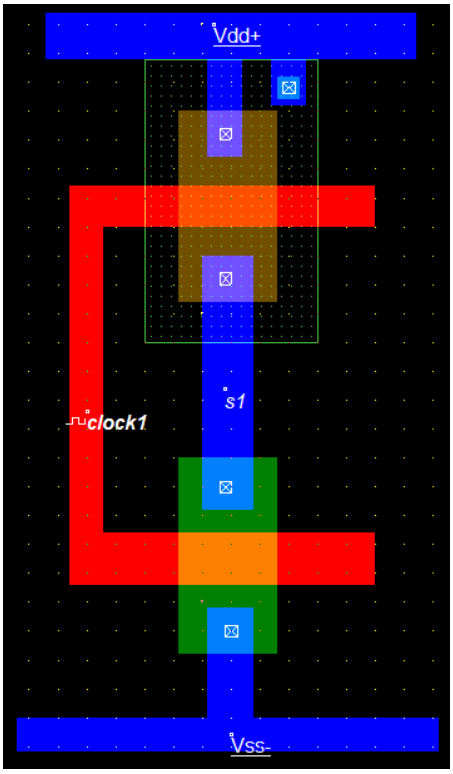
The background of microwind is a p-type substrate. As the drains and sources of p-channel MOSFET are supposed to be n-type and the substrate is supposed to be n-type, we develop an n-well at first where we will place the p-type diffusion layer. We then draw a rectangular diffusion layer inside the n-well and separate the diffusion layer into two halves using polysilicon layer which will act as the gate. The polysilicon layer automatically creates the channel region.

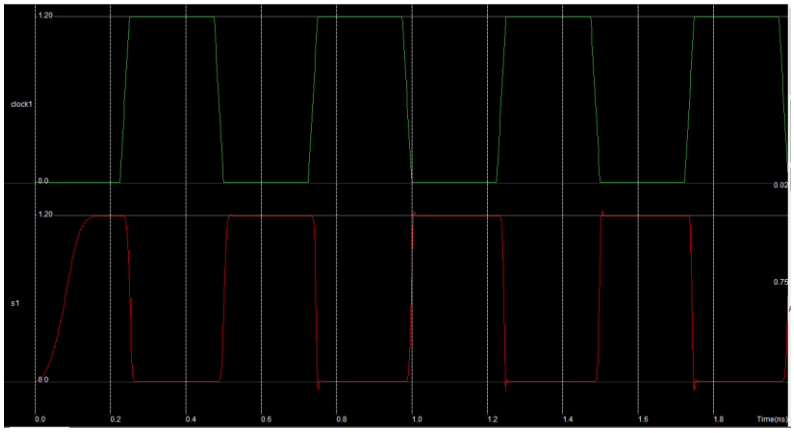


We similarly design the nMOS where we only require the n-type diffusion layer and polysilicon. P-well is not required as the substrate itself is p-type. We connect the two polysilicon gates with polysilicon layer.

Now, polysilicon divides the FET into two parts and since MOSFET are symmetric device, we can consider any one of them as drain and other as source. We then connect the drain of pMOS with the drain of nMOS using metal. Since the drains are diffusion layers, connecting them to metals will require contacts (metal to p-diffusion and metal to n-diffusion respectively). We require contacts whenever we want to connect two different layers.

We then connect the source of pMOS to a metal power line and source of nMOS to metal ground line. We connect VDD and VSS to the power lines. We also connect power to the n-well to bias the n-well. We connect a clock to the polysilicon as input and visible node to metal connecting pMOS with nMOS for observing the output.

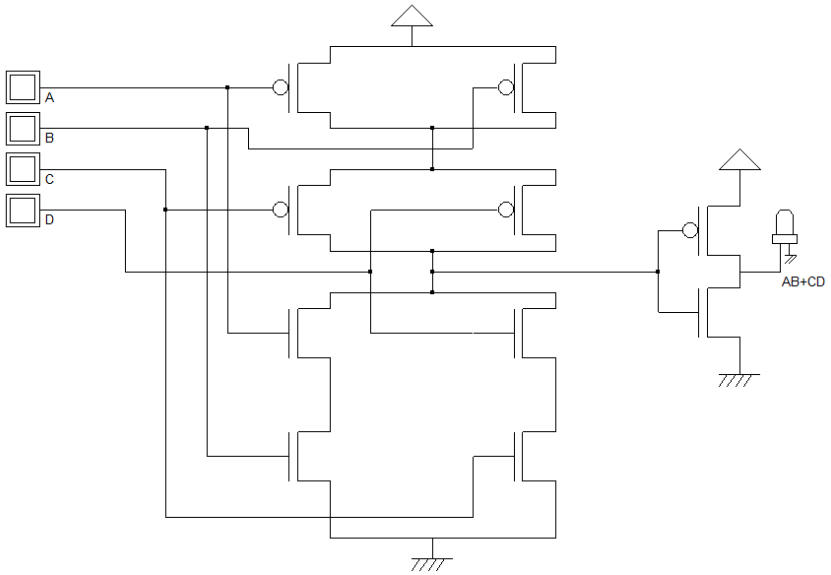




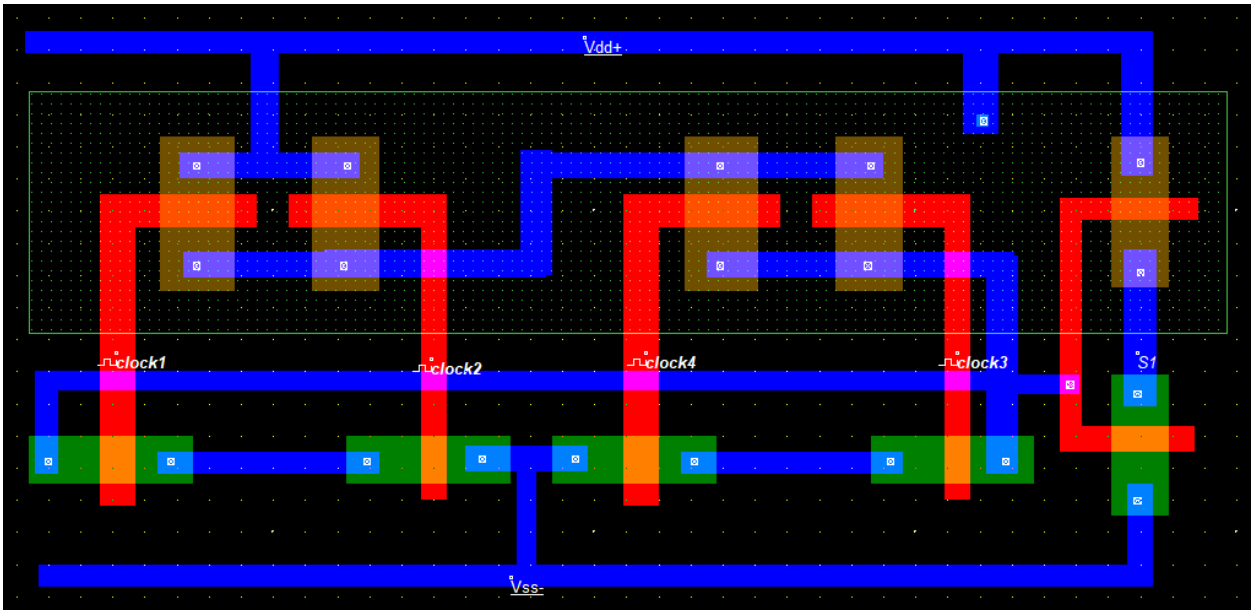
We then click the DRC check option. If there is no error, we press simulation option to check whether the input output relations are as expected.

Example 2: Design the layout of combinational circuit that gives output F=AB+CD

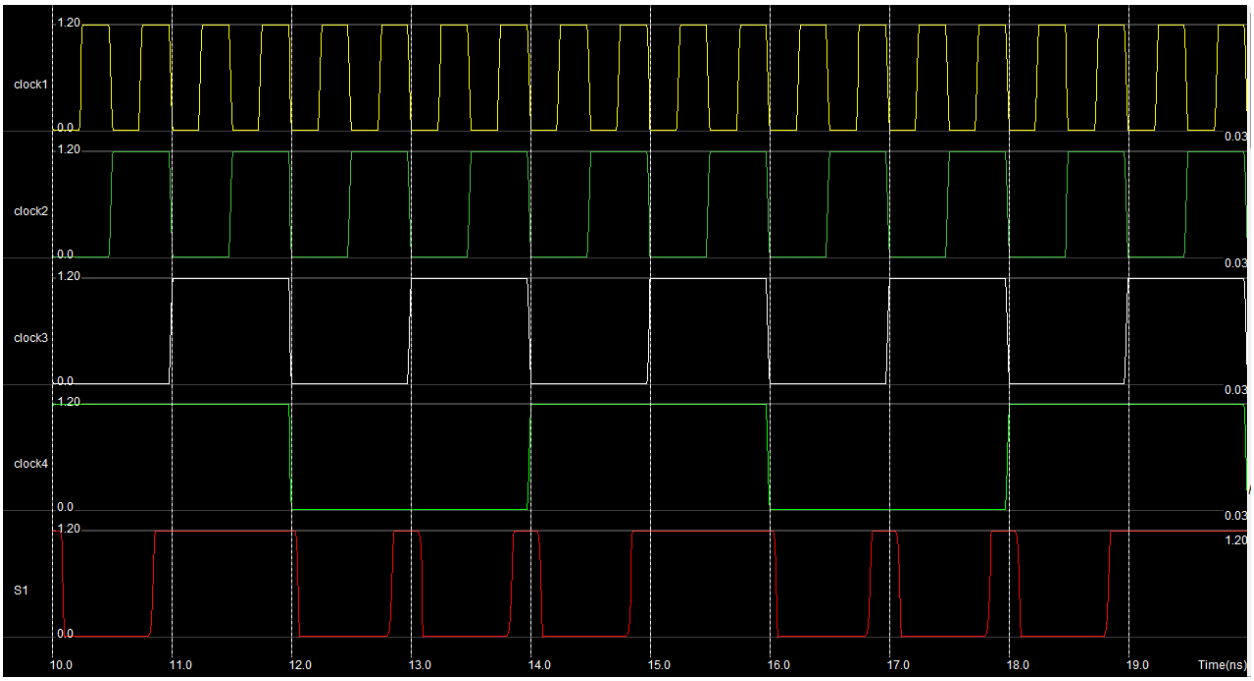
The CMOS implementation of the function is as follows:



The layout may look like the following:



The input output relations is as follows:



Homework:

1. Design the layout of AND, OR and XOR gates using CMOS.

2. Design the layout of 2 to 1 MUX using CMOS.

3. Design the layout of the combinational circuits that gives f=(A+B)C