Brac University

EEE 412/ ECE 412/ CSE 460

VLSI Design Laboratory

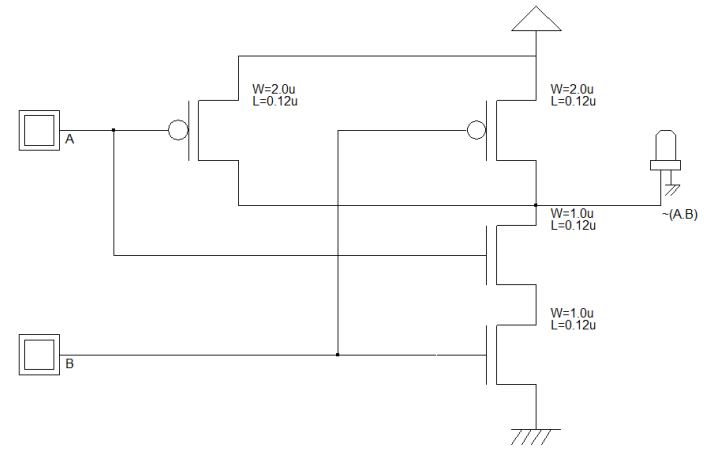
Experiment Title: Optimizing area requirements of CMOS Circuits in analog layout design and digital layout synthesis from structural Verilog using microwind.

Theory:

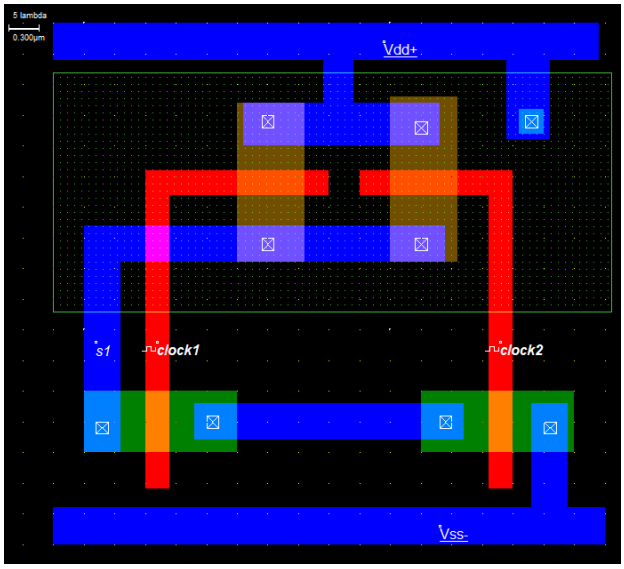
Area optimization is key necessity in VLSI design and with that view, layouts are such designed that two or more FETs share their source/drain in CMOS circuit configuration decreasing the overall area requirement of circuit. While area optimization, we must note that FETs are symmetric device and thus any diffusion region can be chosen as source or drain at any time as required.

Example: Design the layout of a 2 input nand gate.

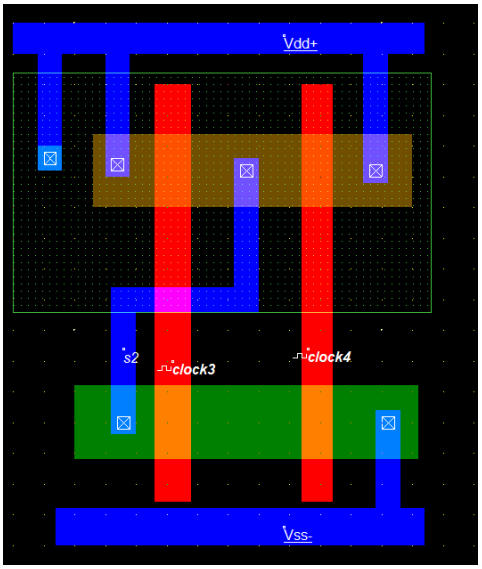
The schematic of the 2 input NAND gate looks as follows:



The circuit with and without area optimization will look as follows:

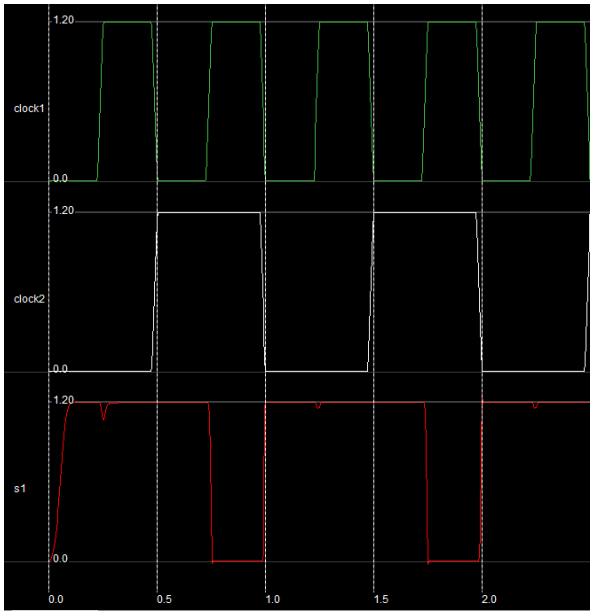


Not optimized

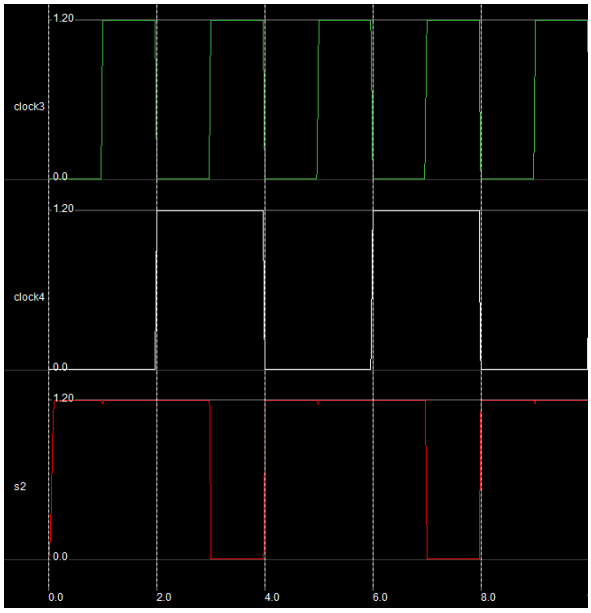


Area Optimized

The waveshapes will look as follows:



Not Optimized



Area Optimized

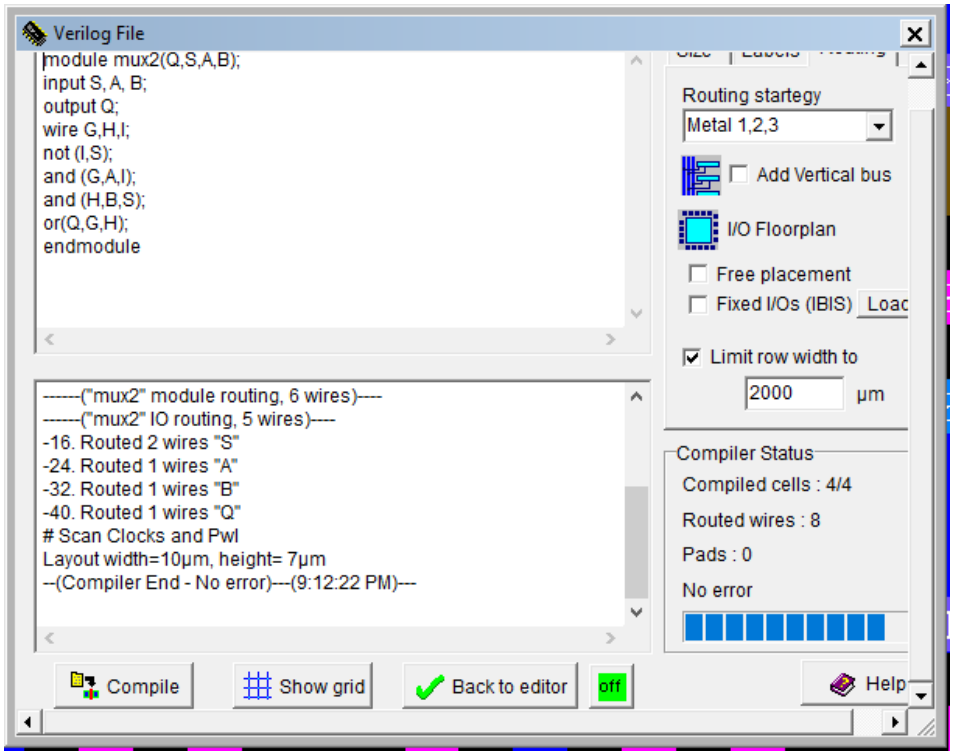
Layout can be synthesized using structural Verilog code. For this, we need to write a Verilog code, define all the variables other than input and output as wire and save it in a file. Suppose we want to design a 2 to 1 MUX. We write the following code:

```
module mux2(Q,S,A,B);
input S, A, B;
output Q;
wire G,H,I;
not (I,S);
and (G,A,I);
and (H,B,S);
or(Q,G,H);
endmodule
```

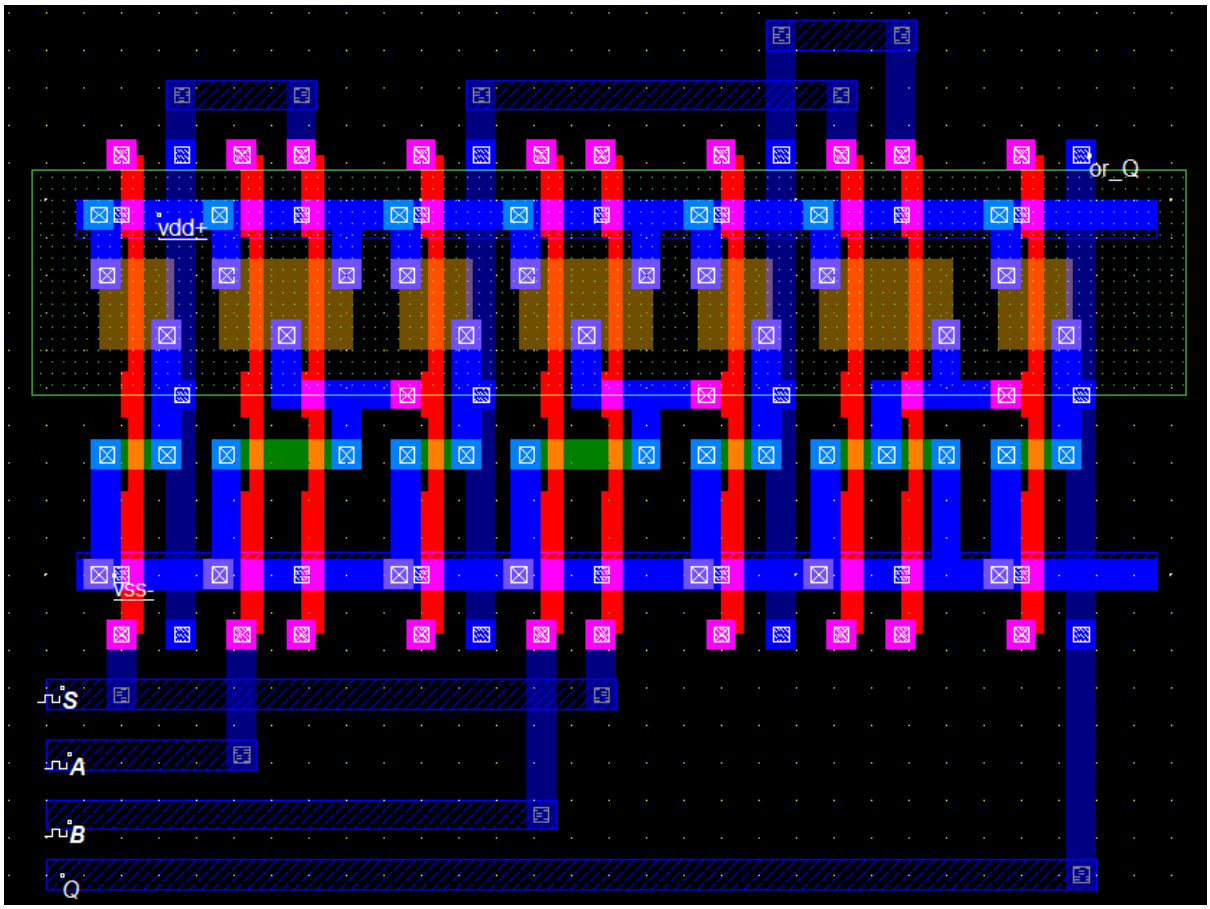
Now, in microwind, click Compile->Compile Verilog file from menu bar. Select the Verilog code file. Press compile in the dialogue box that appears.

You can observe layout being automatically generated in the background.

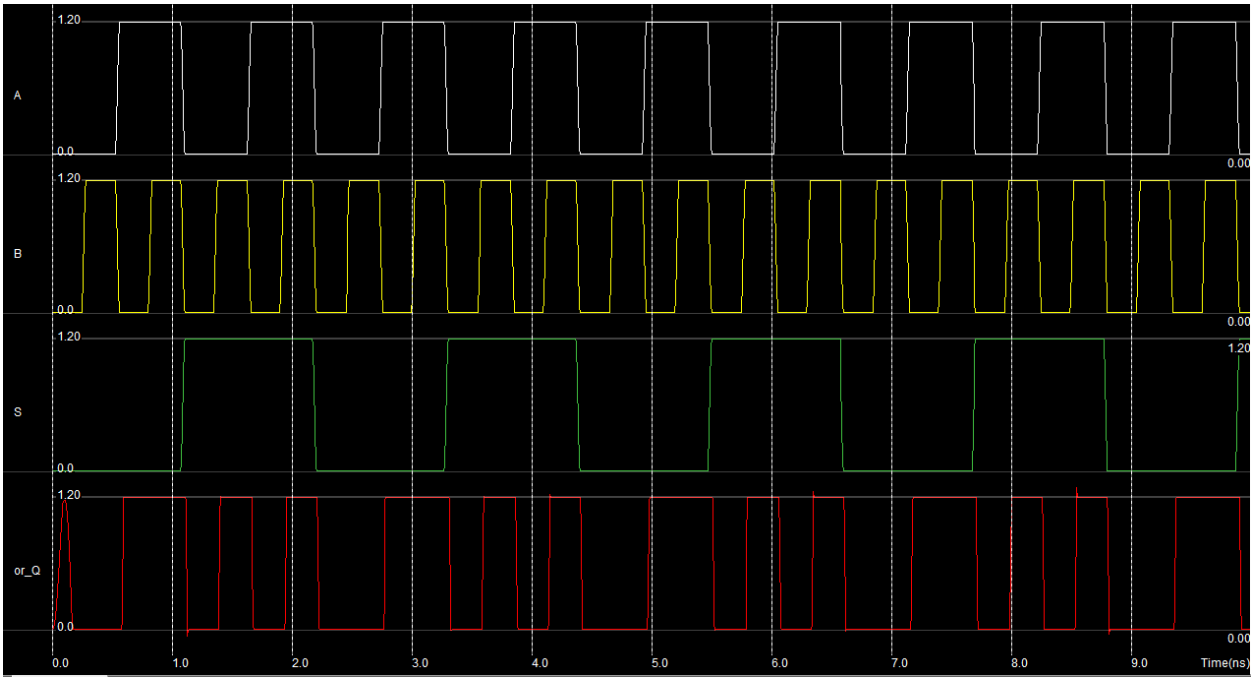
Once the dialog box shows “No Errors”, close the dialog box. Then press “run” in microwind.



The layout looks as follows:



And the timing diagram looks as follows:



Homework:

1. Design the layout of 3 input AND and OR gates with optimized area.

2. Design the layout of 4 to 1 MUX and priority encoder (3>2>0>1) using Verilog.

3. Design the layout of the combinational circuits that gives f=AB+CD optimizing the area.