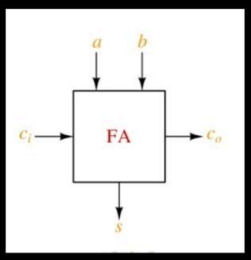
EE635
Digital IC Design

Course Project Report

Group 8 - Jatin, Harshith, Mehak, Ruthwik

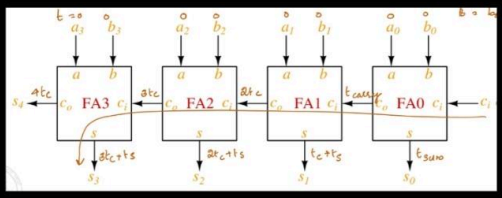
Basic Theory of Full Adder :

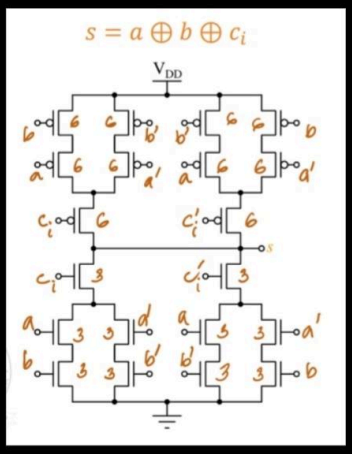


Sum $S = a \oplus b \oplus c_i$

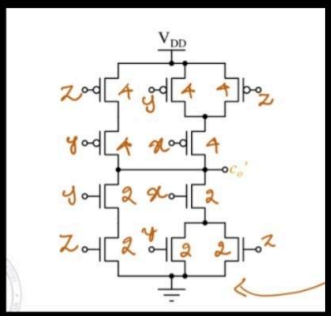
carry $c_o = ab + bc_i + c_i a$

4-Bit Adder as discussed in class :



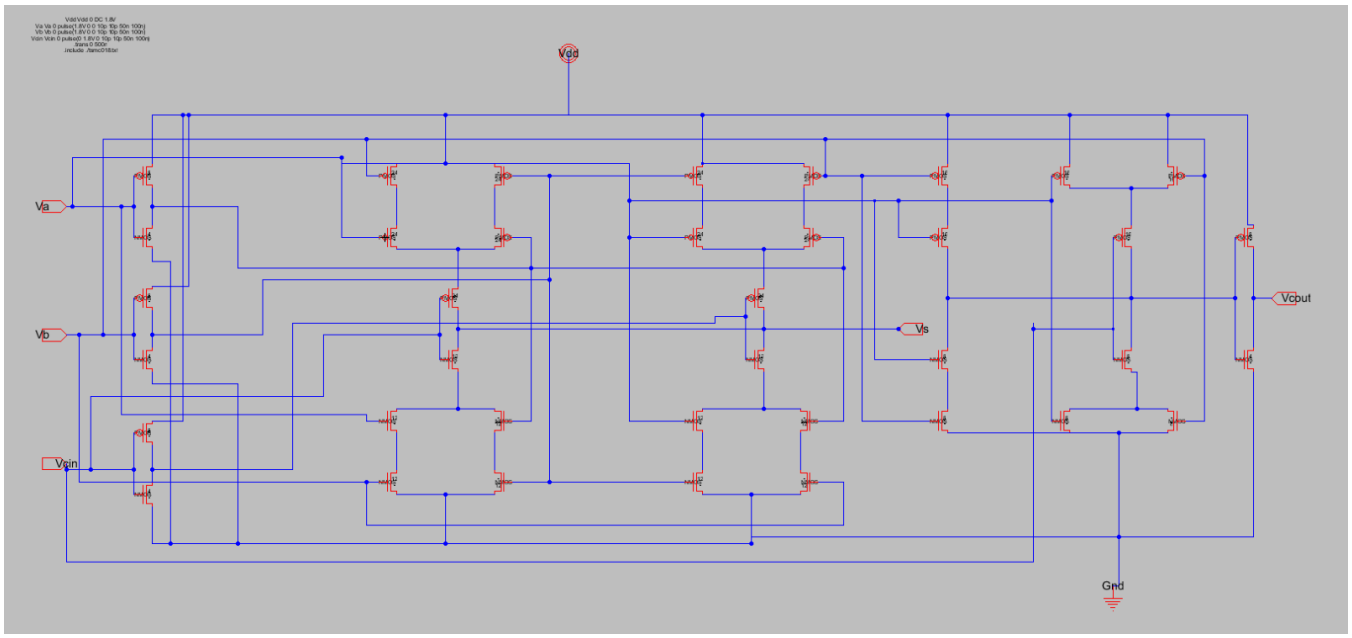


Sum implementation



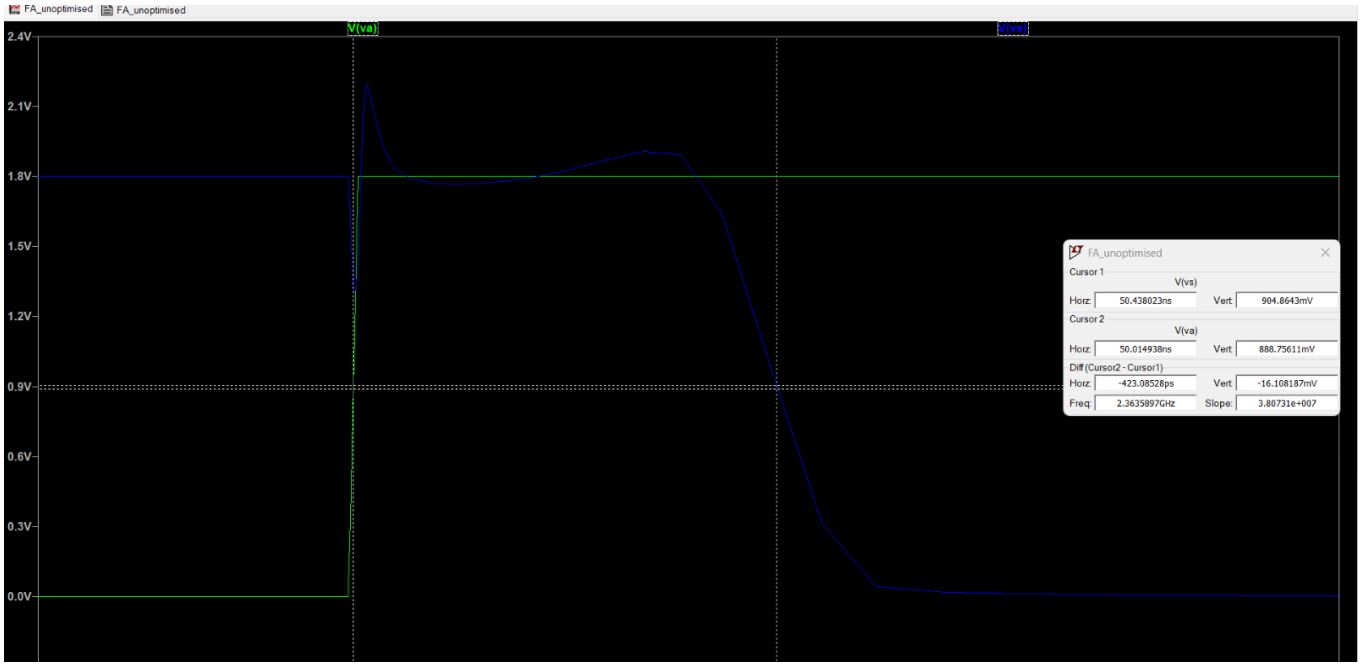
C_o implementation

Un-Optimised Full Adder Schematic (As discussed in class) :

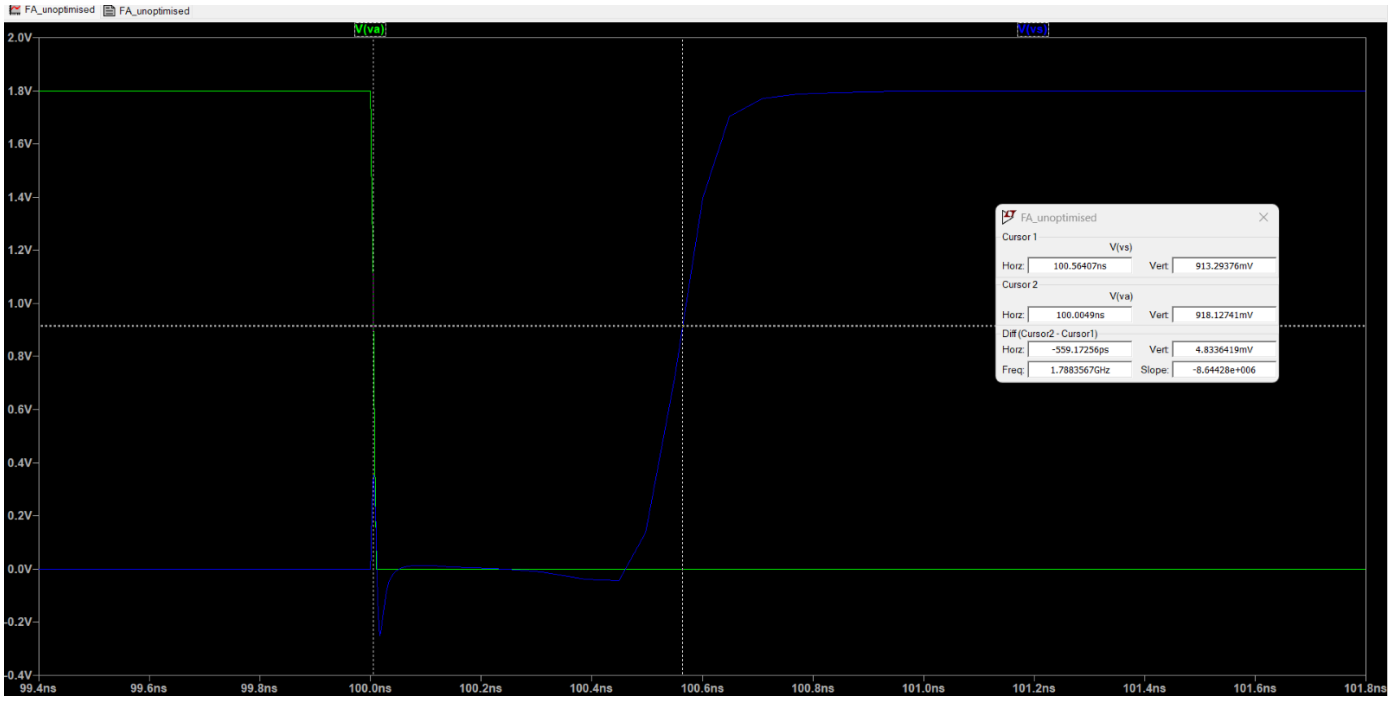


Propagation Delays of Un-Optimised Full Adder :

Case 1 : A,B = 1 → 0 (High to Low), Cin = 0 → 1 (Low to high)

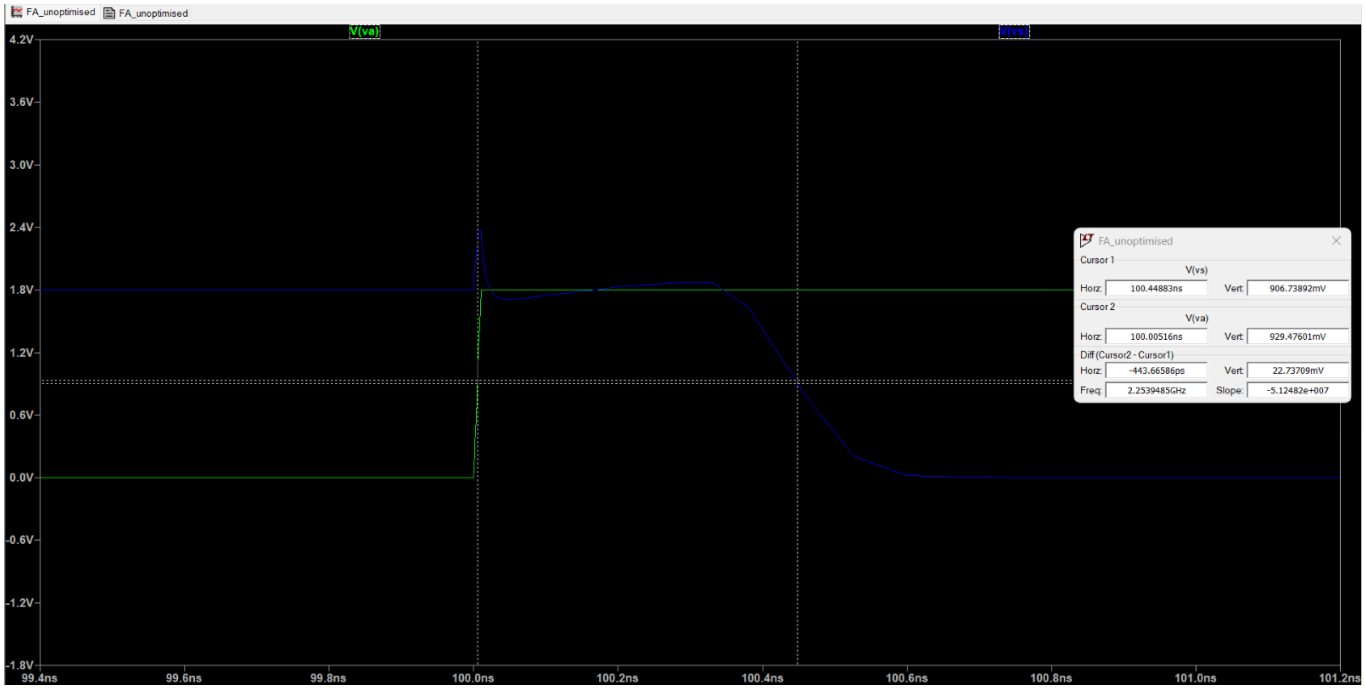


tpHL = 423.08 ps

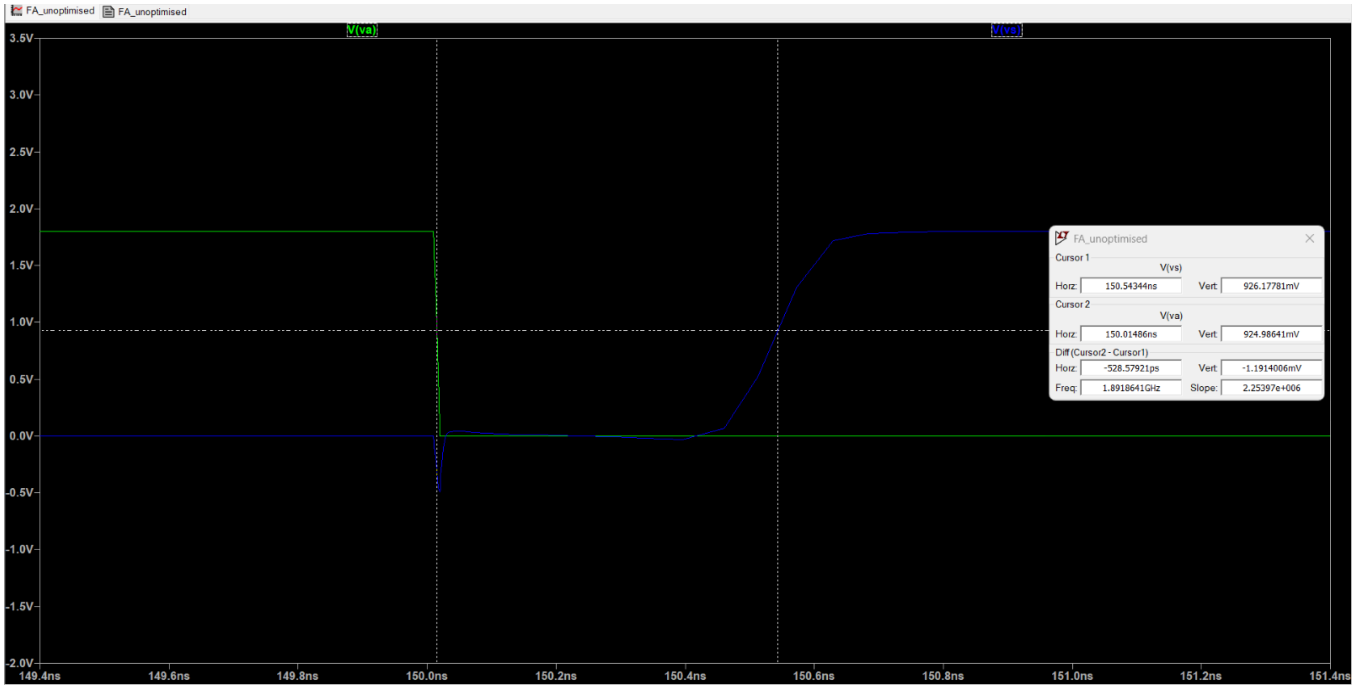


tpLH = 559.17 ps

Case 2 : A = 0 → 1 (Low to High) ,B = 1 → 0 (High to Low), Cin = 0 → 1 (Low to high)

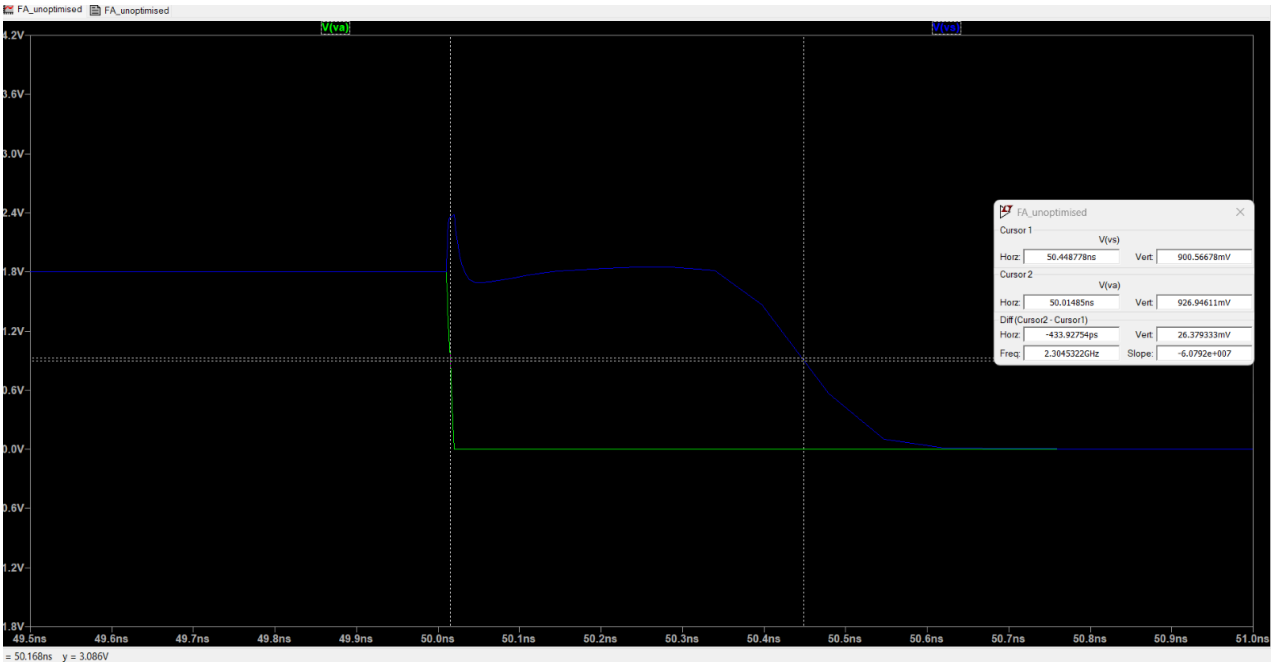


tpHL = 443.66 ps

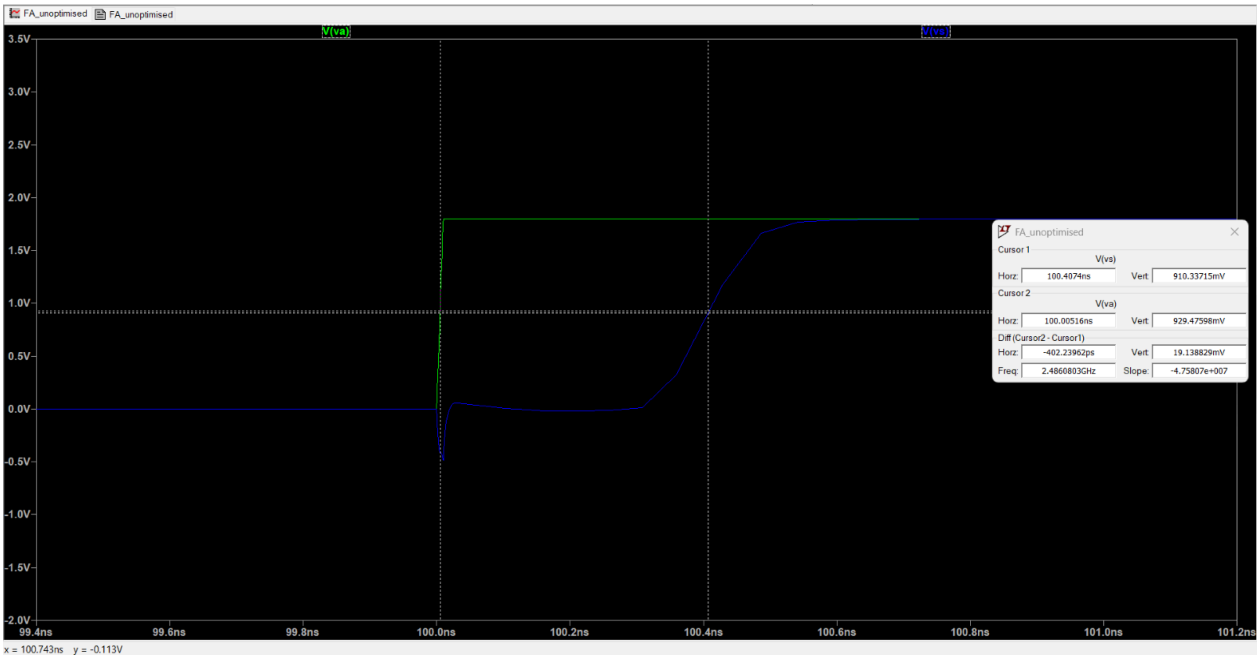


tpLH = 528.57 ps

Case 3 : A = 0 → 1 (Low to High) ,B = 1 → 0 (High to Low), Cin = 1 → 0 (High to Low)



tpHL = 433.92 ps



tpLH = 402.23 ps

Overall Propagation Delays in Tabulated Form for the Un-Optimised Full Adder :

	tpHL	tpLH	tp = (tpHL + tpLH) / 2
A,B = 1→ 0, C = 0→ 1	423.08 ps	559.17 ps	491.12 ps
A,C = 0→ 1, B = 1→ 0	443.66 ps	528.57 ps	486.115 ps
A = 0→ 1, B, C = 1→ 0	433.92 ps	402.23 ps	418.07 ps

Optimisation Idea and Technique :

Optimisation Idea and Technique :

a	b	c_i	s	c_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \Sigma m(1,2,4,7)$

$\overline{S} = \Sigma m(0,3,5,6)$

$C_o = \Sigma m(3,5,6,7)$

$\overline{C_o} = \Sigma m(0,1,2,4)$

$\therefore$ S and C_o can be implemented using mirror logic

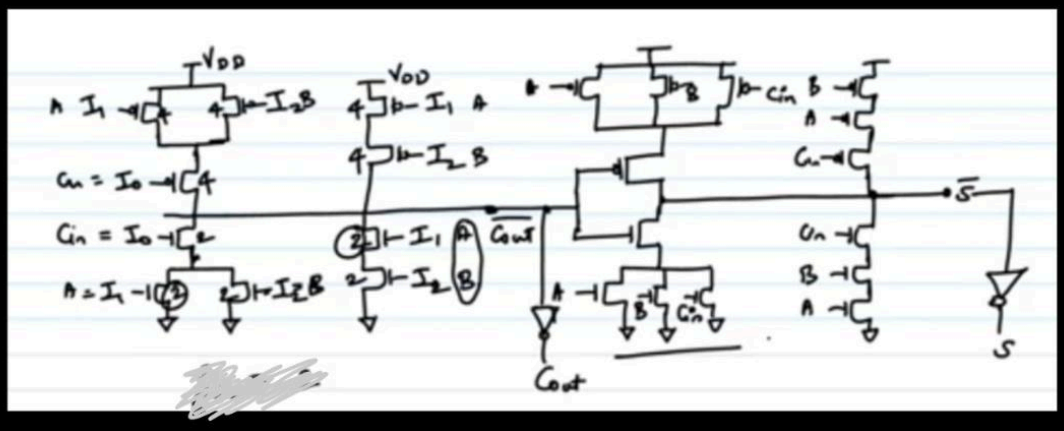
$C_{out} = AB + BC_{in} + C_{in}A$

$S = A \oplus B \oplus C_{in}$

$= A(\overline{B \oplus C_{in}}) + \overline{A}(B \oplus C_{in})$

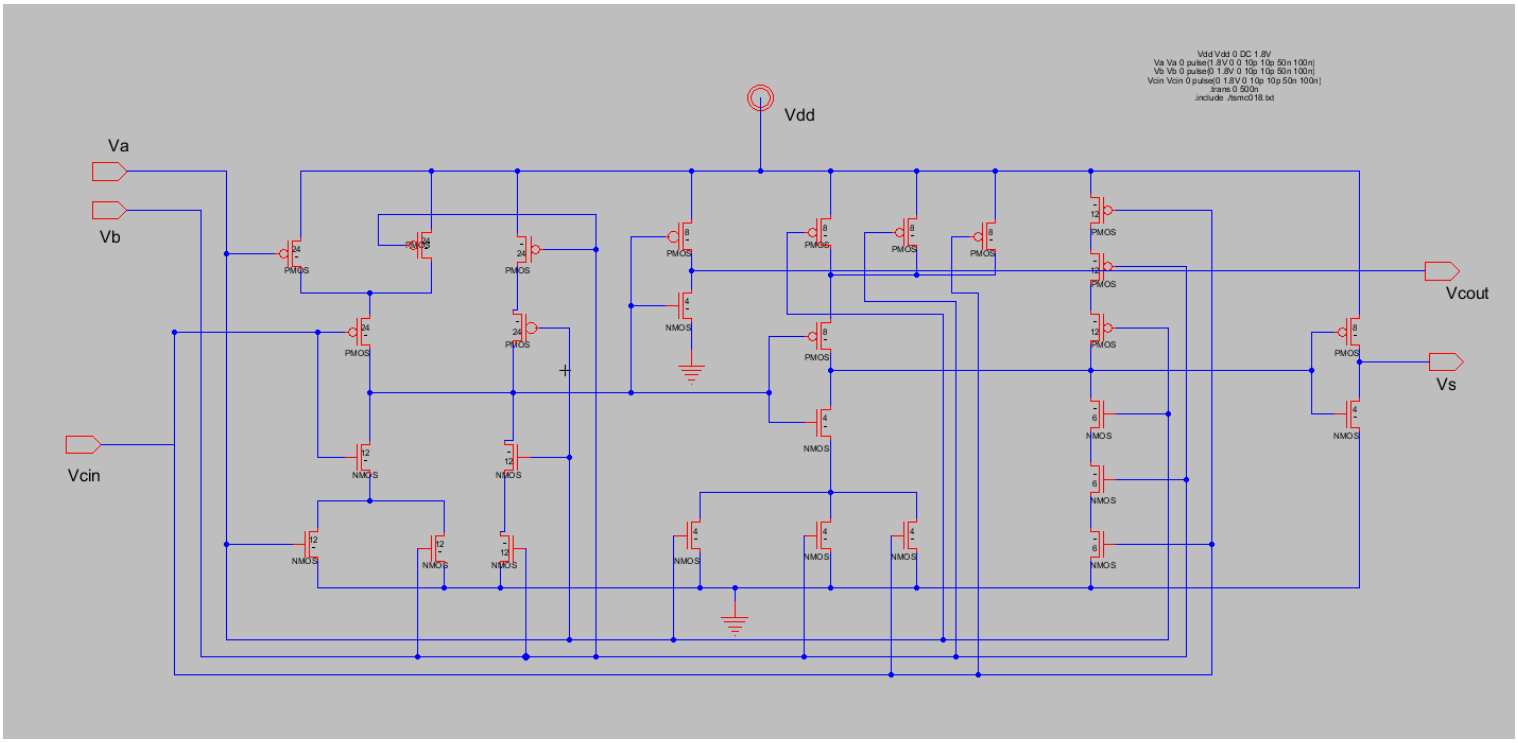
$= A(BC_{in} + \overline{B}\,\overline{C_{in}}) + \overline{A}(B\overline{C_{in}} + \overline{B}C_{in})$

$\therefore S = ABC_{in} + \overline{C_o}(A+B+C_{in})$



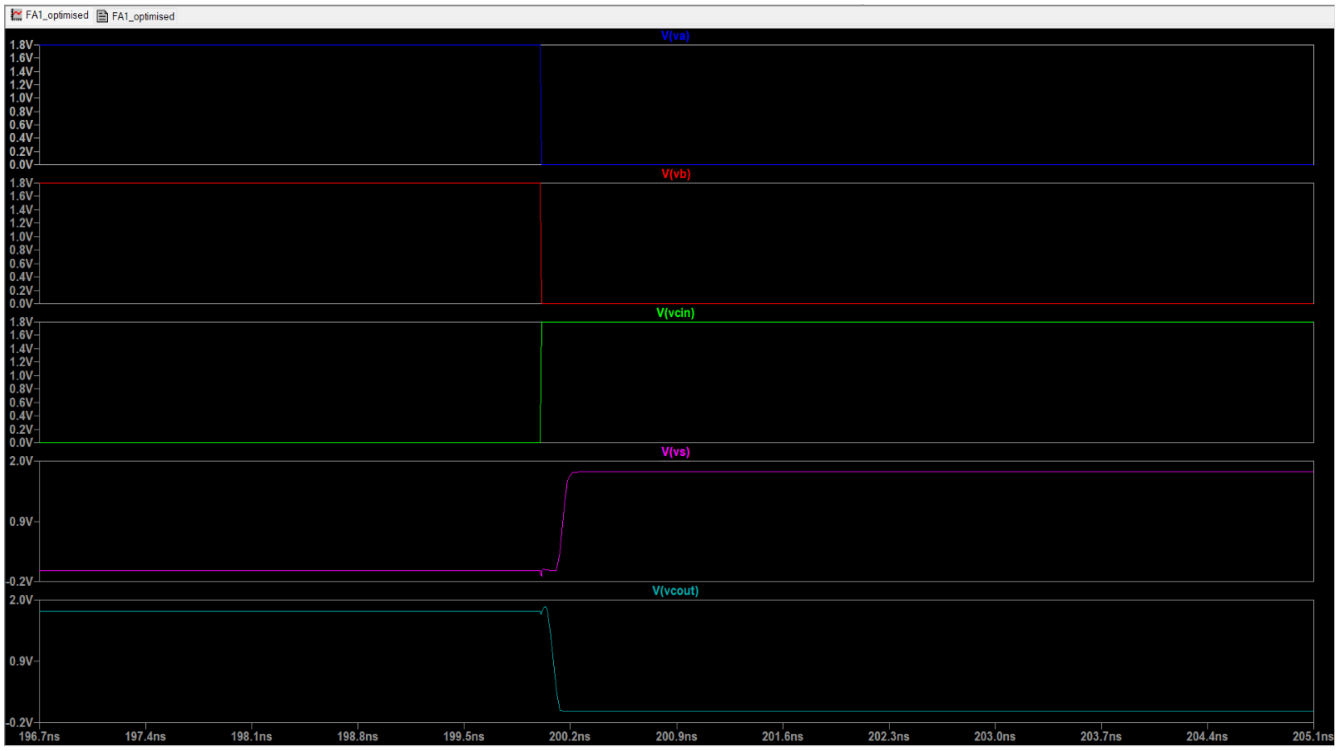
Q2. A) Optimize the full adder given in 1(a) using more efficient topologies than what is discussed in the class. Construct the VTC and find out the propagation delays (both pre- and post-layout levels) of the circuit assuming that all inputs transition simultaneously.

Optimised Full Adder Schematic :

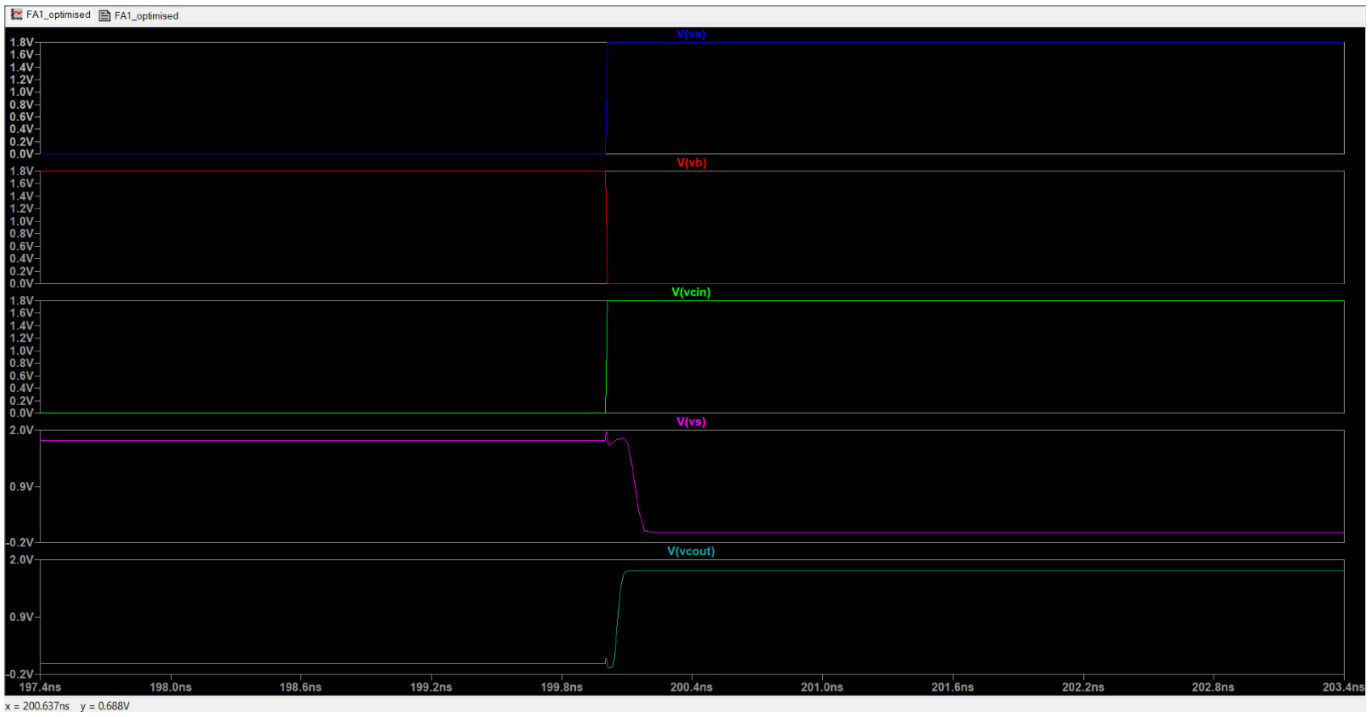


Output Waveforms of Optimised Full Adder using Schematic Simulations :

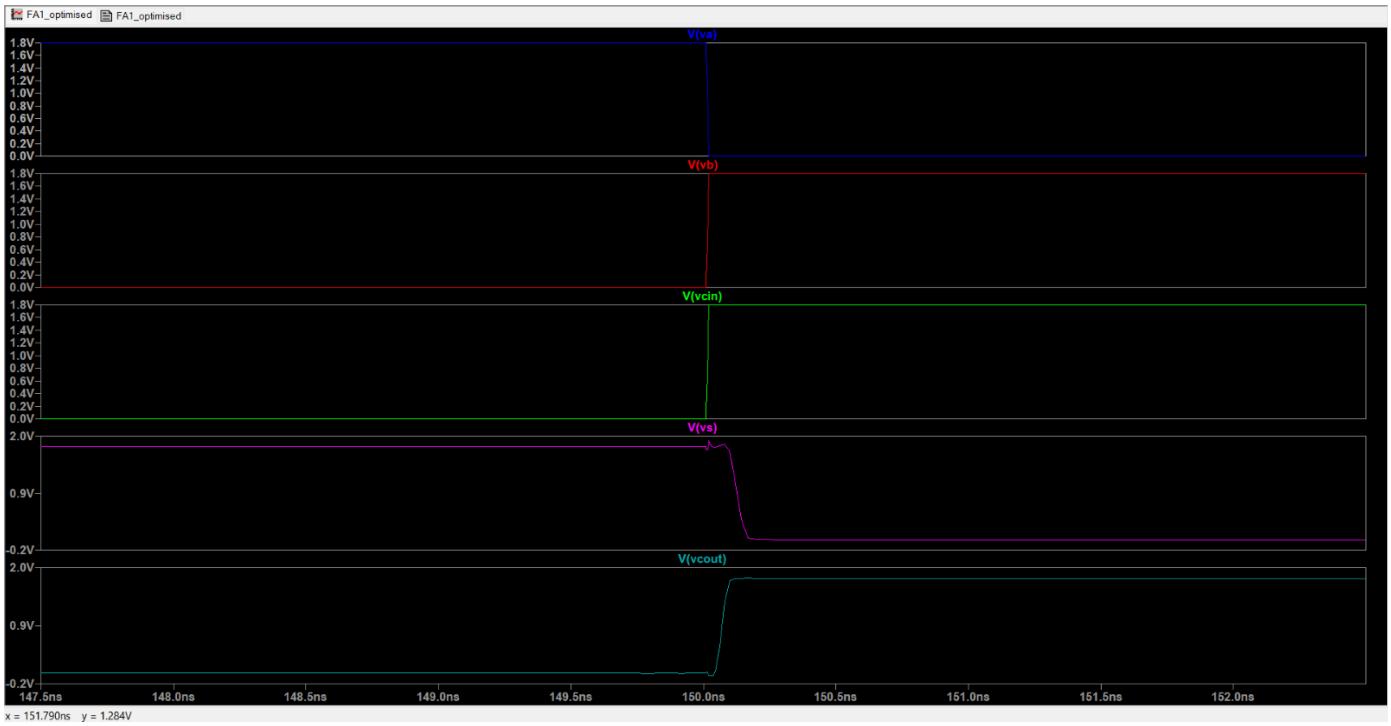
Case 1 : A,B = 1 → 0 (High to Low), Cin = 0 → 1 (Low to high)



Case 2 : A = 0 → 1 (Low to High) ,B = 1 → 0 (High to Low), Cin = 0 → 1 (Low to high)

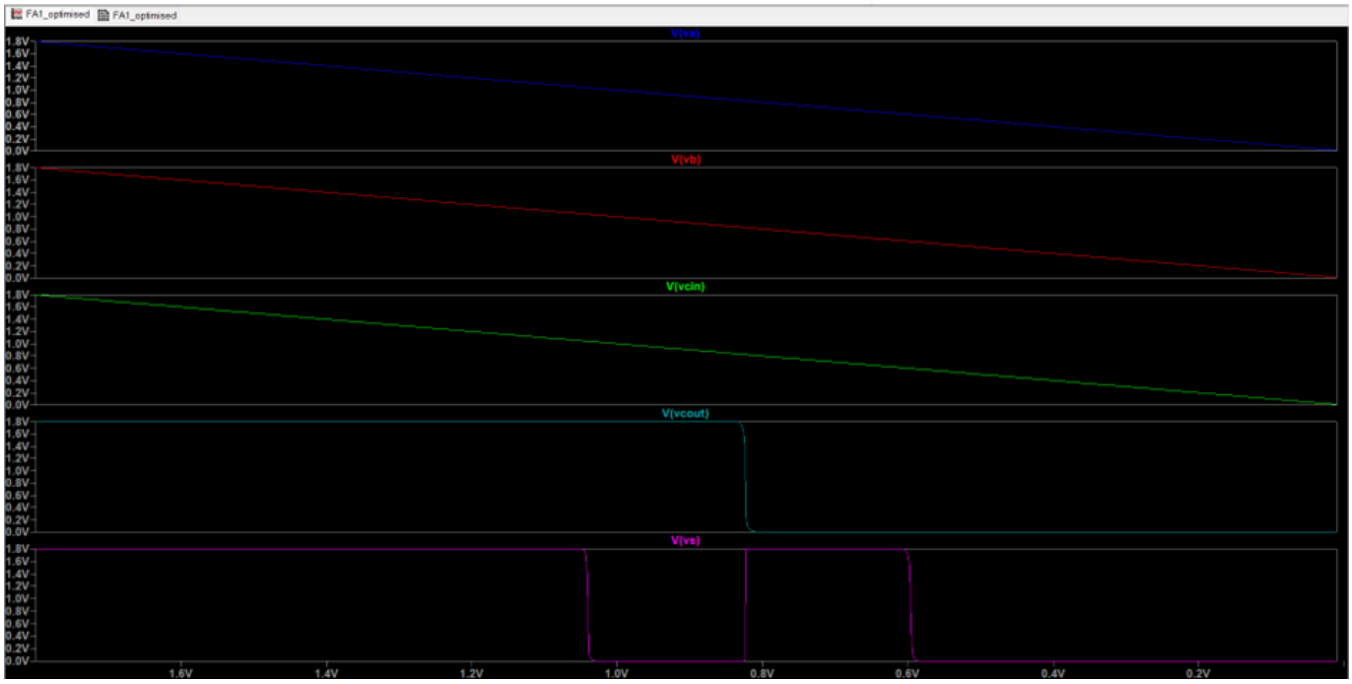


Case 3 : A = 0 → 1 (Low to High) ,B = 1 → 0 (High to Low), Cin = 1 → 0 (High to Low)

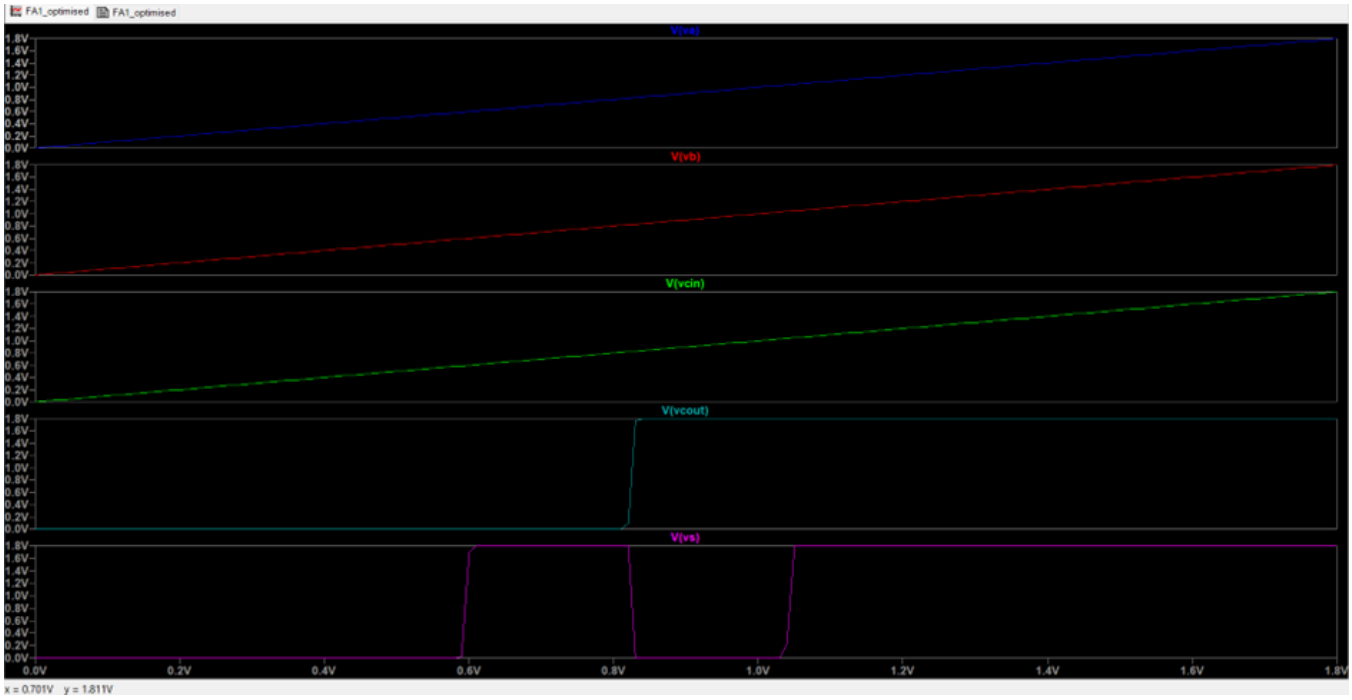


VTC of Optimised Full Adder using Schematic Simulations :

Case 1 : A,B,Cin = 1 → 0 (High to Low)

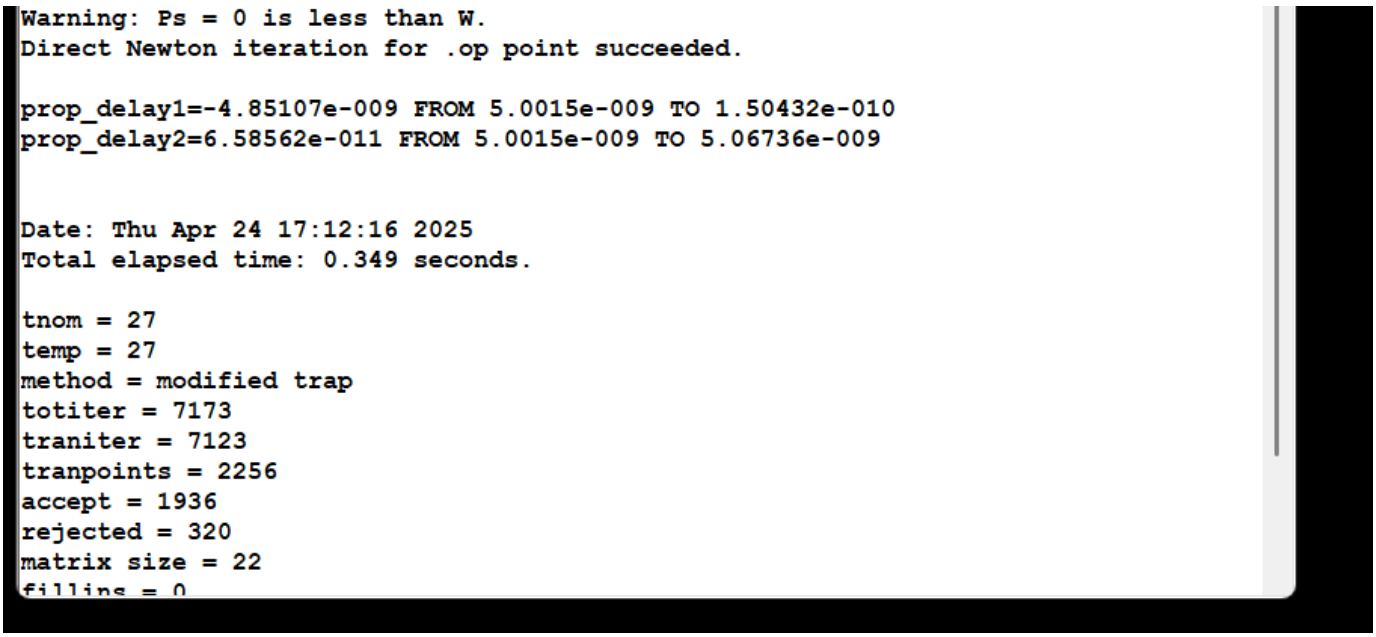


Case 2 : A,B, = 0 → 1 (Low to High)



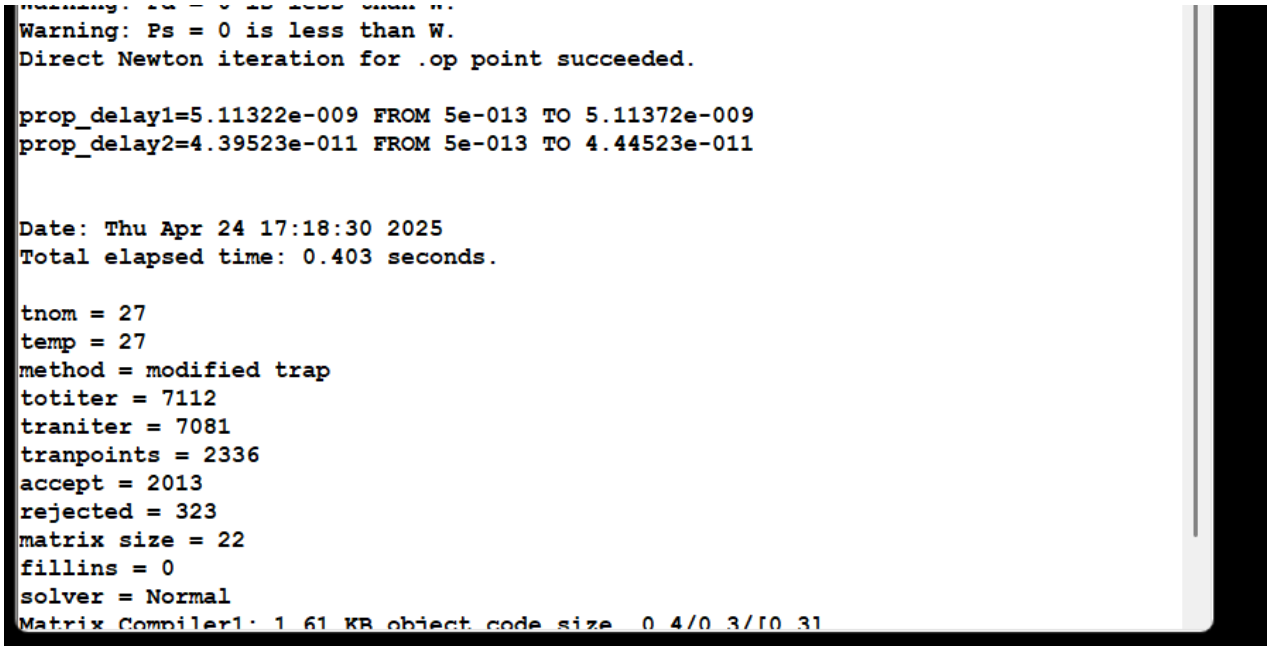
Propagation Delays of Optimised Full Adder using Schematic Simulations :

Case 1 : A,B = 1 → 0 (High to Low), Cin = 0 → 1 (Low to high)



Propagation Delay : 65.85 ps

Case 2 : A = 0 → 1 (Low to High) ,B = 1 → 0 (High to Low), Cin = 0 → 1 (Low to high)



Propagation Delay : 43.95 ps

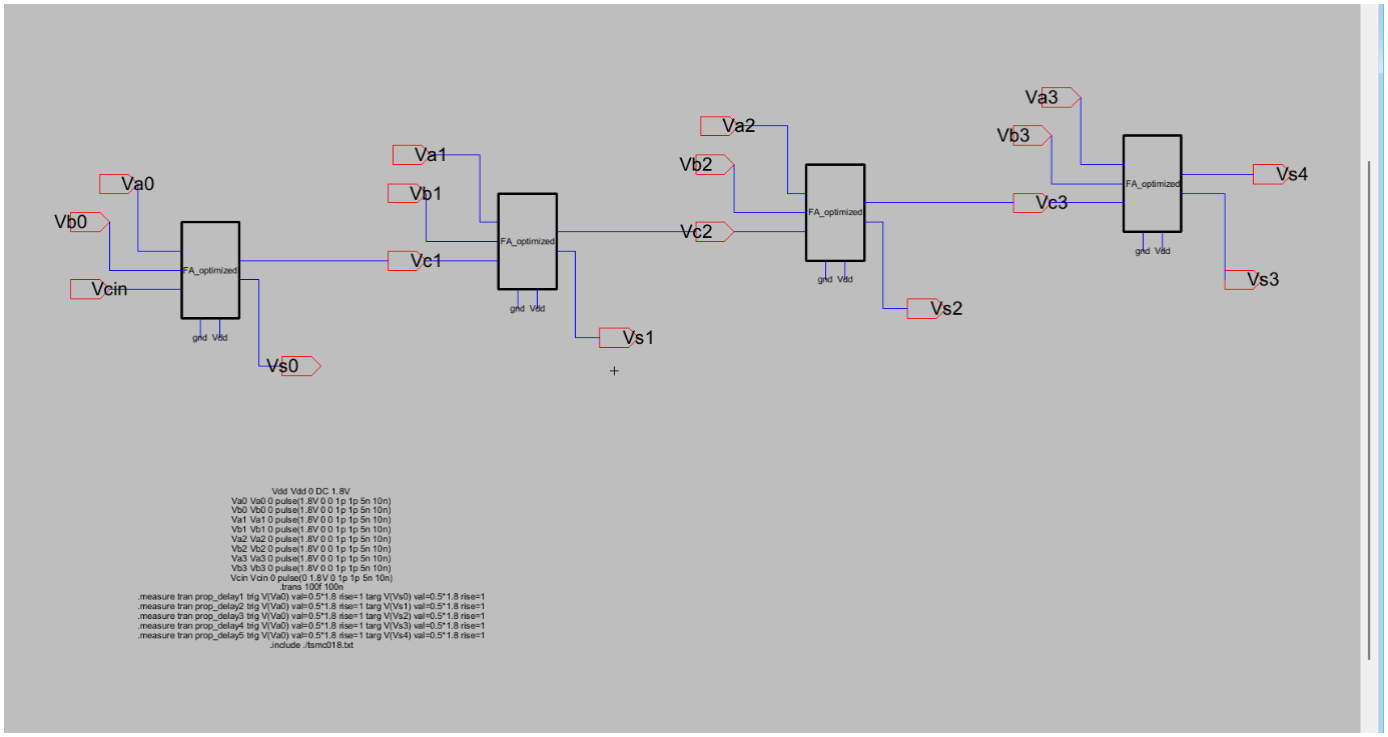
Case 3 : A = 0 → 1 (Low to High) ,B = 1 → 0 (High to Low), Cin = 1 → 0 (High to Low)

```
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

prop_delay1=4.48429e-011 FROM 5e-013 TO 4.53429e-011
prop_delay2=3.23986e-011 FROM 5e-013 TO 3.28986e-011


Date: Thu Apr 24 17:20:07 2025
Total elapsed time: 0.330 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 7087
traniter = 7063
tranpoints = 2280
accept = 1988
rejected = 292
matrix size = 22
fillins = 0
solver = Normal
Thread vector: 19.5/11.5[2] 2.1/2.0[1] 0.8/0.9[1] 0.1/0.7[1]  2592/500
Matrix Compiler1: 1.61 KB object code size  0.3/0.1/[0.1]
```

Propagation Delay : 32.39 ps

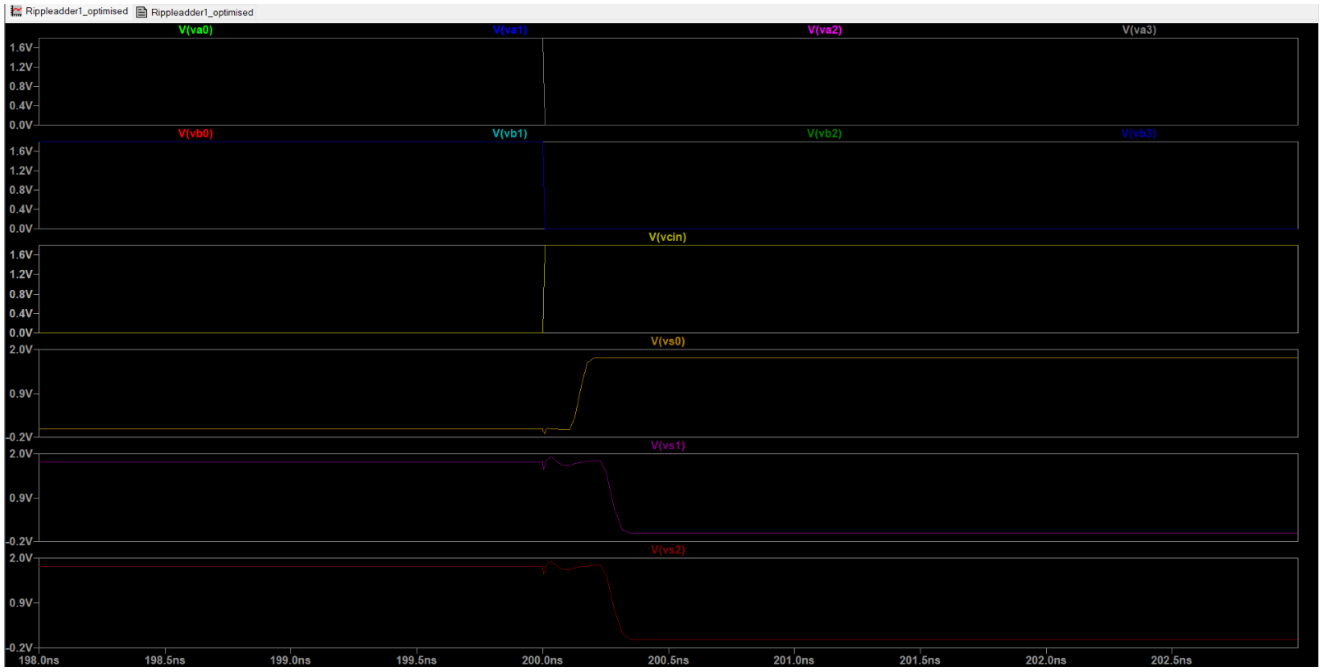
Q2.B) Build an optimized 4-bit adder using the full adder above with or without using additional logic. Demonstrate the functionality through waveforms for 2-3 different input combinations. Estimate the critical path delay through simulations.

Optimised Four-Bit Adder Schematic (by repeating optimised Full Adder Blocks) :

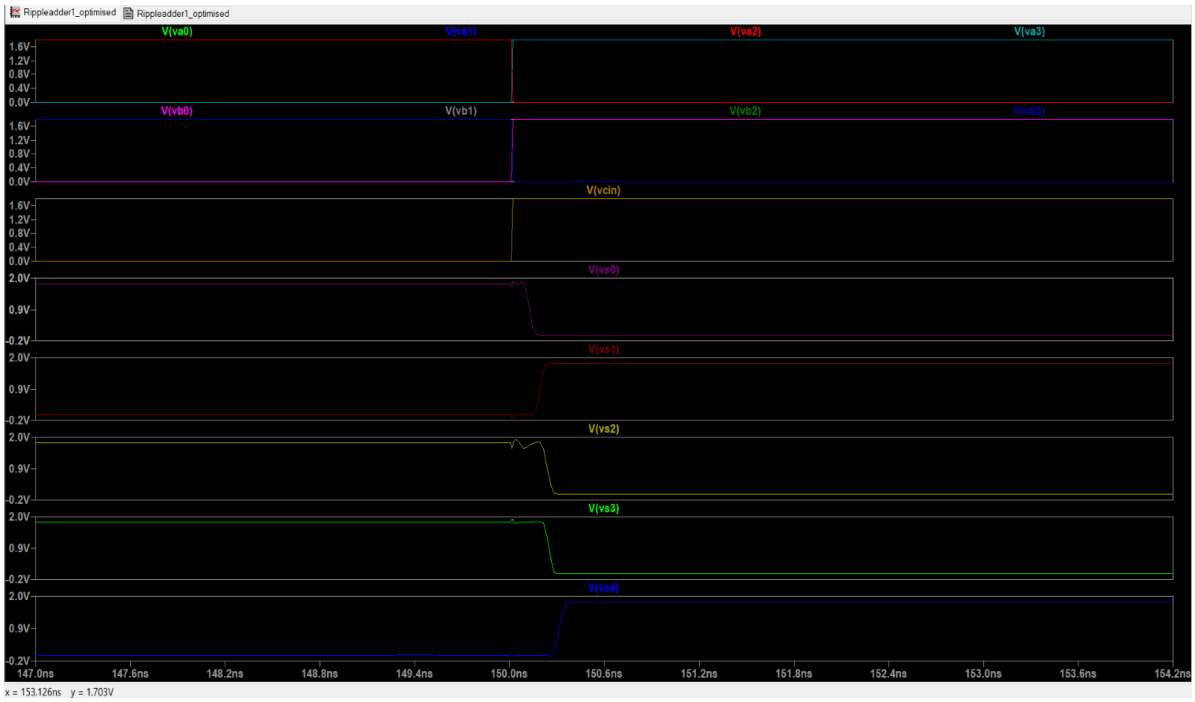


Output Graphs of Optimised Four-Bit Adder using Schematic Simulations :

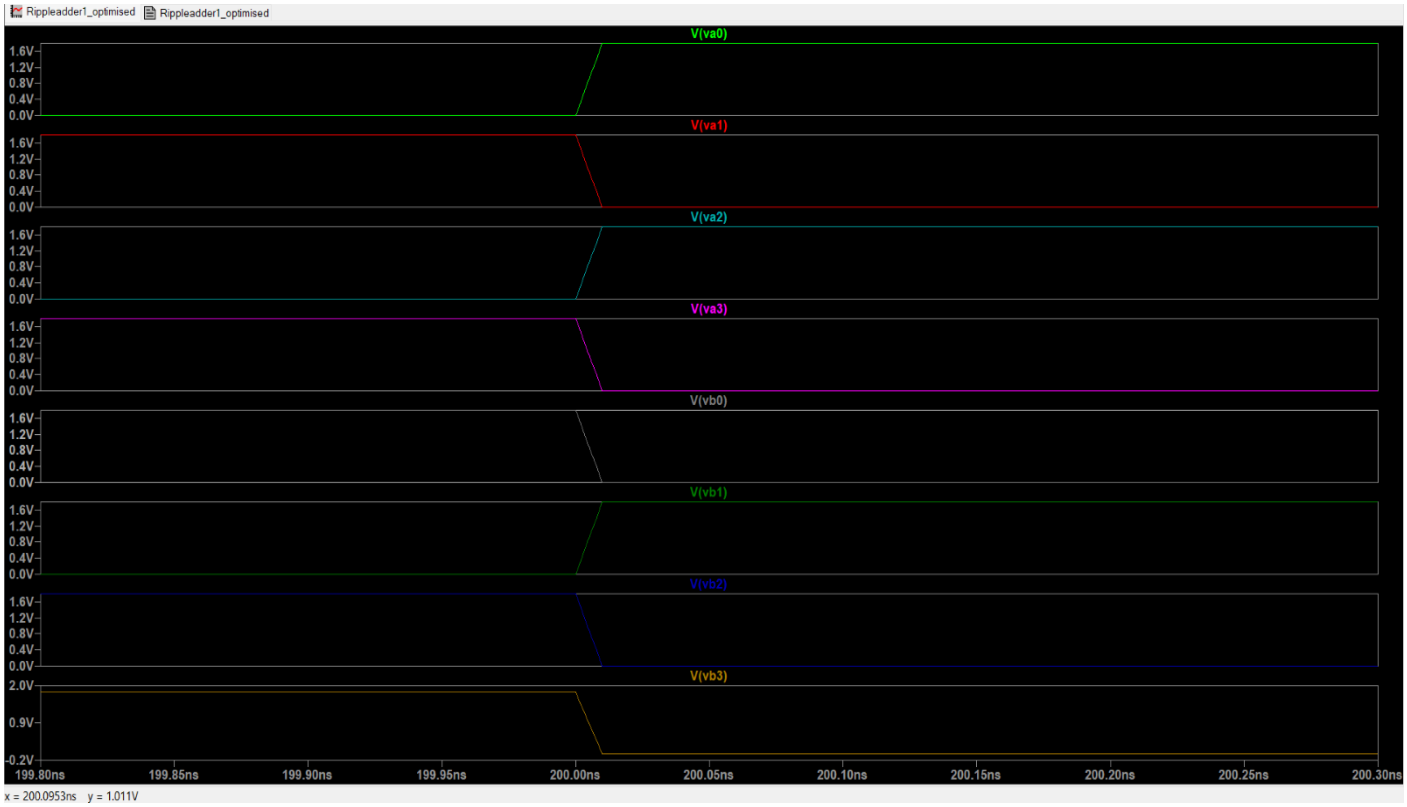
Case 1 : a0, a1 ,a2, a3 = 1 → 0; b0, b1, b2, b3 = 1 → 0; Cin = 0 → 1

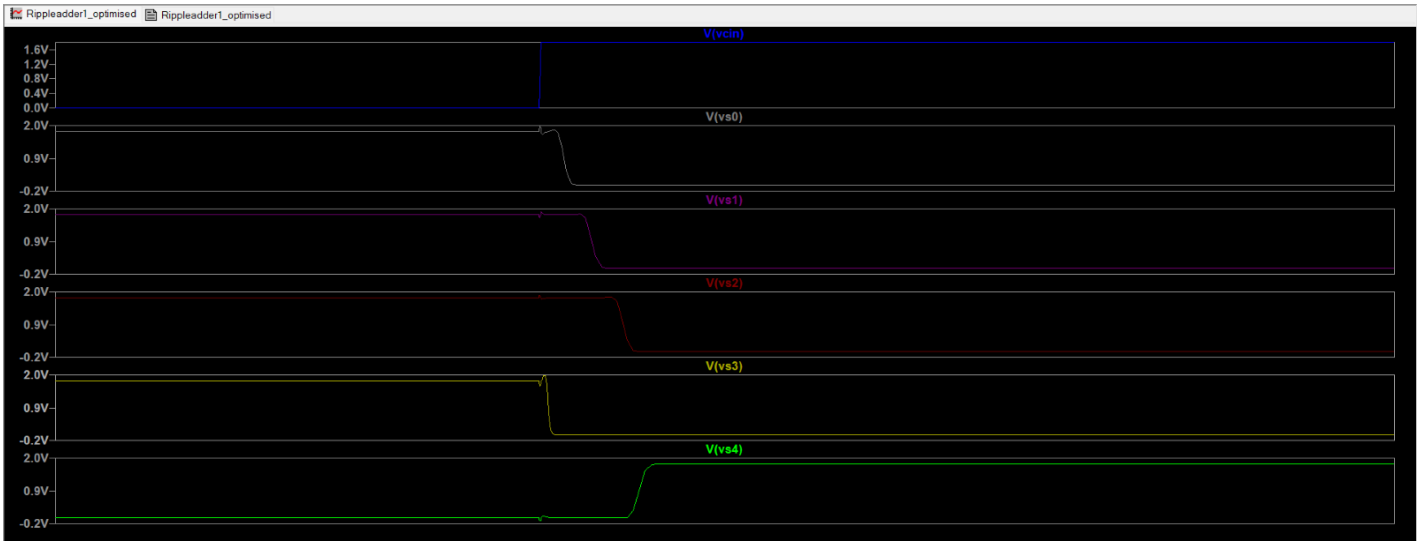


Case 2 : a0, a1, a2 = 0 → 1; b0, a3 = 1 → 0; b1,b2,b3 = 1 → 0; Cin = 1 → 0



Case 3 : a0, a2, b1 = 0 → 1; a1, b0, a3, b3, b2 = 1 → 0; Cin = 0 → 1





Critical Path Delays for Optimised Four-Bit Adder :
(We use S3 for critical path delay)

Case 1 : a0, a1 ,a2, a3 = 1 → 0; b0, b1, b2, b3 = 1 → 0; Cin = 0 → 1

```
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

prop_delay1=-4.85881e-009 FROM 5.0015e-009 TO 1.42692e-010
prop_delay2=2.26357e-010 FROM 5.0015e-009 TO 5.22786e-009
prop_delay3=2.2773e-010 FROM 5.0015e-009 TO 5.22923e-009
prop_delay4=2.27621e-010 FROM 5.0015e-009 TO 5.22912e-009
prop_delay5=6.34556e-011 FROM 5.0015e-009 TO 5.06496e-009


Date: Thu Apr 24 17:02:03 2025
Total elapsed time: 0.992 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 8127
traniter = 8077
```

Propagation Delay : 227.62 ps

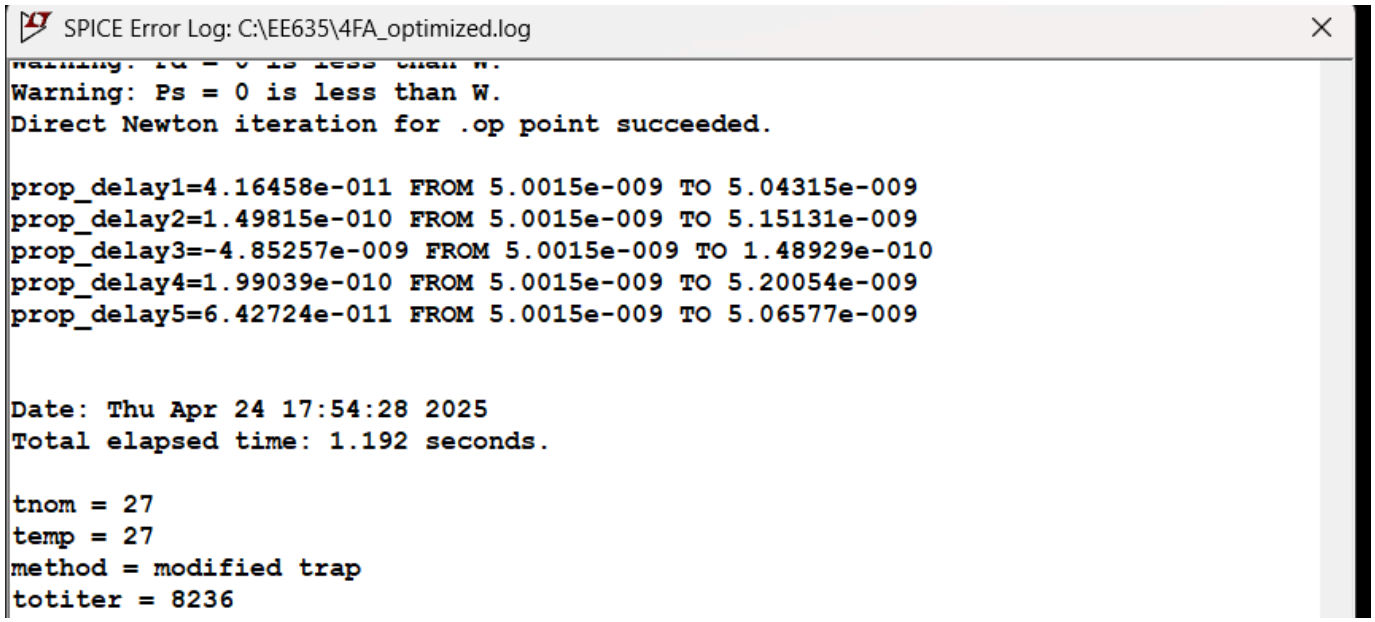
Case 2 : a0, a1, a2 = 0 → 1; b0, a3 = 1 → 0; b1,b2,b3 = 1 → 0; Cin = 1 → 0

SPICE Error Log: C:\EE635\4FA_optimized.log

```
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

prop_delay1=1.18229e-010 FROM 5e-013 TO 1.18729e-010
prop_delay2=2.78668e-010 FROM 5e-013 TO 2.79168e-010
prop_delay3=5.34747e-009 FROM 5e-013 TO 5.34797e-009
prop_delay4=2.9181e-010 FROM 5e-013 TO 2.9231e-010
prop_delay5=5.21636e-009 FROM 5e-013 TO 5.21686e-009


Date: Thu Apr 24 17:46:36 2025
Total elapsed time: 1.368 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 8396
```

Propagation Delay : 291.81 ps

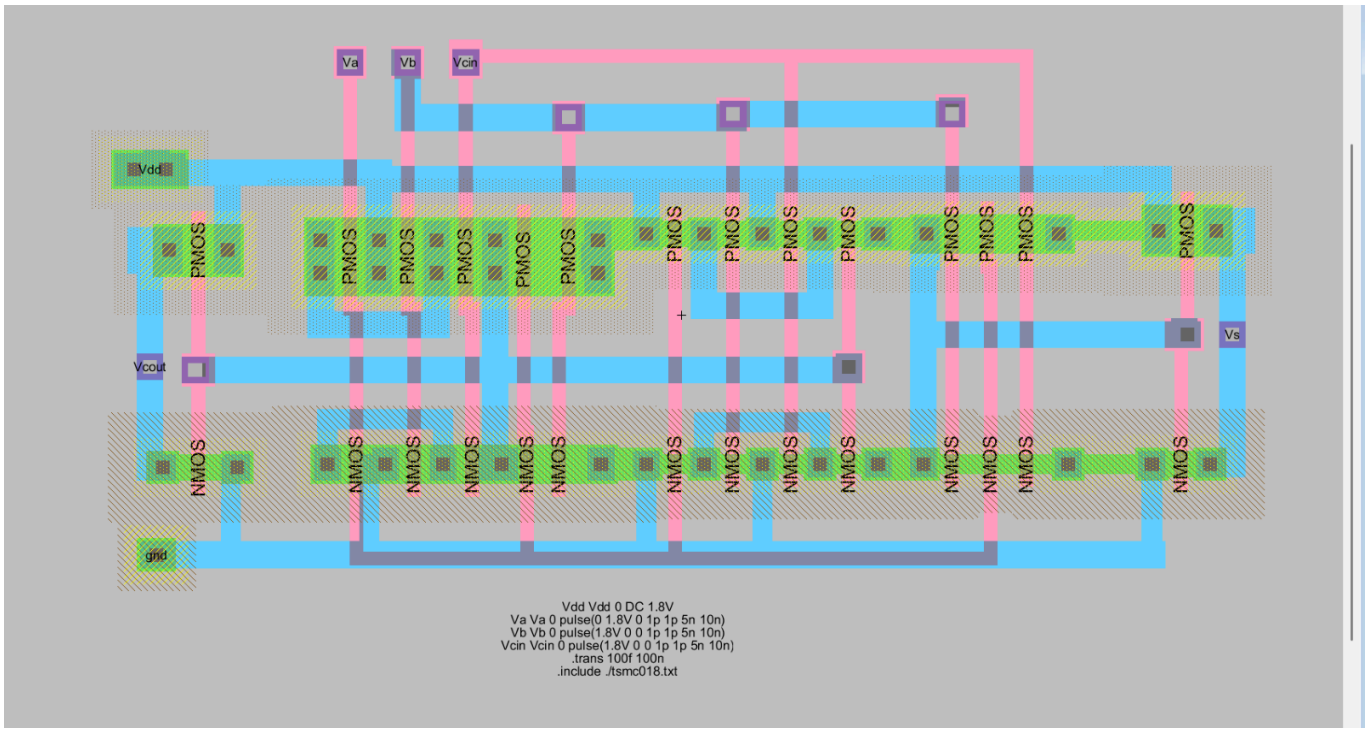
Case 3 : a0, a2, b1 = 0 → 1; a1, b0, a3, b3, b2 = 1 → 0; Cin = 0 → 1



Propagation Delay : 199.03 ps

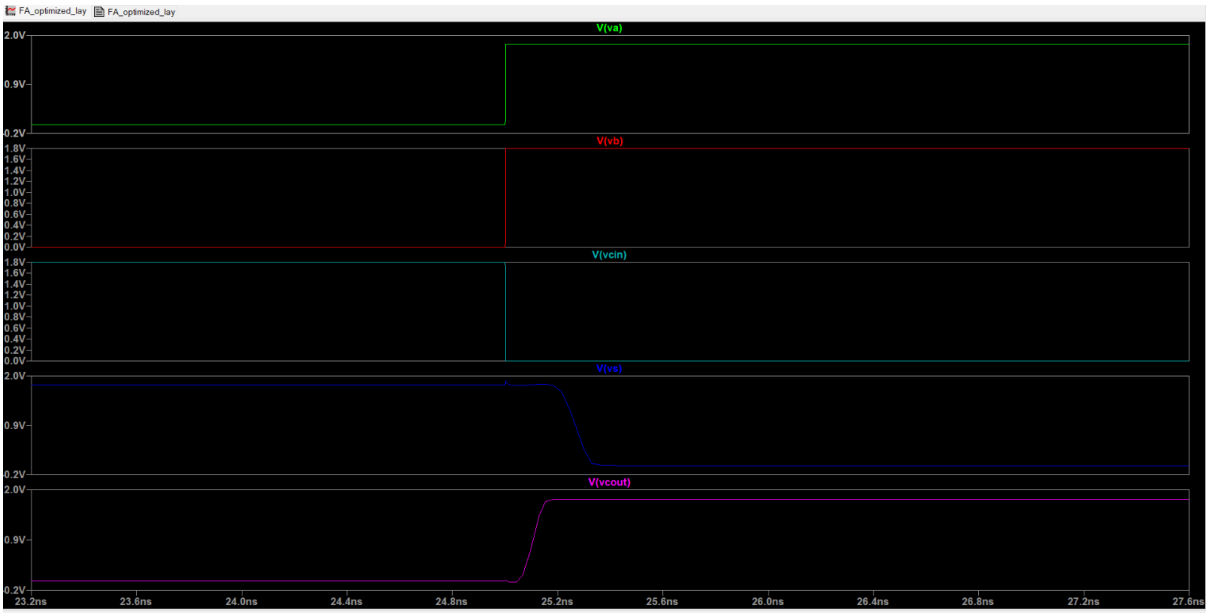
Post-Layout Simulations :

Optimised Full Adder Layout :

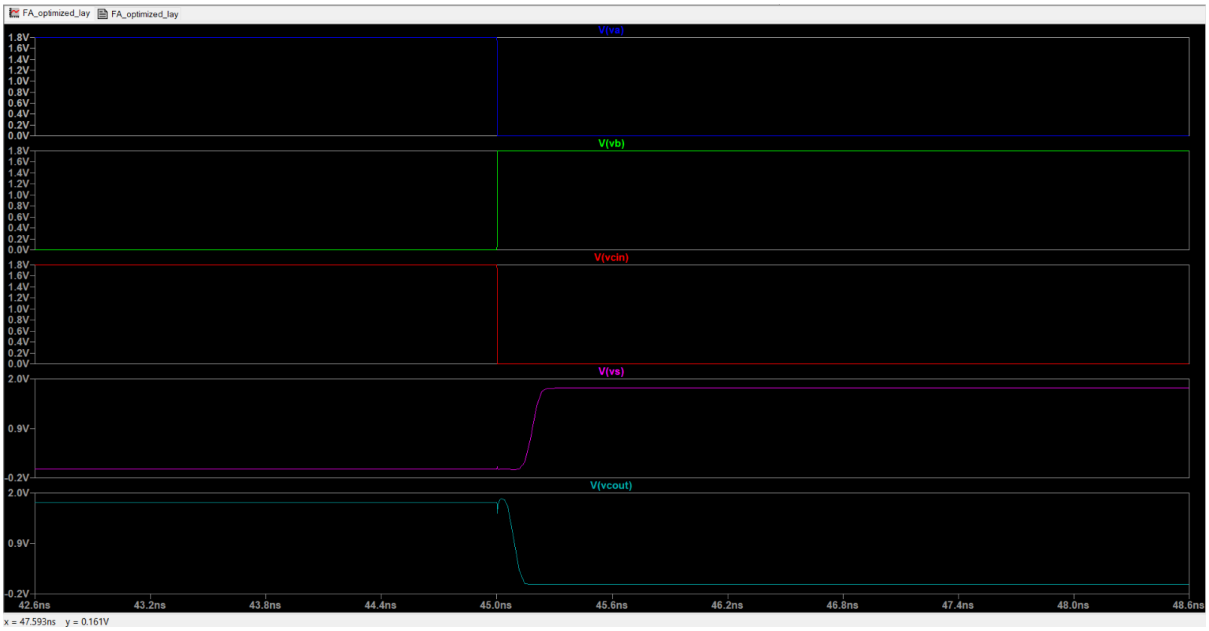


Output Waveforms of Optimised Full Adder using Schematic Simulations :

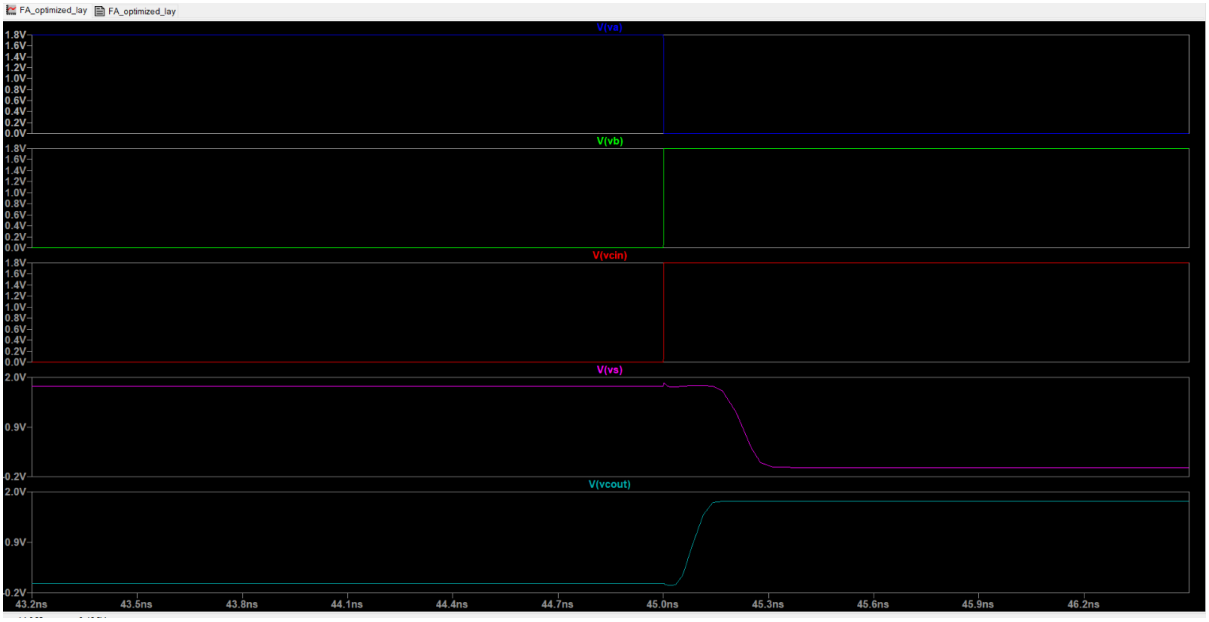
Case 1 : A,B = 1 → 0 (High to Low), Cin = 0 → 1 (Low to high)



Case 2 : A = 0 → 1 (Low to High) ,B = 1 → 0 (High to Low), Cin = 0 → 1 (Low to high)

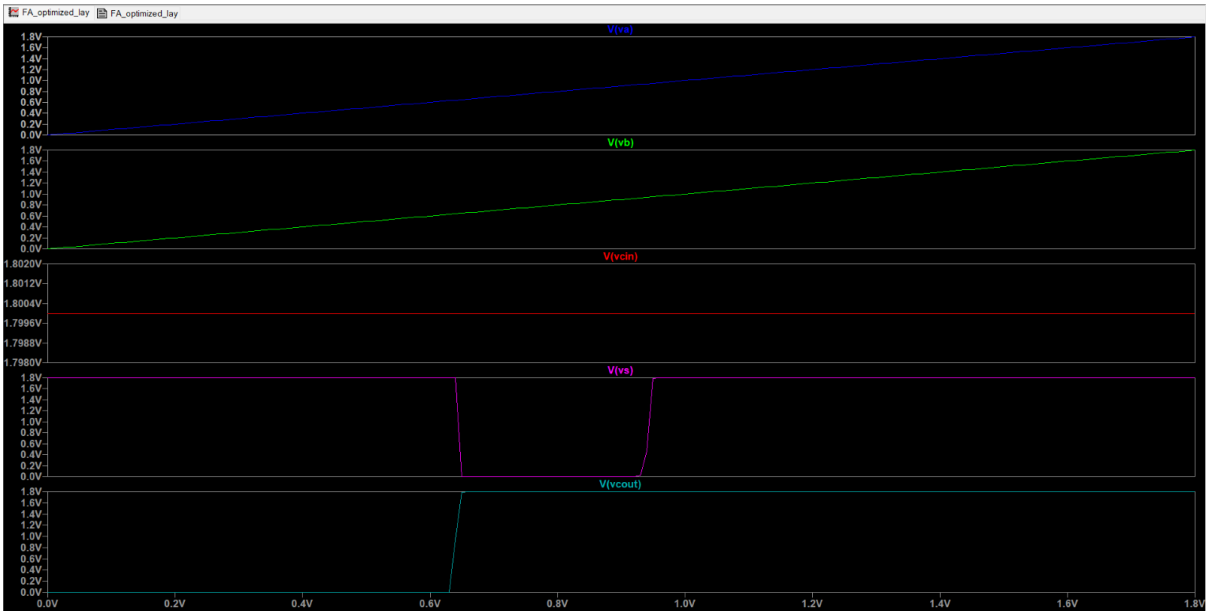


Case 3 : A = 0 → 1 (Low to High) ,B = 1 → 0 (High to Low), Cin = 1 → 0 (High to Low) :

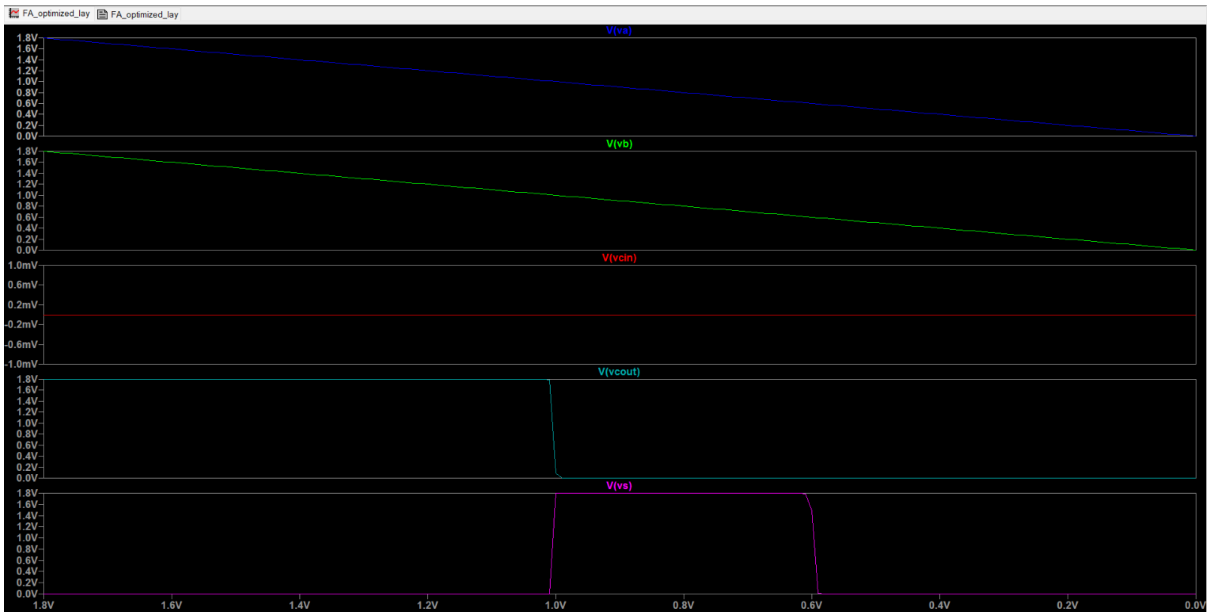


VTC of Optimised Full Adder using Layout Simulations :

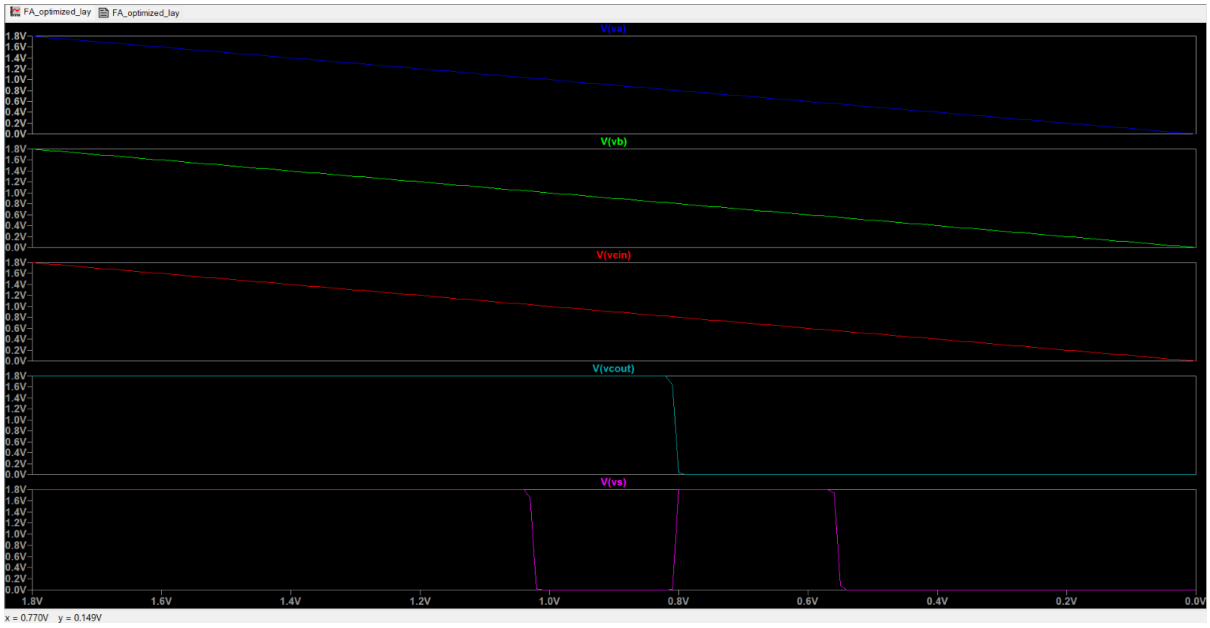
Case 1: A = B = 0 ⟶ 1, Cin = 1



Case 2: A = B = 1 ⟶ 0, Cin = 0



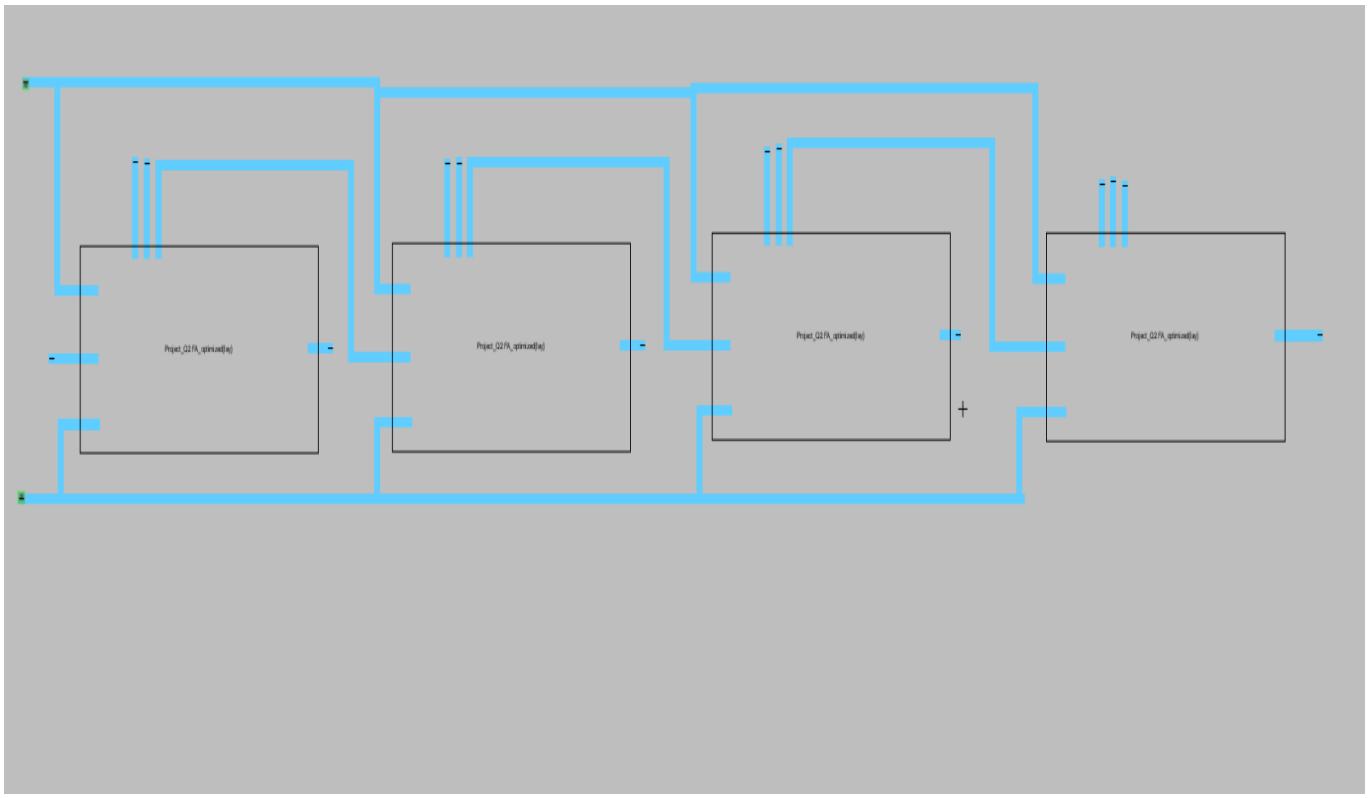
Case 3: A = B = Cin = 1⟶ 0



Propagation Delays of Optimised Full Adder using Layout Simulations :

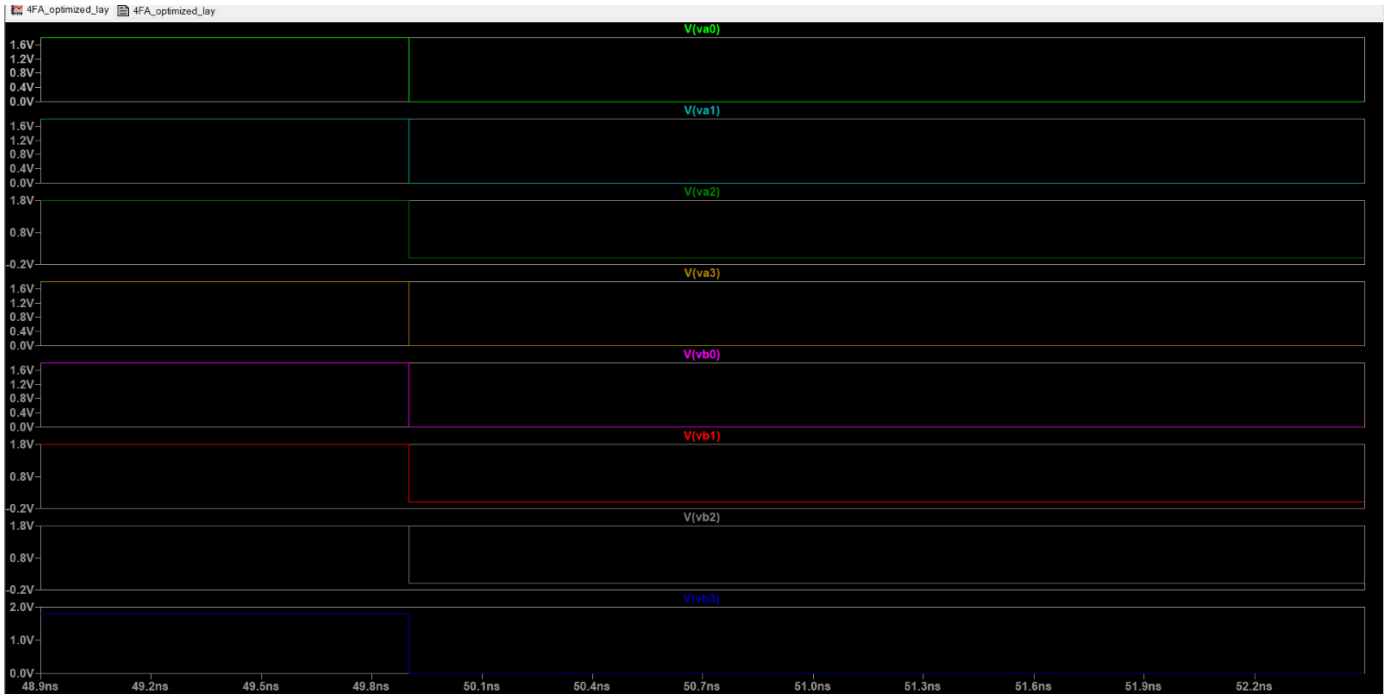
Case 1 : A,B = 1 → 0 (High to Low), Cin = 0 → 1 (Low to high)

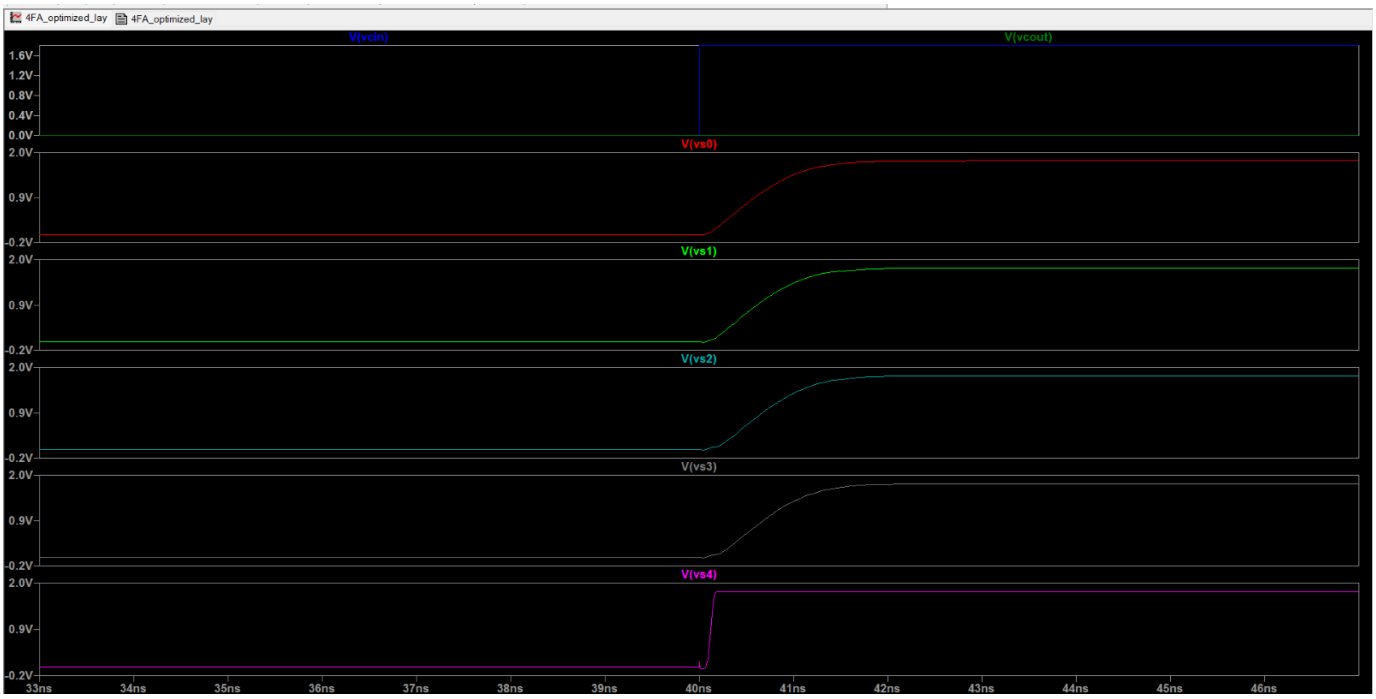
Optimised Four-Bit Adder Layout (by repeating optimised Full Adder Layout Blocks) :



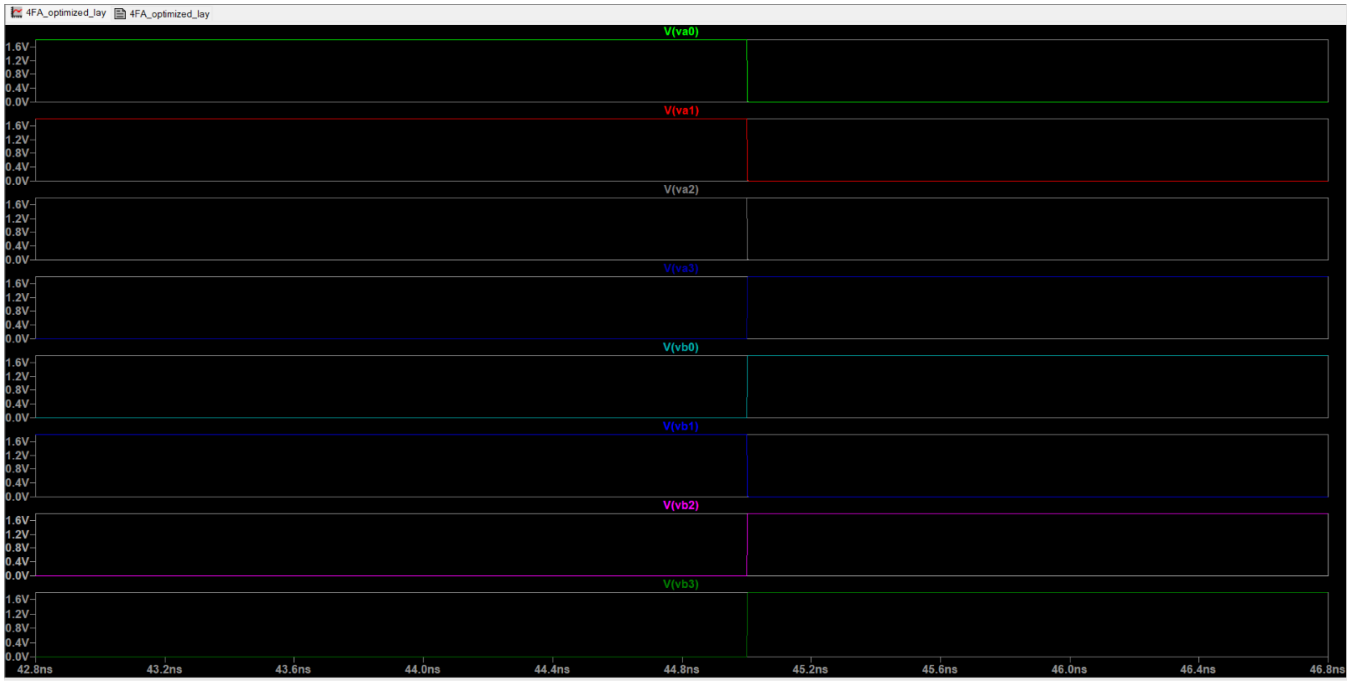
Output Graphs of Optimised Four-Bit Adder using Schematic Simulations :

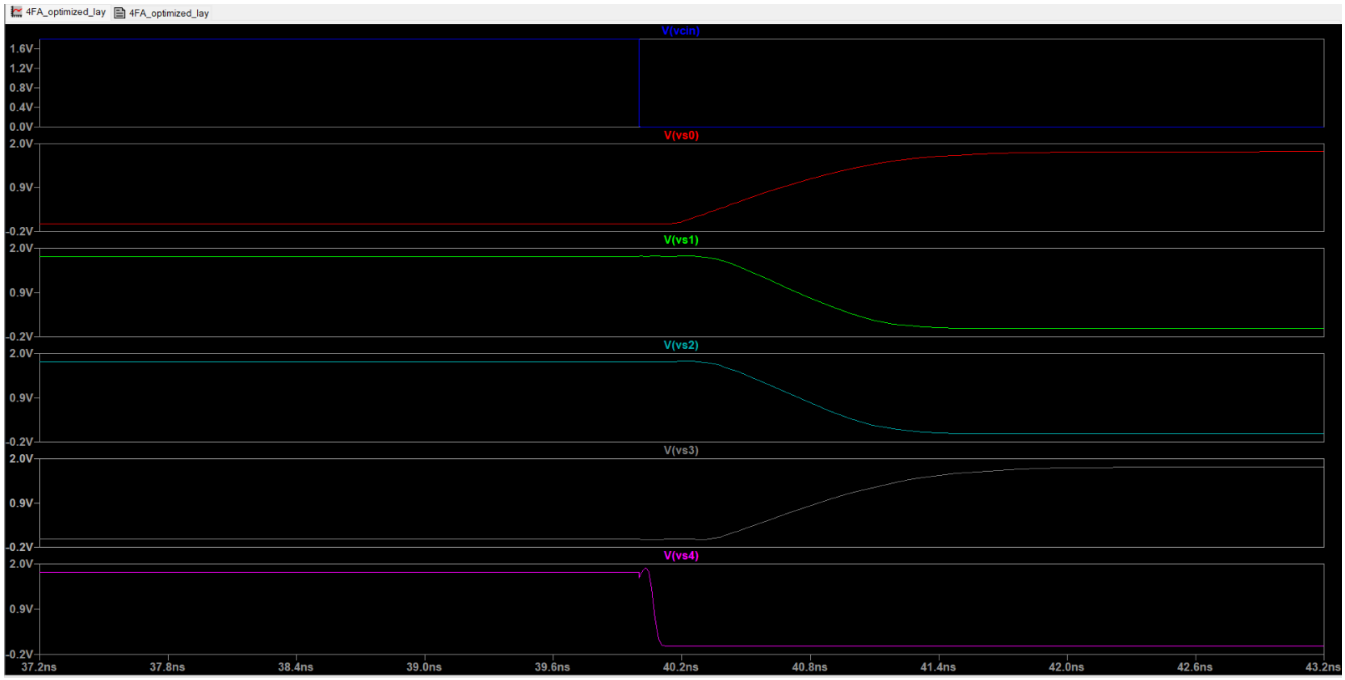
Case 1 : a0, a1 ,a2, a3 = 1 → 0; b0, b1, b2, b3 = 1 → 0; Cin = 0 → 1



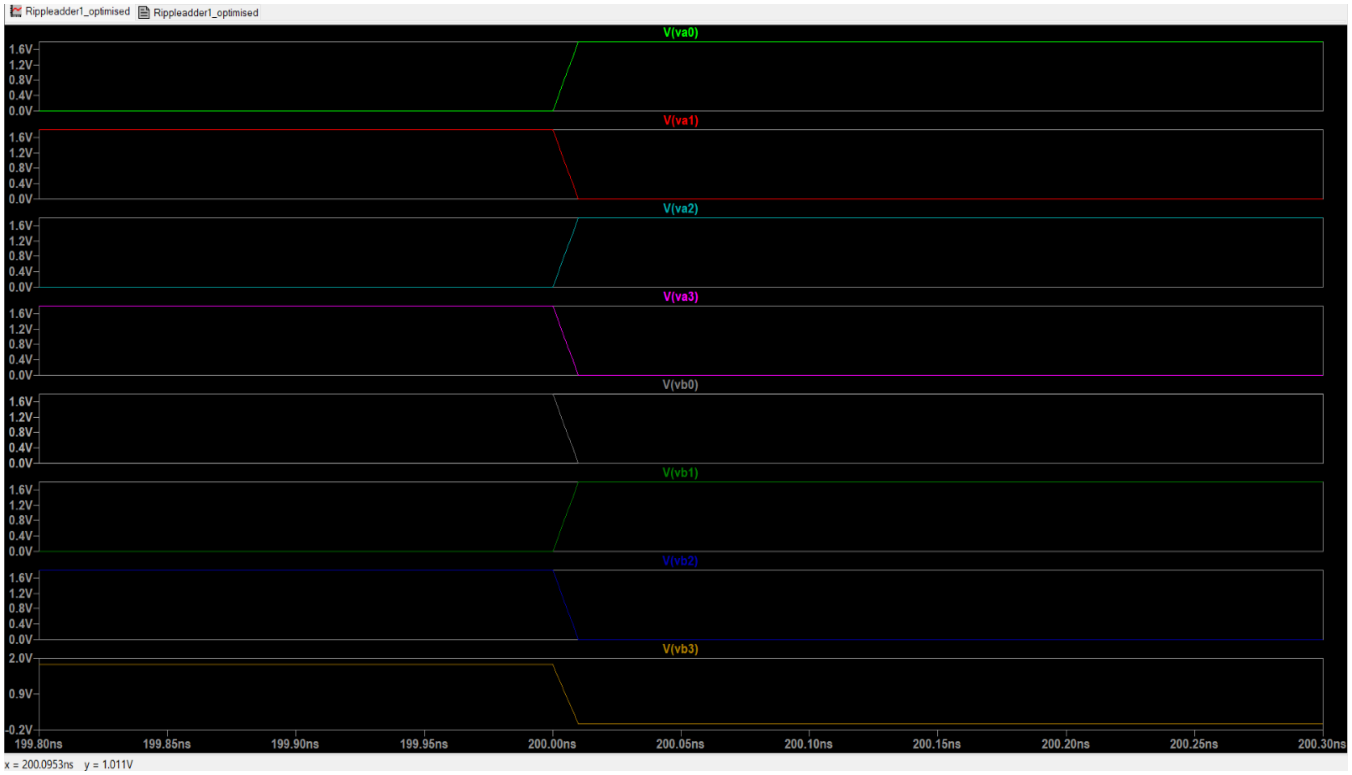


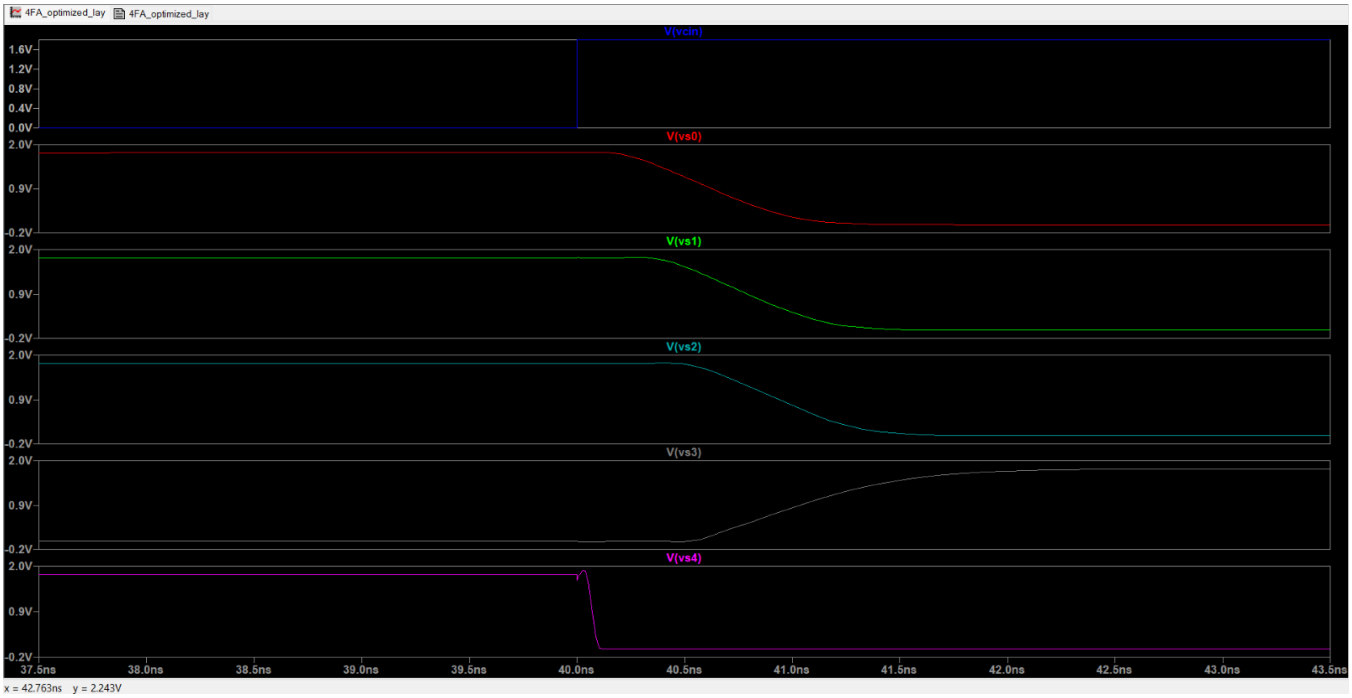
Case 2 : a0, a1, a2 = 0 → 1; b0, a3 = 1 → 0; b1,b2,b3 = 1 → 0; Cin = 1 → 0





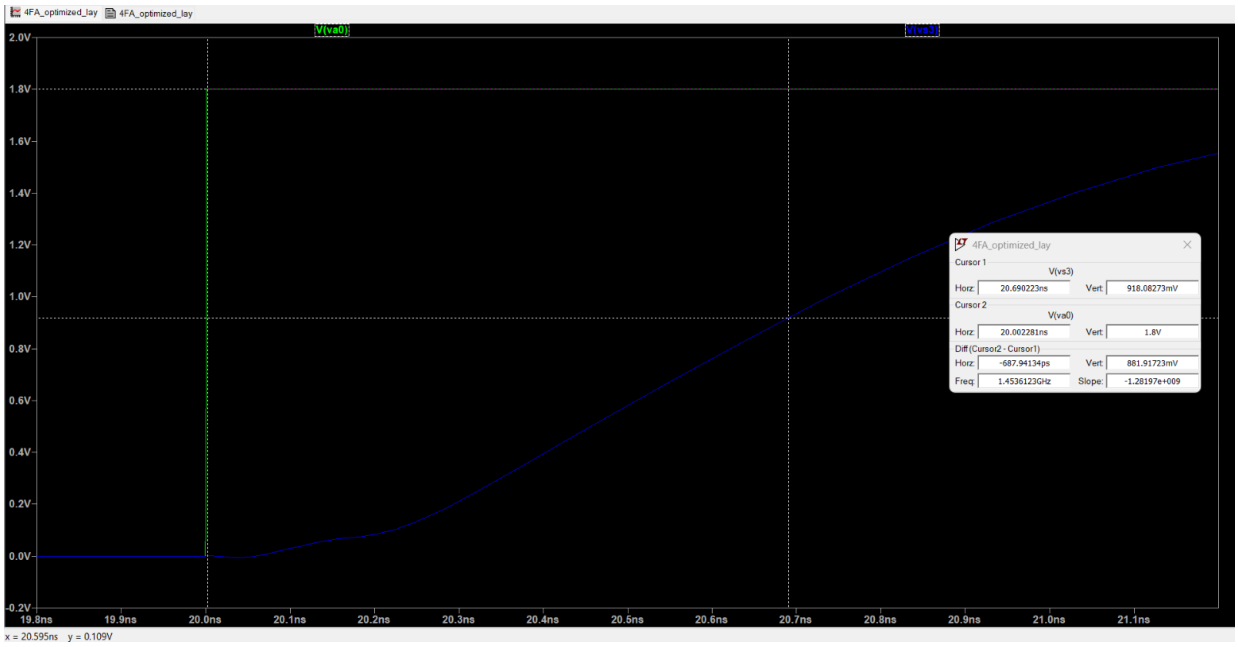
Case 3 : a0, a2, b1 = 0 → 1; a1, b0, a3, b3, b2 = 1 → 0; Cin = 0 → 1



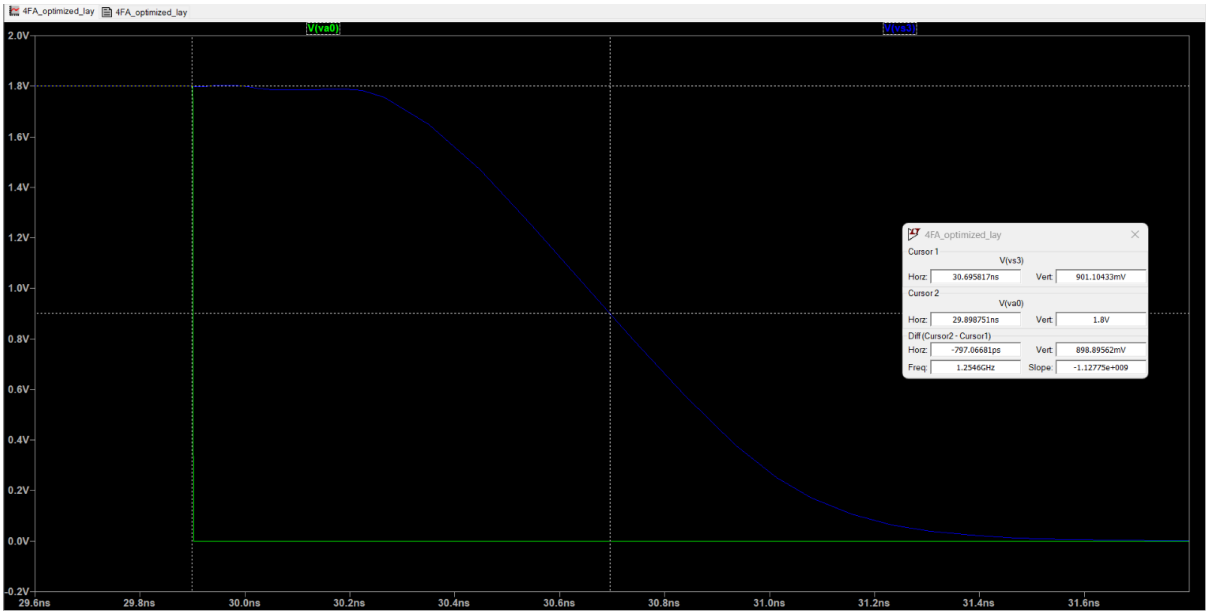


Critical Path Delays for Optimised Four-Bit Adder :
(We use S3 for critical path delay)

Case 1 : a0, a1 ,a2, a3 = 1 → 0; b0, b1, b2, b3 = 1 → 0; Cin = 0 → 1



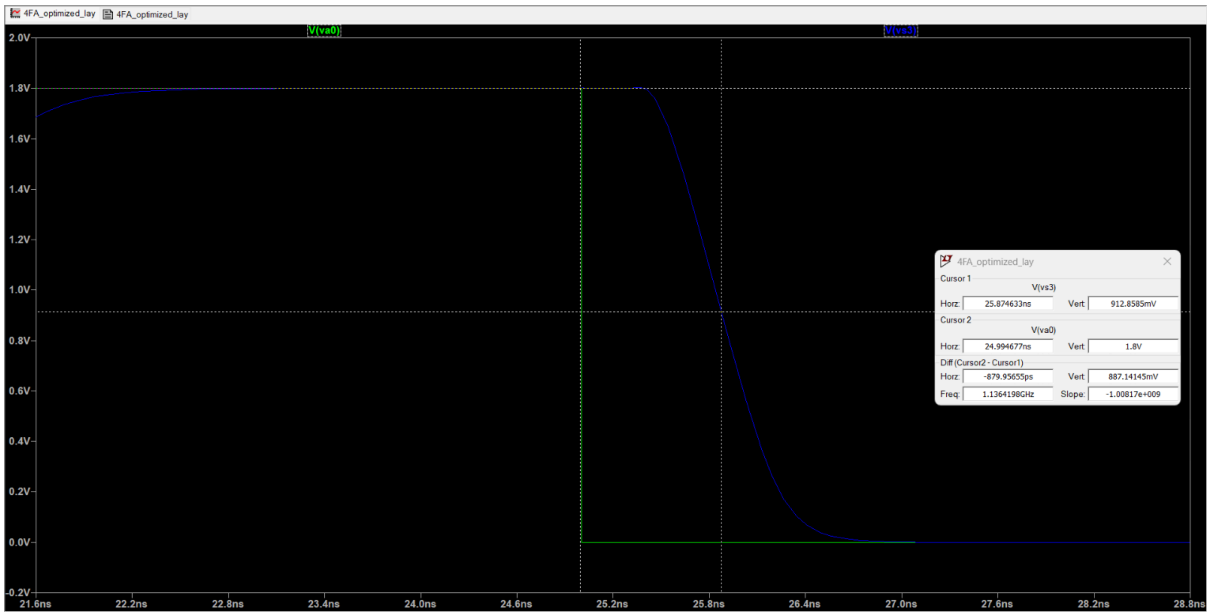
tpLH = 647.94 ps



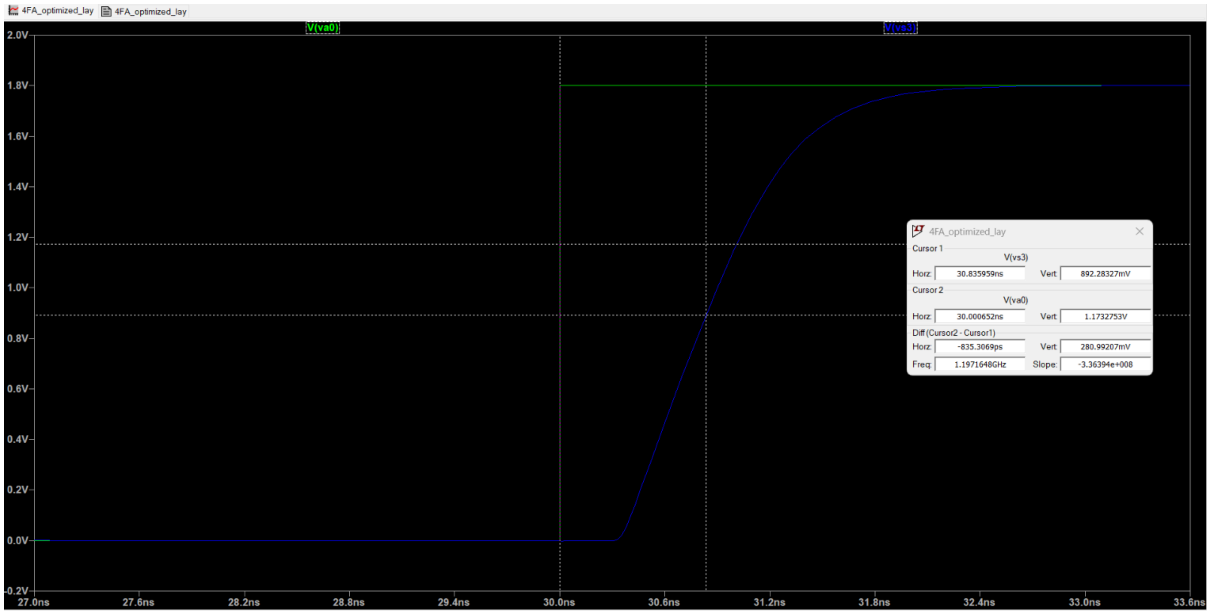
tpHL = 797.66 ps

Propogation delay = (tpLH + tpHL)/2 = 722.8 ps

Case 2 : a0, a1, a2 = 0 → 1; b0, a3 = 1 → 0; b1,b2,b3 = 1 → 0; Cin = 1 → 0



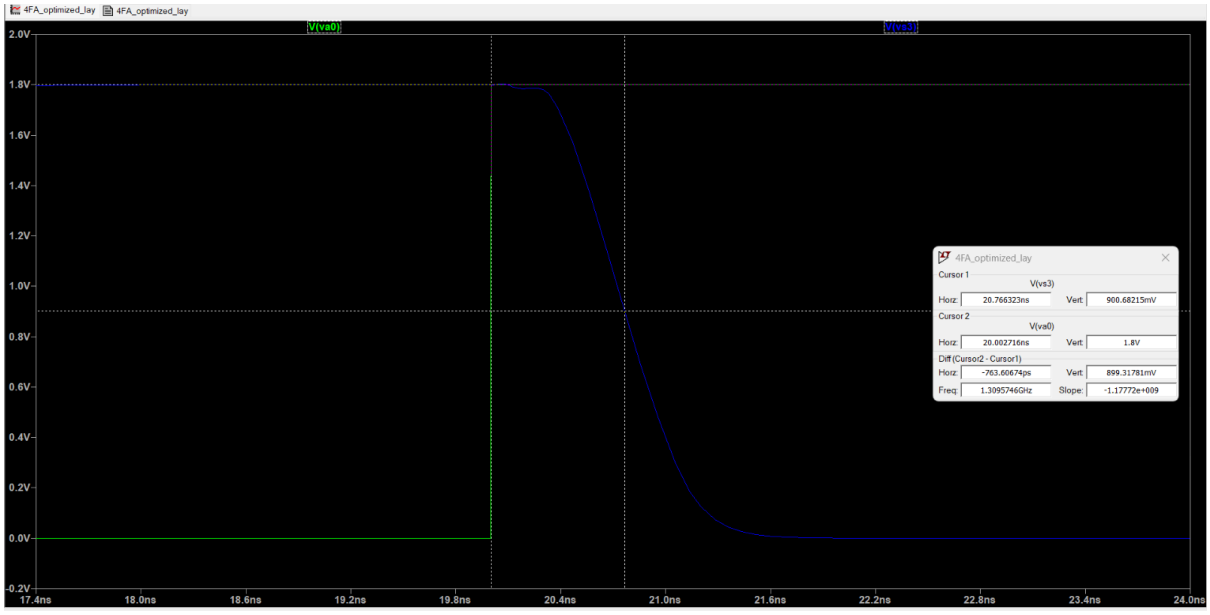
tpHL= 879.95 ps



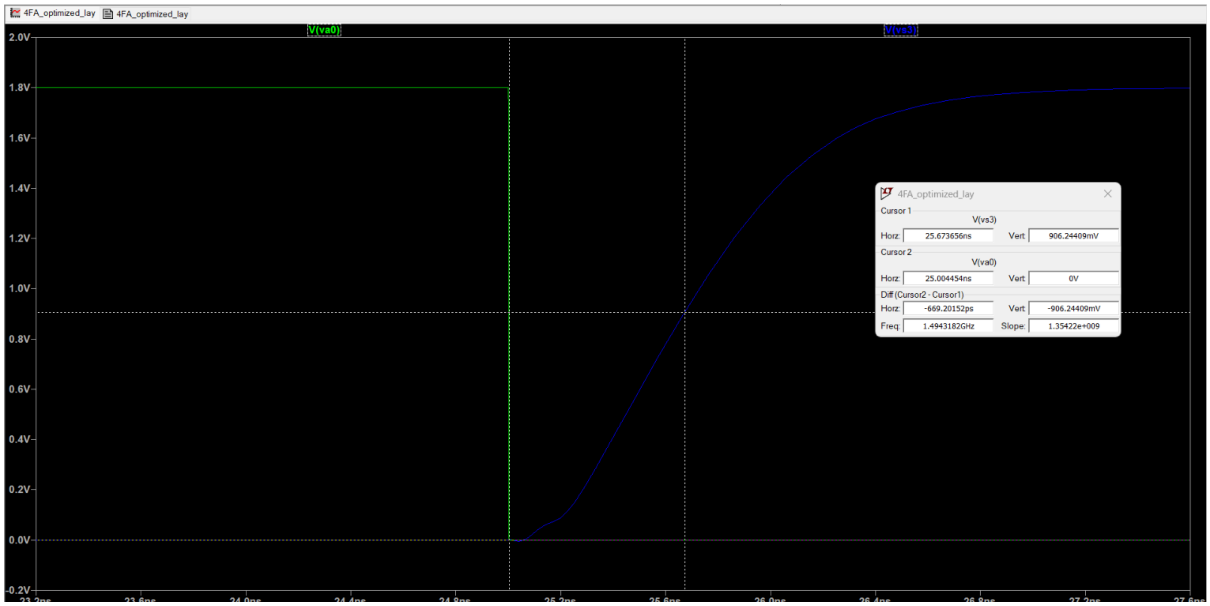
tpLH = 835.30 ps

Propogation delay = (tpLH + tpHL)/2 = 857.62 ps

Case 3 : a0, a2, b1 = 0 → 1; a1, b0, a3, b3, b2 = 1 → 0; Cin = 0 → 1 :



tpLH = 763.60 ps



tpHL = 669.20 ps

Propogation delay = (tpLH + tpHL)/2 = 716.4 ps

Conclusion:

By optimizing the Full Adder design, we achieved a significant reduction in propagation delay. This improvement enhances the overall speed and performance of the 4-bit Adder, making it more efficient for digital circuit applications. The results validate the effectiveness of our optimization approach in high-speed arithmetic unit design.

Teamwork Distribution:

Team Members Name	Contribution
Mehak	Schematic full adder(unoptimised)+propagation delay simulations of unoptimised full adder +full adder layout + 4 bit adder schematic
Jatin	Schematic full adder(optimised)+propagation delay simulations of optimised full adder + full adder layout + 4 bit adder schematic
Harshith	Schematic full adder(optimised)+propagation delay simulations of optimised full adder + full adder layout + 4 bit adder layout and schematic
Ruthwik	Schematic full adder(unoptimised)+propagation delay simulations of unoptimised full adder + full adder layout