

A Tensor Compiler for Processing-In-Memory Architectures

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Abstract—Processing-In-Memory (PIM) devices integrated with high-performance Host processors (e.g., GPUs) can accelerate memory-intensive kernels in Machine Learning (ML) models, including Large Language Models (LLMs), by leveraging high memory bandwidth at PIM cores. However, Host processors and PIM cores require different data layouts: Hosts need consecutive elements distributed *across* DRAM banks, while PIM cores need them *within* local banks. This necessitates data rearrangements in ML kernel execution that pose significant performance and programmability challenges, further exacerbated by the need to support diverse PIM backends. Current compilation approaches lack systematic optimization for diverse ML kernels across multiple PIM backends and may largely ignore data rearrangements during compute code optimization. We demonstrate that data rearrangements and compute code optimization are interdependent, and need to be jointly optimized during the tuning process. To address this, we design DCC, the first data-centric ML compiler for PIM systems that jointly co-optimizes data rearrangements and compute code in a unified tuning process. DCC integrates a multi-layer PIM abstraction that enables various data distribution and processing strategies on different PIM backends. DCC enables effective co-optimization by mapping data partitioning strategies to compute loop partitions, applying PIM-specific code optimizations and leveraging a fast and accurate performance prediction model to select optimal configurations. Our evaluations in various individual ML kernels demonstrate that DCC achieves up to 7.68× speedup (2.7× average) on HBM-PIM and up to 13.17× speedup (5.75× average) on AttAcc PIM backend over GPU-only execution. In end-to-end LLM inference, DCC on AttAcc accelerates GPT-3 and LLaMA-2 by up to 7.71× (4.88× average) over GPU.

I. INTRODUCTION

Machine Learning (ML) models achieve state-of-the-art results in various tasks of everyday applications across domains including finance [1], [2], retail [3], healthcare [4], [5], and autonomous systems [6], [7]. These models process increasingly large datasets and comprise both compute-intensive kernels such as general matrix-matrix multiplication (GEMM) and convolutions, as well as memory-intensive kernels such as general matrix-vector multiplication (GEMV) and element-wise operations. For instance, Large Language Models (LLMs) [8], [9] contain both compute-intensive fully-connected layers with GEMM kernels and memory-intensive attention layers with GEMV kernels. However, when executed on processor-centric CPU/GPU systems, memory-intensive ML kernels are significantly bottlenecked by data movement between off-chip

memory and processors [10]–[14]. Such memory bottlenecks increasingly limit end-to-end ML execution performance.

Processing-In-Memory (PIM) [15]–[19] has emerged as a promising paradigm to alleviate data movement bottlenecks by placing low-power processing units (PIM cores) near memory arrays. Numerous works [11]–[14], [20]–[31] demonstrate that PIM can provide significant performance benefits for memory-intensive ML kernels by reducing data movement costs.

A PIM system includes multiple PIM-enabled memory devices connected to a high-performance *Host* processor (e.g., CPU, GPU, TPU). Near-bank PIM devices tightly couple a PIM core with one or few DRAM banks, exploiting bank-level parallelism to enable large aggregate memory bandwidth. Each PIM core can only access data from its local bank(s). PIM cores of a device may not be able to directly communicate with each other, and inter-core communication can happen via the Host. Manufacturers have already started to commercialize near-bank PIM designs. UPMEM PIM [11], [12], [19] is the first commercialized near-bank PIM device, and can be integrated with CPUs. Samsung HBM-PIM [18] and SK Hynix GDDR6-AiM [16], [17] PIM devices have been prototyped and validated, and can be integrated with GPUs. These PIM systems can enable heterogeneous ML execution, where memory-intensive kernels run on PIM cores and compute-intensive kernels run on Host processor.

Host and PIM cores require fundamentally different data layouts to exploit large available memory bandwidth. Host distributes consecutive elements *across* multiple DRAM banks to exploit bank-level parallelism, and enables large bandwidth when accessing data at cache line granularity. In contrast, a PIM core can access data only from its local bank(s), thus in PIM consecutive elements must be placed *within* the same bank to enable efficient multi-element accesses and maximize local bandwidth. Consequently, the execution of a PIM kernel has three steps: (1) input data rearrangements to place consecutive elements within the same banks for local PIM processing, (2) computation on PIM cores, and (3) output data rearrangements to merge partial results produced from step (2) on PIM cores or prepare output data for Host access by redistributing consecutive elements across banks. These data rearrangements are typically performed via the Host memory bus (outside PIM devices), and thus incur large data movement

costs that can dominate end-to-end performance [11]–[14].

Therefore, programming PIM devices is a challenging task [11]–[14], [32]. Programmers must manually craft data rearrangement strategies that balance data movement costs with computation efficiency, which requires deep understanding of both the PIM system and the kernel-specific access patterns of each ML operator. This also demands expertise in low-level programming across multiple PIM backends [11]–[14], [16]–[31], which may expose different programming interfaces and optimization capabilities. This complexity necessitates compilation tools that automatically and intelligently generate and optimize data rearrangements and compute code to enhance programmability and minimize end-to-end execution time.

Compilation support with performance optimization capabilities for PIM systems remains in early stages. Existing compilation works for PIM [14], [31]–[34] lack systematic optimization and auto-tuning for diverse ML kernels and/or support for multiple PIM backends. They largely ignore data rearrangement costs or target only UPMEM PIM. However, UPMEM PIM is designed for CPU systems using DDR4 interfaces, has limited hardware multiplication support and lacks floating-point arithmetic support, making it unsuitable for ML workloads that typically require GPU-PIM co-execution [13], [20], [25], [26], [29] and native floating-point operations. ATiM [31] is a search-based tensor compiler that optimizes diverse ML kernels, but supports only UPMEM PIM, being limited to CPU-PIM co-execution. More critically, ATiM follows a compute-centric approach: it optimizes compute code *without* accounting for data rearrangement costs *during* the compute generation step. However, as we demonstrate in §II-B, compute code transformations and data rearrangements are *interdependent*. Optimizing them in isolation yields sub-optimal performance (See Fig. 2): a compute transformation that appears efficient in isolation may require expensive data rearrangements, while a less efficient compute transformation discarded during compute optimization could enable cheaper data rearrangements. Achieving optimal performance requires balancing both costs during tuning rather than optimizing them in isolation.

To this end, we propose DCC, a data-centric ML compiler for PIM systems that elevates data rearrangements at the core of the tuning process, jointly co-optimizing them with compute code to improve end-to-end ML kernel performance and enhance programmability. DCC comprises four key components. First, we propose a generic multi-layer abstraction that maps PIM memory hierarchy into a compute hierarchy, where PIM cores form PIM groups. This abstraction decouples the compiler from backend-specific semantics, enabling DCC to support multiple PIM backends and explore diverse data distribution and data processing strategies. Second, we design a data-centric schedule generator that constructs all candidate data tensor partitions of an ML kernel across PIM resources and maps them to compute loop partitions. This mapping enables comprehensive co-optimization of data rearrangements with compute code. Third, we integrate a PIM-specific code optimizer that applies data rearrangement and compute code

optimizations tailored for PIM systems. This optimizer can be extended with additional PIM-specific optimizations. Fourth, we design a learning-based coupled predictor that jointly evaluates data rearrangement and compute code times, and selects the best-performing end-to-end kernel configuration. This predictor provides fast and accurate performance estimates on diverse PIM backends and ML kernels.

We evaluate DCC across diverse ML kernels, tensor sizes, and models using two state-of-the-art PIM backends, HBM-PIM [18] and AttAcc [20]. In individual ML kernels, DCC achieves up to 7.68 \times speedup (2.7 \times average) on HBM-PIM and up to 13.17 \times speedup (5.75 \times average) on AttAcc compared to GPU-only execution. In end-to-end LLM inference on AttAcc, DCC achieves up to 7.71 \times speedup (4.88 \times average) over GPU and up to 2.74 \times speedup (1.86 \times average) over AttAcc’s original implementations.

Overall, we make the following contributions:

- We demonstrate that data rearrangements and compute code must be jointly optimized for ML kernels on PIM architectures, and propose DCC, the first data-centric ML compiler that co-optimizes both in a unified tuning process.
- We design a multi-layer abstraction that maps PIM memory hierarchy into a compute hierarchy, and propose a schedule generator that constructs data tensor partitions and maps them to compute loop partitions. We integrate PIM-aware optimizations for data rearrangements and compute code, and employ a learning-based coupled predictor to select optimal end-to-end execution time configurations.
- We evaluate DCC on two state-of-the-art PIM backends, and show that DCC achieves significant performance improvements for diverse ML kernels, tensor sizes, and LLMs.

II. BACKGROUND AND MOTIVATION

A. Processing-In-Memory (PIM) Architectures

Processing-In-Memory (PIM) [12], [16]–[18] places low-power processing units near memory arrays, and can alleviate data movement bottlenecks in processor-centric CPU/GPU systems. Near-bank PIM designs tightly couple each core with one (or a few) DRAM banks that can access data from its local bank(s). Near-bank PIM provides larger aggregate memory bandwidth and parallelism compared to near-rank PIM, where cores are placed at DRAM buffer chip. UPMEM PIM [12], [19] is the first commercialized PIM system. Samsung HBM-PIM [18] and SK Hynix GDDR6-AiM [16], [17] have been prototyped and validated in real systems.

UPMEM PIM is built on DDR4 interfaces for CPU systems, has limited hardware multiplication support and no floating-point arithmetic units [12]. Due to these limitations, UPMEM PIM with CPU-PIM co-execution in ML workloads cannot typically outperform GPU-only execution [12]–[14]. In contrast, Samsung HBM-PIM [18] and SK Hynix GDDR6-AiM [16], [17] are 3D memory devices that integrate with a high-performance xPU processor such as GPU and TPU, provide hardware multiplication and floating-point units (e.g., FP16), thus making them suitable for ML acceleration. Building on these industry products, numerous research works [20]–

[30] explore enhanced PIM core microarchitectures to further accelerate ML kernels. In this work, we target near-bank PIM devices that can be integrated with GPUs/TPUs, have hardware multiplication support and/or floating-point arithmetic units.

We find common characteristics in existing PIM designs [16]–[30], as shown in Fig. 1. First, a high-performance processor, **Host xPU** (e.g., GPU, TPU) with on-chip cache hierarchy and Host memory typically connects to multiple PIM devices. Second, each PIM device contains multiple processing unit (**PIM cores**) that can be organized into **PIM groups**. Each PIM core (e.g., a SIMD unit, GEMV unit or other specialized processing units) has exclusive access to one or few local memory banks, enabling larger aggregate memory bandwidth and lower latency than Host cores have. Third, PIM cores have register files or scratchpad data memory. They may support SIMD execution, hardware multiplication, low-precision floating-point units or other specialized units. Fourth, the Host sends compute instructions that are stored as PIM instructions in register files (or instruction cache) of PIM cores. PIM cores execute PIM instructions to move data from/to their local banks to/from registers and/or perform computations (e.g., MUL, ADD) using data stored in registers. Fifth, PIM designs may integrate specialized compute units per PIM core group for specific ML kernels. For example, AttAcc [20] provides hardware softmax and accumulator support per PIM core group, enabling full attention execution on the PIM side. Finally, PIM cores may not be able to directly communicate with each other, and communication between them typically happens via the Host memory bus.

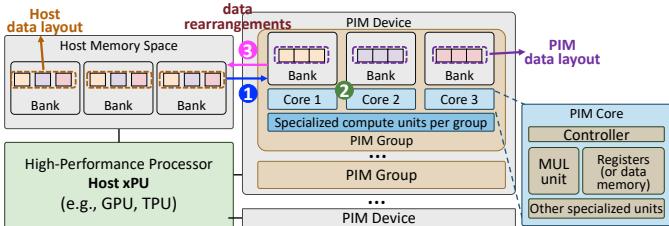


Fig. 1: Near-bank PIM architecture and kernel execution workflow showing (1) input rearrangement, (2) computation execution, and (3) output rearrangement steps.

Host xPU and PIM cores require different data layouts to fully leverage the available memory bandwidth, necessitating software-managed data rearrangements (Fig. 1). Host xPU distributes consecutive elements *across* multiple DRAM banks to exploit bank-level parallelism for large bandwidth, when accessing multiple elements as a cache line. Instead, PIM cores require consecutive elements *within* the same bank: since each core accesses data only from its local bank(s), maximizing local bandwidth requires placing consecutive elements in the same bank to efficiently fetch multiple elements at once as a block. Thus, PIM kernel execution has three steps (Fig. 1): (1) input data rearrangements to place consecutive elements within the same banks for local PIM core processing, (2) computation execution on PIM cores, and (3) output data rearrangements to either merge partial results from step (2) on PIM cores or pre-

pare output data for Host access by redistributing consecutive elements across multiple banks. Data rearrangements in steps (1) and (3) are needed even if data is mapped to the same bank, that is used for either Host or PIM access. They are typically performed via the Host memory bus (outside PIM devices), thus incurring significant **data movement overheads**.

B. Need for Data-Centric ML Compiler Support for PIM

PIM software support remains in early stages, with limited automation and compilation frameworks. SimplePIM [32] optimizes only 1D tensor kernels on UPMEM PIM. PIM-DL [14] effectively supports only the GEMM kernel. CINM [33] integrates multi-level intermediate representations to lower abstractions to PIM, again targeting UPMEM. PIMFlow [34] supports only convolution kernels, automating kernel offloading to GPU or PIM, but without kernel-level tuning optimizations and largely ignoring data rearrangement costs. These works lack systematic optimization and auto-tuning for diverse ML kernels and support for multiple PIM backends. Moreover, most of them target UPMEM PIM, a CPU-integrated DDR4-based device that has no floating-point support. This makes UPMEM unsuitable for ML models, where compute-intensive kernels typically run on GPUs/TPUs and memory-intensive kernels on PIM cores may need floating-point arithmetic.

ATiM [31] is a search-based tensor compiler designed for UPMEM PIM. ATiM optimizes ML workloads on CPU-PIM systems, however, CPU-PIM co-execution typically performs worse than GPU-only execution [12], [13]. In contrast, GPU-PIM co-execution can deliver substantial performance benefits in ML [20], [25], [26], [29] over GPU-only. Although ATiM considers data rearrangement costs, it could not provide optimal performance due to its *compute-centric* tuning approach. ATiM has a three-step sequential process: (i) uses TVM [35] to find and fix a set of templates for compute code generation, (ii) generates data rearrangements needed for each template using UPMEM-specific optimizations, and (iii) searches within this *fixed* set of templates to find the best-performing configuration. This sequential approach is suboptimal because it treats compute code generation and data rearrangements as *independent* problems, while they are fundamentally *interdependent*. A compute schedule that appears efficient in isolation may require expensive data rearrangements, while a slightly less efficient schedule might enable cheaper data rearrangement costs, yielding better end-to-end performance. By fixing compute templates before generating data rearrangements, ATiM explores only a restricted search space and cannot discover configurations where alternative compute schedules paired with different data layouts could minimize total time.

Fig. 2 shows the breakdown of compute (step (2) in Fig. 1) and data rearrangement (steps (1) and (3) in Fig. 1) time for the Reduction and GEMV kernel running on a PIM system [20] (detailed in §V) using various matrix sizes, comparing a TVM-based [35] compilation approach against a manually-tuned best-performing implementation. For the TVM-based point, we tune TVM for Reduction and GEMV using performance profiling on the evaluated PIM backend. TVM selects the

best-performing compute code templates based on its cost model. For each template, we generate the optimized data rearrangements and measure end-to-end performance (compute plus data rearrangement). We present the configuration with the best performance among TVM’s selected templates. For the manually-tuned best-performing implementation, we manually selected some promising data partitioning strategies across PIM cores, and deploy optimized compute code for all of them. Then, we evaluate all of them and present the configuration that achieves the minimum total execution time.

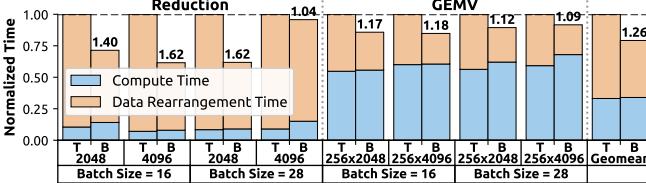


Fig. 2: Normalized breakdown of compute and data rearrangement time in Reduction and GEMV comparing TVM-based compilation scheme (**T**) and a manually-tuned best-performing end-to-end implementation (**B**), at various matrix sizes. The numbers on each bar show speedup of **B** over **T**.

We make two observations. First, the TVM-based approach has suboptimal performance, being on average $1.26\times$ worse than the manually-best implementation. This is because TVM approach is compute-centric: it selects compute code templates that minimize compute time, while largely ignoring data rearrangement costs. Consequently, data rearrangements contribute 64.68% of the total kernel time on average. Second, while the manually-tuned implementation has $1.09\times$ worse compute time than TVM-based approach, it reduces data rearrangement costs by $1.62\times$ compared to TVM-based scheme. It provides better trade-offs that result in better end-to-end performance. Overall, these results demonstrate that compute schedules and data rearrangements are *interdependent*, and optimal performance requires balancing both costs.

III. DCC: OVERVIEW

DCC is the first data-centric ML compiler for PIM architectures that *co-optimizes* data rearrangement strategies with compute code optimization in a unified tuning process. DCC supports diverse ML kernels and multiple PIM backends. Fig. 3 presents a high-level overview of DCC components. Users develop ML kernels using the DCC API, which enables execution on target PIM backends. At compile time, DCC analyzes ML kernels in the model and trains its coupled predictor. At runtime, once input tensor dimensions are known (e.g., token counts in LLMs), DCC uses its pre-trained coupled predictor to generate optimized schedules for all PIM-running kernels. The schedules orchestrate data loading to the target PIM backend, computation on PIM cores, and final output data with the appropriate layout. DCC has four components.

1. Multi-Layer Abstraction. We design a general multi-layer abstraction for near-bank PIM systems, where PIM cores form PIM groups, that enables DCC to reason about data distribution across memory banks and data processing on

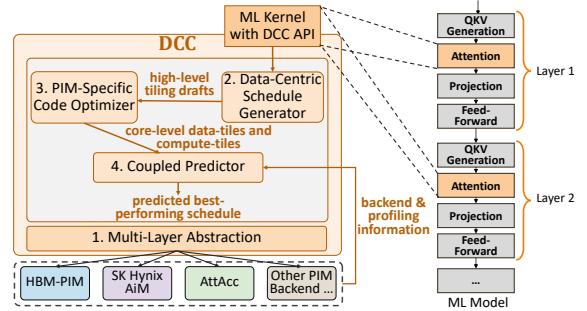


Fig. 3: DCC overview with multiple PIM backend support.

PIM groups and cores. Our abstraction (i) enables coarse-grained optimizations at the PIM group level and fine-grained optimizations at the PIM core level, and (ii) decouples the compiler from backend-specific semantics, allowing DCC to support multiple current and future PIM backends.

2. Data-Centric Schedule Generator. We follow a *data-first* scheduling strategy that first generates all candidate tensor data partitions across PIM resources, and then maps them to corresponding loop partitions in the compute code, creating *tiling drafts*. This approach enables effective *co-optimization* of data rearrangements with compute code.

3. PIM-Specific Code Optimizer. We further optimize data rearrangement and compute code performance of tiling drafts through two PIM-specific optimizations. This optimizer can be easily extended with additional backend-agnostic optimizations or backend-specific passes to create specialized compiler variants for particular PIM backends.

4. Coupled Predictor. We use a learning-based predictor that models the interdependence between data rearrangement costs and compute efficiency and selects the optimal configuration that minimizes end-to-end time. It can provide fast and accurate performance predictions on various PIM backends.

IV. DCC: DETAILED DESIGN

A. Multi-Layer Abstraction for Near-Bank PIM Architectures

To efficiently support multiple PIM backends, we introduce a **general multi-layer abstraction**, which maps the traditional memory hierarchy into a compute hierarchy, allowing DCC to configure where and how each ML tensor is distributed and processed, and cover various PIM backends [12], [16]–[30]. These PIM devices have similar logical organization: they place one PIM core (e.g., specialized acceleration or floating point unit) close to one or a few memory banks. Multiple PIM cores can form **PIM groups** (e.g., cores of the same memory channel or the same DRAM rank can form a group), and the memory bus controller of Host xPU can serve as a controller for all PIM groups. PIM devices may include specialized compute units for each PIM core group (Fig. 1) that can access data from multiple memory banks within the same PIM group. Although the PIM core may have different compute units across different PIM backends, the overall computational model remains consistent across PIM backends. Key differences lie primarily in hardware circuitry design and compute units placement rather than execution

semantics. Any current or future PIM system that satisfies our proposed multi-layer abstraction can be seamlessly supported by DCC for ML kernel acceleration. Our abstraction has three levels. There are two levels within PIM device.

(1) System Level. Our system-level PIM abstraction consists of three major components (see Fig. 1): the **Host xPU**, **Host memory space** and the **PIM devices**. The Host xPU (e.g., CPU, GPU, TPU) orchestrates global execution control, data rearrangements and kernel scheduling. PIM devices perform near-memory computation. The Host memory space is an address space that follows the Host-side data layout, accessible through standard DRAM commands (e.g., LD/ST). It maps to physical addresses in PIM-enabled or normal memory banks. **(2) PIM Group Level.** A PIM group represents multiple PIM cores (and their local memory banks) belonging to the same memory channel or rank, depending on the device architecture. A PIM group may include specialized compute units that access data from all banks within the group and/or buffers to temporarily store group-wide data. Each group is managed by the Host xPU memory controller, which may issue group-level instructions. A group-level instruction can be a read/write/compute command (i) that broadcasts to all cores within the group, typically using identical bank address offsets, or (ii) is executed by the specialized compute units of the group. In the latter case, the instruction may access data from shared group-wide buffers or merge partial results produced by PIM cores of the group. Each group has a dedicated memory bus to the Host xPU, enabling DCC to schedule *parallel* data rearrangements across multiple PIM groups. Host can coordinate global data movements across groups or between Host and PIM memory. By scheduling coarse-grained group-level instructions broadcast to all cores within a group, DCC can reduce instruction traffic on the memory controller, and enables parallel operations on the group’s cores.

(3) PIM Core Level. A PIM core represents the processing unit and its local memory bank(s). A core can be a SIMD unit or floating-point unit or any specialized compute unit. It may have a scratchpad memory or register files to temporarily store data for processing. If the Host memory space is mapped to PIM banks, a portion of each bank serves as Host memory, and the PIM backend provides address offsets for the PIM mapping. PIM cores are controlled via bank-level instructions or broadcast group-level instructions sent by the Host memory controller, or instructions stored in dedicated instruction memory per core. By scheduling fine-grained bank-level instructions that allow independent computation and data flow at cores, DCC enables optimizations on individual cores.

This abstraction enables a PIM device to operate under either group-level or bank-level control, providing a unified yet flexible interface for near-bank computation. It enables DCC to optimize at multiple granularities: coarse-grained at the PIM group level (e.g., effectively partitioning data across groups or scheduling computation on specialized units of a group) and fine-grained at the core level (e.g., optimizing memory access within a bank or local data layout and computation). Moreover, our abstraction decouples DCC from hardware-specific instruc-

tion semantics, thus enabling DCC to easily support multiple PIM backends that conform to this abstraction.

B. Data-Centric Schedule Generation

Traditional ML compilers [35]–[45] use loop transformations to divide computation into blocks, and improve data locality. DCC adopts a **data-first schedule** strategy that inverts this process: it first generates all candidate partitions of data tensors (called **data tiles**) across PIM groups and cores, then maps data tiles to their corresponding loop partitions in the compute code (called **compute tiles**), optimizes each tile’s performance, and finally uses its predictor to evaluate all data-compute tile mappings and selects the best-performing one.

To find the optimal data-compute schedule for a given kernel and hardware configuration, DCC generates a comprehensive set of **tiling drafts**, each representing a potential mapping between tensor sizes, computation loops, and PIM hardware resources. The generation process includes four stages shown in Fig. 4 for an example ML kernel and explained next.

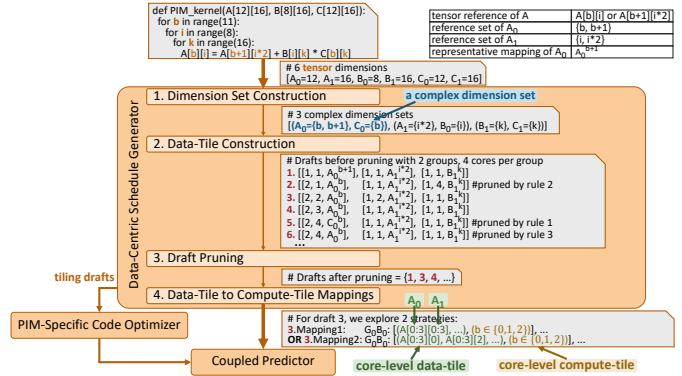


Fig. 4: Example schedule generation process for GEMV.

1. Dimension Set Construction. To jointly co-optimize compute-data, we need to correlate the data tensors with the compute code. For a k -dimensional tensor A , we map its dimensions A_0, A_1, \dots, A_k to the compute code: we leverage loop variables as intermediaries to associate tensor dimensions to indexing functions as *dimension sets*. Specifically, for a tensor A with tensor reference $A[b+1][i^*2]$, where A_0 is the first dimension and A_1 is the second dimension, we use the variables and constants to build mapping functions for each dimension: e.g., the mapping functions $F(b)=b+1$ and $F(i)=i^*2$ are for dimensions A_0 and A_1 , respectively. A tensor may have multiple tensor references in the compute code, e.g., tensor A in Fig. 4 has two references $A[b][i]$ and $A[b+1][i^*2]$, creating multiple mapping functions for the same tensor dimension. The dimension A_0 is associated with both $F(b)=b$ and $F(b)=b+1$. We build all mapping functions for each tensor dimension and collect them into a **reference set**. The reference set for dimension A_0 is $\{b, b+1\}$, and for A_1 is $\{i, i^*2\}$. The reference set for the tensor dimension C_0 is $\{b\}$, and for C_1 is $\{k\}$. When two or more tensor dimensions share the *same* loop variable in their reference sets, they are grouped into a **complex dimension set**. For example, dimensions A_0 and C_0 both contain variable b in their reference sets, so we

group them as ($A_0=\{b, b+1\}$, $C_0=\{b\}$) to be processed jointly, since these dimensions must share the same data tile and compute tiles. Tensor dimensions that do not share variables with any other dimension form simpler dimension sets.

2. Data-Tile Construction. We explore all candidate data tile options through exhaustive depth-first search with memoization to construct data tiles for each dimension set. For the i -th dimension set among n dimension sets, given k available PIM groups and m available cores per group, we try all possible PIM allocations, i.e., $[1, k]$ PIM groups and $[1, m]$ cores per group. The available PIM groups and cores for the $(i+1)$ -th dimension set are computed recursively as $\text{avail_resources}_{i+1} = \frac{\text{avail_resources}_i}{\text{allocated_resources}_i}$. Memoization caches all valid allocation solutions for each subproblem, enabling reuse when the same PIM resource configuration recurs during search. Once the allocation of PIM resources is done for all dimension sets, we create multiple tiling drafts as follows. Each draft has n parts, one for each dimension set. Each part includes three parameters: [the number of groups, the number of cores, a representative mapping]. The **representative mapping** is an assignment of a mapping function (e.g., $b+1$) to a tensor dimension (e.g., A_0). We create drafts via exhaustive search for all possible assignments of representative mappings for a given dimension set. For instance, in Fig. 4, the first draft has three parts for its three dimension sets. The first part is $[1, 1, A_0^{b+1}]$, which represents 1 PIM group, 1 core per group, and the representative mapping $A_0=b+1$. The second part $[1, 1, A_1^{i*2}]$ represents 1 group, 1 core per group, and the representative mapping $A_1=i*2$. Similarly, the third part is $[1, 1, B_1^k]$. When this step finishes, we have generated all possible tiling drafts for all possible data tiles.

3. Draft Pruning. DCC applies pruning rules to eliminate unpromising tiling drafts and reduce tuning time, while maintaining high performance. **Rule 1.** We remove redundant tiling drafts that have the same data tiles and equivalent representative mappings for all dimension sets. In Fig. 4, the 5th draft $[[2, 4, C_0^b], \dots]$ and the 6th draft $[[2, 4, A_0^b], \dots]$ are redundant. In their first part (relates to the first dimension set), they have the same data tile, i.e., 2 PIM groups and 4 cores per group, and equivalent representative mappings, i.e., their representative mappings C_0^b and A_0^b use the same mapping function $F(b)=b$, thus they relate to *identical* compute tile. The second and third parts of these tiling drafts are identical. Thus, one of these two drafts, i.e., the 5th draft, is removed. **Rule 2.** PIM backends [18], [20], [25], [27] support multi-data instructions (e.g., SIMD-style instructions) that enable PIM cores to fully leverage the large memory bandwidth available to their local bank(s). For example, HBM-PIM [18] supports 16-way SIMD instructions. In a PIM backend with d -way multi-data instruction support, the draft pruner speculatively eliminates drafts where the length of the dimension set assigned to a PIM core is not a multiple of d : these drafts cannot fully utilize the core's local bandwidth and hardware datapaths designed for d -way execution. In Fig. 4, let us assume a PIM backend with 16-way MUL instructions, and consider the dimension set ($B_1=\{k\}$, $C_1=\{k\}$) for the computation $B[i][k] \times C[b][k]$. The 2nd draft

allocates 4 cores to dimensions B_1 and C_1 that are both of size 16, resulting in 4 elements per core. Since 4 elements per core are not a multiple of the 16-way MUL instruction requirement, this draft is pruned. If all drafts fail to satisfy the d -way alignment requirement, or if the PIM backend does not support multi-data instructions, DCC skips this pruning rule. **Rule 3.** Within a PIM group, execution performance is primarily determined by the core of the group that performs worse. Thus, if there are drafts of multiple PIM groups and for each group they have the *same* worst per-core performance, only one draft needs to be kept, while others are pruned. To detect this, we quickly estimate the per-core performance for each PIM group of the tiling draft based on the *length* of the dimension set assigned to each core. Then, we keep the core with the largest length for a representative mapping as the worst performance for that group. If multiple drafts have the same worst performance for *all* their PIM groups, only one of them is kept. In Fig. 4, the 4th and 6th drafts have two groups for the first dimension set ($A_0=\{b, b+1\}$, $C_0=\{b\}$) and the largest length for the representative mapping of both groups in both drafts is the same: in the 4th draft is $\text{round}(\frac{A_0}{\text{groups} \times \text{cores}}) = \text{round}(\frac{12}{2 \times 3}) = 2$ and in the 6th draft is $\text{round}(\frac{A_0}{\text{groups} \times \text{cores}}) = \text{round}(\frac{12}{2 \times 4}) = 2$. The other dimension sets of 4th and 6th drafts also have the same per-core performance for all groups. Thus, one draft, i.e., the 6th draft is pruned.

4. Data-Tile to Compute-Tile Mappings. Once the drafts are pruned, DCC constructs core-level **data-tiles** and maps them to core-level **compute-tiles**. The current drafts include only the high-level tiling (number of groups, and cores per group) of the representative mapping of all dimension sets, but we need to (1) lower the high-level tiling to core-level data-tile, and (2) map the core-level data-tile to core-level compute-tile.

(1) For each dimension set, given the high-level tiling, we define the data-tile of a representative mapping for *each* core j of a PIM group i as $R_{G_i B_j}$. In Fig. 4, the first part of the 3rd draft $[2, 2, A_0^b]$ on the dimension set ($A_0=\{b, b+1\}$, $C_0=\{b\}$) has tiled size $\frac{A_0}{\text{groups} \times \text{cores}} = \frac{12}{2 \times 2} = 3$ for the representative mapping A_0^b . Thus, the data-tile on the first dimension set for the first PIM core B_0 of the group G_0 is $G_0 B_0 = A[0:3]$. We similarly calculate all data-tiles for all dimension sets for each core.

(2) For each dimension set, given the *core-level* data-tile of a representative mapping $R_{G_i B_j}$ and the assigned mapping function $F(b)$, we map the data-tile to compute-tile for each core by calculating the loop range of the variable b . The loop range is a set that includes all the values of b that satisfy $F(b) \in R_{G_i B_j}$. In Fig. 4, for the 3rd draft with the $R_{G_0 B_0}$ from step (1) and the mapping function $F(b)=b$, the loop range of the variable b is $\{0, 1, 2\}$. Similarly, we calculate all loop ranges for all variables as the compute-tiles for all cores.

Once the compute-tile for each core is determined, DCC finds all necessary data indices of all tensors at core-level by iterating through loop variable values. When necessary indices of a tensor are non-contiguous in a dimension, DCC finalizes the necessary tensor data using two alternative strategies:

(i) expands the data indices of this dimension to cover a contiguous range, adding the missing or straddling values (e.g., in Fig. 4 in 3.*Mapping1* the indices of A_1 is expanded from $\{0, 2\}$ to $[0:3]$), and (ii) keeps only the necessary indices (e.g., in 3.*Mapping2* the index set of A_1 is $\{0, 2\}$ and is kept as it is). These two alternative approaches are two different possible distribution strategies for the irregular indices, so that DCC selects the best-performing distribution strategy.

C. PIM-Specific Code Optimizer

Once tiling drafts are generated, data has been mapped across PIM banks and compute loop partitions have been mapped to PIM cores. DCC then applies a **PIM-specific code optimizer** for *each* tiling draft that further optimizes data rearrangements and compute code execution, exploiting common architectural characteristics of PIM systems.

I) Data Rearrangement Optimization. Host and PIM devices require different data distributions to achieve high performance. In Host memory, contiguous data needs to be distributed across multiple memory channels to exploit channel-level parallelism. For example, on a two-channel CPU, a 1KB block is divided into 16 cache lines (indexed 0-15), with odd-indexed lines routed to one channel and even-indexed lines to the other channel. This enables *parallel* sequential reads across multiple memory channels. Instead, PIM devices require contiguous data to be stored in a single memory bank, i.e., using one single memory channel for writes, since each PIM core can only process data stored in its local bank(s). This creates the following data movement challenge: (i) reading contiguous data sequentially from Host memory exploits Host channel parallelism, but writes to only one PIM memory channel, underutilizing PIM bandwidth, while instead (ii) using multiple PIM channels for parallel writes requires simultaneous reads from *non-contiguous* Host addresses, potentially causing Host channel conflicts and degrading read performance. To enable channel parallelism for both Host reads and PIM writes, DCC exploits controllable on-chip memory (e.g., GPU shared memory) to reorganize data within the Host. For a PIM device with N channels, the compiler calculates the data block size as $B = \frac{\text{on-chip memory size}}{N}$. DCC then serially reads N blocks of size B from Host memory to on-chip memory, followed by parallel write operations that distribute these blocks across all N PIM channels simultaneously. This approach transforms data movement into N sequential read operations from Host channels and N parallel writes to PIM channels, leveraging channel parallelism in both reads and writes. If there is no controllable on-chip memory in the system (e.g., on CPUs), DCC performs data rearrangement using the PIM backend's default data copy or DMA interfaces. For PIM backends with specialized layout constraints (e.g., alignment or interleaving requirements), DCC apply additional reorganization passes.

II) Compute Code Optimization. PIM backends [16]–[18], [20] can use specialized DRAM commands to control computation. However, when all PIM cores need to perform computation in parallel, the Host memory controller must issue significantly more commands than in conventional DRAM. The

limited memory bus bandwidth and the controller constrain the number of commands that can be issued per cycle, creating a control bottleneck. To address this, PIM backends [16]–[18], [20] introduce group-level commands that provide SIMD-style control, issuing a single command to all cores within a group. DCC employs a hierarchical command generation strategy leveraging both **group-level** and **bank-level** control to balance efficiency and flexibility. DCC prioritizes **group-level commands**, which broadcast a single command across all PIM cores in a group. Since DRAM command formats constrain group-level commands to use identical address offsets for all cores in the group, DCC pads each core's tensor data to the same size, ensuring consistent local addressing. This way we allow the memory controller to issue one command per PIM group, significantly reducing command traffic. If the backend lacks group-level command support or when cores need to access different address offsets, DCC generates *parallel bank-level commands*, achieving fine-grained, bank-level parallelism. This hierarchical command generation strategy adapts to different PIM backends, and minimizes command traffic.

Our optimizer applies PIM-specific optimizations that accelerate performance, while it remains backend-agnostic. It has a modular design that allows easy extension to support additional optimizations common across PIM backends. Developers can extend DCC with custom optimization passes tailored to specific PIM backends, creating specialized compiler variants (e.g., DCC +HBM for HBM-PIM-specific optimizations).

D. Coupled Predictor

Although pruning substantially reduces the search space, the schedule generator can still produce thousands of valid tiling drafts. Profiling all drafts on PIM system can be prohibitively expensive. To efficiently identify the optimal draft, DCC employs a **coupled learning-based performance predictor** that estimates end-to-end execution time. The coupled predictor serves two purposes: (i) co-estimating data rearrangement and compute costs to find the optimal tiling draft, and (ii) providing fast and accurate predictions across multiple PIM backends. While analytical models can achieve sufficient accuracy with device-specific formulas and parameters, they are difficult to maintain as PIM architectures evolve. Instead, learning-based models (already effectively adopted by widely-used ML compilers [35], [46], [47]) can be easily retrained or fine-tuned for new hardware with minimal adaptation, and provide both high speed and accuracy. We use an XGBoost model [48] to predict end-to-end kernel time, leveraging XGBoost's proven efficiency in compiler cost modeling [35], [46], [47].

The coupled predictor supports both static and dynamic tensor sizes. For static sizes, the most common case, where model and input dimensions are fixed during inference, DCC trains the predictor offline (similarly to prior ML compilers [35], [46], [47]) and configures the best-performing draft during model initialization. For dynamic inputs, which occur in language models, DCC finds and selects optimal drafts at inference time. **Offline Training:** Given model-defined or user-provided tensor sizes, DCC samples a diverse subset of drafts across different

tensor sizes from the schedule generation step. Each draft is profiled on the target PIM backend to measure execution time as labels, with drafts’ configurations and backend information as inputs to the XGBoost model. After training, DCC predicts performance for all drafts at given tensor sizes of ML kernels and records the best-performing draft in a lookup table. When multiple drafts have identical predicted performance, one is selected randomly. This training occurs *once* per PIM backend using given ML models and tensor sizes. Offline training for all ML kernels across all tensor sizes, ML models, and PIM backends used in our evaluation takes only \sim 42 seconds. This cost is negligible and is amortized across multiple users’ inference requests for that ML model. At runtime, DCC *directly* uses the best-performing draft for recorded tensor sizes.

Dynamic Prediction: When a new tensor size appears during inference, DCC generates the corresponding tiling drafts and uses the predictor to estimate performance, recording the best-performing draft in the lookup table for future use. In ML models with dynamic tensor sizes, e.g., evaluation of LLMs in Fig. 8, the cost to generate drafts on-the-fly and estimate performance is accounted for in total time. Optionally, DCC can support training the predictor at inference time: it can profile a small batch of new drafts, and use the (updated) predictor to estimate performance for remaining drafts.

E. DCC Integration and Programming Interface

DCC provides a Python interface with PyTorch to develop, integrate and compile PIM-running kernels into ML models, as described in Table I. A DCC kernel is defined as a Python function with the `@DCC_kernel` annotator. All parameters and return values must be PyTorch tensors or constants. The function body describes the tensor computation using for loops with arithmetic operators or backend-supported instructions. DCC provides `DCC.Tensor()` and `DCC.Tensor.zero()` to create and initialize temporary tensors.

Interface	Description
<code>@DCC_kernel</code>	Annotator to define PIM-running kernels.
<code>DCC.Tensor</code>	Tensor class used in kernel. It can be converted to <code>torch.Tensor</code> .
<code>DCC.Layer</code>	Class to define a new PIM-running layer.
<code>DCC.Kernel</code>	Class to represent a PIM-running kernel.
<code>DCC.init_kernel()</code>	Function to initialize the kernel for given input sizes. It returns a <code>DCC.Kernel</code> object.
<code>DCC.Kernel.update()</code>	Function called when the best tiling draft has been determined.
<code>DCC.Kernel.pre_load()</code>	Function to load data to PIM devices and return a PIM address. It also supports partial updates of tensors in PIM memory with address offset.
<code>DCC.Kernel.run()</code>	Function to execute a PIM-running kernel with <code>torch.Tensor</code> or PIM address.
<code>DCC.set_model()</code>	Function to register the model and extract model-level metadata necessary for tuning.

TABLE I: The DCC Programming Interface.

To integrate a PIM-running kernel into an ML model, users can create ML layers with `DCC.Layer` to replace existing model layers. PIM-running kernels must be initialized with given input tensor sizes. After adding PIM layers to the model,

DCC initializes necessary model metadata, infers all tensor sizes, and performs offline training. During inference, when a request is received, DCC asynchronously infers tensor sizes for all PIM-running kernels and selects their best-performing drafts. Users can override the function `DCC.Layer.update()` to pre-load data to PIM devices using `DCC.Kernel.pre_load()` before running the kernel. When `forward()` is called, the PIM-running kernel is executed with input data and returns the results as a `torch.Tensor`. DCC synergistically works with xPU compilers (e.g., ML compilers [35], [37] for GPUs) via PyTorch. During the optimization for xPU, the PIM layer will be configured as non-fusible to enable intra- and inter-kernel optimizations. Then, DCC will compile and optimize this layer for the PIM backend.

Fig. 5 shows an example of replacing the QKV generation layer in GPT-3 13B model with a PIM-running layer. Lines 1-8 define the PIM-running kernel with for loops. Line 10 creates class `QKV_Layer` inheriting from the `torch.nn.Module` and `DCC.Layer`. In lines 11-14, DCC initializes the kernel and model parameters. Lines 16-18 pre-load weights and bias to PIM devices after having selected the best-performing draft. Line 21 executes the kernel with a given input and pre-loaded data. Lines 23-28 replace the original QKV layer in the loaded GPT-3 model and handle inference requests.

```

1 @DCC_kernel
2 def PIM_kernel(weight, bias, x): # define PIM kernel
3     y = DCC.Tensor.zero([x.size(0), weight.size(0)])
4     for b in range(y.size(0)):
5         for i in range(y.size(1)):
6             for j in range(x.size(1)):
7                 y[b][i] += x[b][j] * weight[i][j] + bias[j]
8     return y
9
10 class QKV_Layer(torch.nn.module, DCC.Layer):
11     def __init__(self, layer, input_sizes): # init kernel and weight
12         self.kernel = DCC.init_Kernel(PIM_kernel, input_sizes)
13         self.weight = layer.weight
14         self.bias = layer.bias
15
16     def update(self, best_draft): # pre-load data
17         self.PIM_W = self.kernel.pre_load(best_draft, self.weight)
18         self.PIM_b = self.kernel.pre_load(best_draft, self.bias)
19
20     def forward(self, x): # execute PIM kernel
21         return self.kernel(self.PIM_w, self.PIM_b, x)
22
23 model = torch.load("GPT3-13B.model") #load model
24 in_sizes=[[model.qkv_0.weight.sizes(), model.qkv_0.bias.sizes(),
25            [1, model.hidden_size]]]
26 model.qkv_0 = QKV_Layer(model.qkv_0, in_sizes) # replace QKV layer
27 model = DCC.set_model(model) # collect model infomation
28 output = model(get_request()) # run the inference

```

Fig. 5: An example of adding DCC kernels to a GPT3 model.

V. EVALUATION

Simulation Methodology. We modify and use the open-sourced AttAcc simulator [20] with Ramulator 2.0 [49]. We evaluate data movement costs to/from PIM devices using DRAM commands (i.e., LD/ST) simulated in Ramulator 2.0. We modified the simulator to support both AttAcc and HBM-PIM with its corresponding DRAM compute commands [18]. We simulate a heterogeneous platform with a NVIDIA A100 GPU and 5 PIM-enabled HBM devices, corresponding to 80GB GPU memory. We evaluate HBM3 memory with

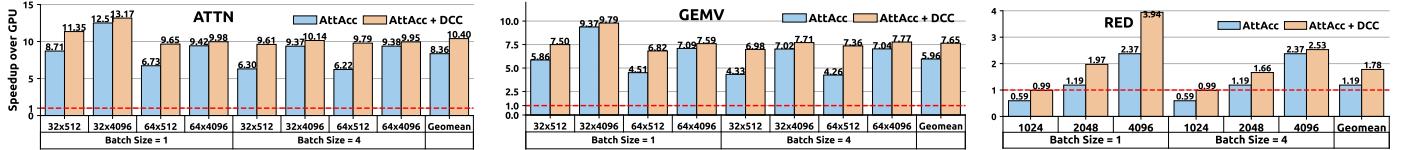


Fig. 6: Speedup of AttAcc and AttAcc+DCC over GPU for ATTN, GEMV and RED kernels, when varying the tensor sizes.

5.2Gbps per pin and running at 333MHz. Each HBM has 16 pseudo-channels and 64 banks per pCH. In AttAcc, each bank is equipped with a GEMV unit and each channel has a softmax unit. In HBM-PIM, every two banks share a 16-way FP16 FPU and two 16×256 -bit GRF registers (one per bank).

ML Kernels and Models. We evaluate seven memory-intensive ML kernels. In AttAcc, we evaluate the general-matrix-vector-multiplication (GEMV), reduction (RED) and attention (ATTN) kernels. In HBM-PIM, we evaluate the GEMV, RED, vector addition (VA) and RELU kernels. Attention requires a softmax unit which only exists on AttAcc. However, AttAcc does not have near-bank compute units that could support and run RELU and VA. For GEMV and ATTN, we use input size 128, the most common per-head dimension in LLMs. We also evaluate end-to-end inference using GPT3-13B and LLAMA2-33B models. We evaluate FP16 data type.

Comparison Points. We evaluate five comparison points. (1) **GPU:** all kernels are running on GPU cores. (2) **AttAcc:** AttAcc’s [20] default open-source implementation that distributes different batches or attention heads across 16 channels, partitions the first tensor dimension across 16 bank groups per channel, and partitions the second tensor dimension across 4 banks per bank group. (3) **AttAcc+DCC:** we enable DCC compiler on AttAcc backend. (4) **HBM-PIM:** we use AttAcc’s data distribution and processing assignment. (5) **HBM-PIM+DCC:** we enable DCC compiler on HBM-PIM backend. We trained the predictor with 5000 iterations with learning rate of 0.1 for offline training. The offline draft generation, training and prediction for all evaluated kernels take ~ 42 seconds in total.

A. ML Kernel Performance

Fig. 6 shows the speedup of AttAcc and AttAcc+DCC over the GPU baseline in various ML kernels, when varying the batch size, number of heads and tensor sizes.

We make three key observations. First, AttAcc significantly outperforms GPU across all kernels, achieving $10.4\times$ speedup for ATTN, $7.65\times$ for GEMV, and $1.78\times$ for RED on average. AttAcc leverages high aggregate PIM bandwidth and integrates specialized units (GEMV, softmax, and accumulator) that provide hardware-level support for these operations. Second, DCC provides further performance improvements over AttAcc: $1.24\times$, $1.28\times$, and $1.50\times$ average speedup, and up to $1.57\times$, $1.73\times$, and $1.66\times$ peak speedup for ATTN, GEMV, and RED kernels, respectively. Notably, for RED with tensor size 1024, AttAcc underperforms GPU by $0.59\times$, while with DCC achieves almost same performance with GPU. Third, with DCC performance scales well in RED as tensor size increases. In RED, data rearrangement costs dominate the total time (see Fig. 10) and with larger tensor sizes, DCC explores a larger

search space, allowing it to more effectively optimize data rearrangement costs. In RED with batch size 1 and tensor size 4096, DCC provides a large speedup of $3.94\times$. Overall, DCC significantly accelerates end-to-end time on the state-of-the-art AttAcc backend by up to $13.17\times$ ($5.75\times$ on average) over GPU across diverse ML kernels, batch and tensor sizes, thanks to its comprehensive data-compute co-optimization.

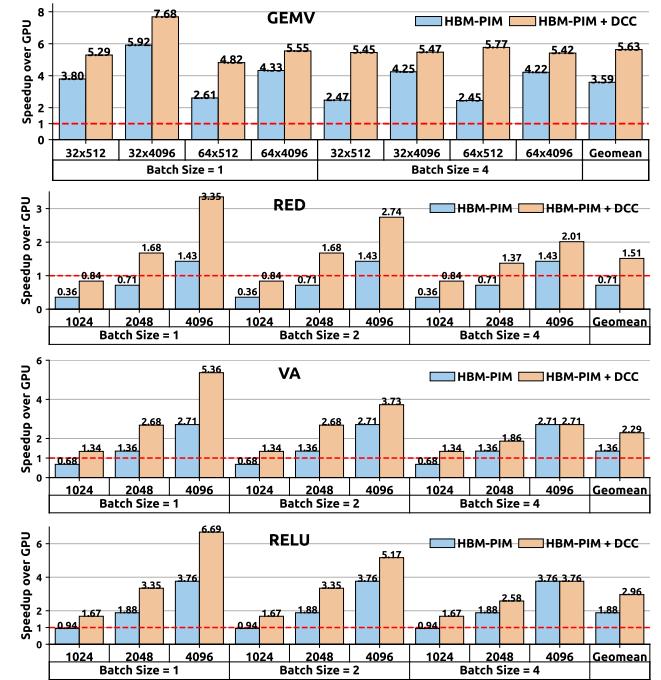


Fig. 7: Speedup of HBM-PIM and HBM-PIM+DCC over GPU for GEMV, RED, VA and RELU, varying the tensor sizes.

Fig. 7 shows the speedup of HBM-PIM and HBM-PIM+DCC over GPU in various ML kernels, when varying the batch size and tensor sizes. We make three key observations. First, DCC significantly improves HBM-PIM performance by $1.57\times$, $2.11\times$, $1.69\times$, and $1.58\times$ for GEMV, RED, VA, and RELU on average, respectively, enabling HBM-PIM to further outperform GPU by $5.63\times$, $1.51\times$, $2.29\times$, and $2.96\times$, respectively. Second, when using the same batch and tensor size configurations for both HBM-PIM and AttAcc in GEMV and RED, DCC achieves $1.57\times$ and $2.11\times$ average speedup over HBM-PIM, respectively, and $1.28\times$ and $1.50\times$ average speedup over AttAcc, respectively. DCC provides greater performance improvements on HBM-PIM than on AttAcc, because HBM-PIM is less optimized in hardware than AttAcc for GEMV, i.e., HBM-PIM includes general SIMD units, while AttAcc has specialized GEMV units. Third, for RED with tensor sizes 1024 and 2048, HBM-PIM underperforms

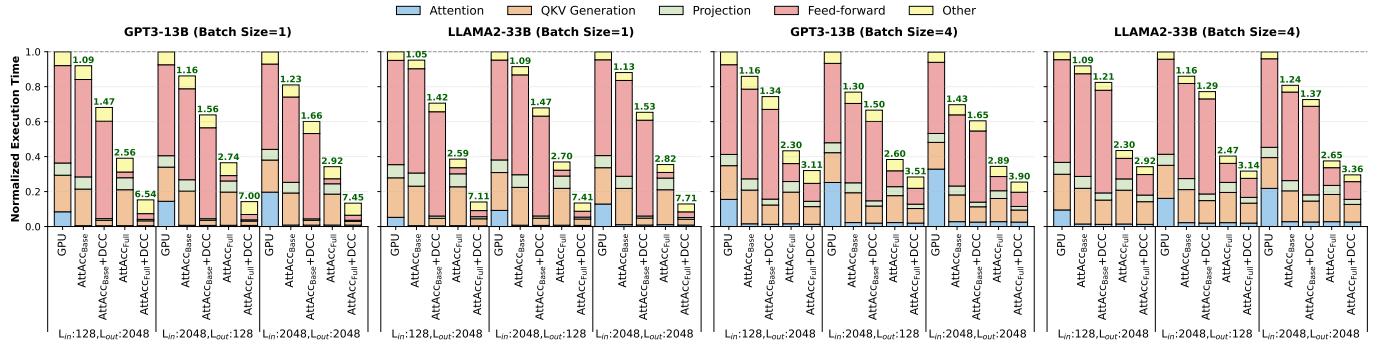


Fig. 8: Normalized time breakdown for GPT3-13B and LLaMA2-33B models for various input, output token and batch sizes.

GPU by 0.51 \times averaged across all batch sizes, because the combination of small tensor sizes and HBM-PIM’s fixed tiling scheme results in poor SIMD utilization: the per-core tensor partition size does not align with the 16-way SIMD instruction width. However, DCC improves their performance by 2.27 \times on average, enabling HBM-PIM to outperform GPU at tensor size 2048. Overall, DCC demonstrates robustness across multiple PIM backends through its multi-layer PIM abstraction, providing consistent performance improvements across diverse ML workloads on both HBM-PIM and AttAcc.

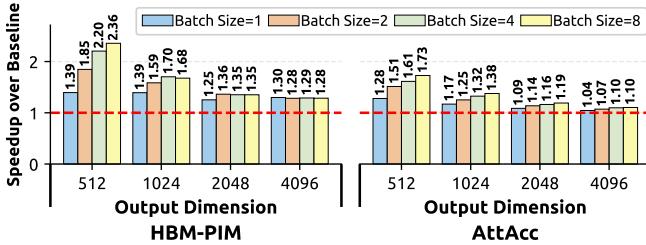


Fig. 9: Speedup of DCC over HBM-PIM (left) and AttAcc (right), when increasing the batch size in the GEMV kernel.

Fig. 9 shows the speedup of DCC over HBM-PIM and AttAcc, when increasing the batch size in GEMV, evaluating in an attention layer with head count 32, input size 128 and various output sizes. In both PIM backends, DCC improves performance over the baseline as the batch size increases. On average, DCC performance gains increase with batch size, from 1.33 \times to 1.61 \times on HBM-PIM, and from 1.14 \times to 1.33 \times on AttAcc, as batch size grows from 1 to 8.

B. End-to-End LLM Inference

Fig. 8 presents the normalized execution time breakdown of AttAcc and AttAcc+DCC over GPU for the main computational phases in inference of two state-of-the-art models, while varying the input and output token sizes and batch sizes. We evaluate two variants: AttAcc_{Base} runs only attention layers on PIM, and AttAcc_{Full} runs attention layers and a portion of the Feed-forward on the PIM side (See [20]), while the largest portion of Feed-forward runs on GPU. For both AttAcc variants, QKV generation, projection and Other run on GPU. However, with DCC’s optimizations, we enable QKV generation and projection to be also executed on the PIM side,

achieving performance benefits over running them on GPU. In LLM inference, DCC initializes the kernels with few random requests, then generates tiling drafts on-the-fly for new tensor sizes; this generation time is included in our measurements. The numbers in the top of each bar show speedup over GPU.

We make three key observations. First, DCC provides high performance benefits on both AttAcc_{Base} and AttAcc_{Full} by 1.24 \times and 1.86 \times on average, respectively, improving performance over GPU by 1.45 \times and 4.88 \times on average, respectively. DCC significantly strengthens AttAcc, enabling it to substantially outperform GPU across different models and token sizes. Second, DCC improves performance on Attention layers by on average 1.12 \times and 1.16 \times over AttAcc for GPT3-13B and LAMMA2-33B model, respectively. AttAcc uses a fixed tiling strategy across all token counts and batch sizes, while DCC adapts tiling strategies to different workload configurations. Third, in QKV generation and projection layers, DCC achieves 3.21 \times and 3.61 \times speedup over GPU, respectively. In both AttAcc variants, these layers run on GPU, because AttAcc’s fixed tiling strategy underperforms GPU by 1.25 \times in these layers. In contrast, DCC comprehensively explores the data-compute co-optimization space to identify optimal tiling configurations, enabling these layers to run efficiently on PIM and significantly outperform GPU. Overall, we conclude that DCC provides significant performance benefits in various state-of-the-art LLMs with different token count and batch sizes. These results demonstrate that DCC can serve as a practical and effective compiler for heterogeneous ML acceleration on high-performance processors (e.g., GPUs) and PIM backends.

C. ML Kernel Time Breakdown

Fig. 10 shows the normalized time breakdown split into time spent on *compute* and *data rearrangements* for various ML kernels using two batch sizes, and two different backends with and without DCC. The numbers above bars show the speedup provided by DCC. The execution time is normalized to that of the respective PIM backend with its default implementation.

We draw two findings. First, DCC co-optimizes both compute time and data rearrangement time, providing 1.73 \times and 1.79 \times speedup, respectively. DCC comprehensively explores a broader joint optimization space, and identifies the optimal balance between data movement and computation costs. Second, DCC provides larger performance benefits in ML kernels,

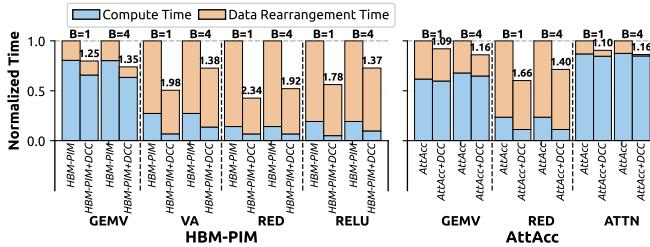


Fig. 10: Normalized time breakdown of compute and data rearrangement time in various ML workloads and backends.

where data rearrangement dominates execution time. The VA, RED, RELU kernels exhibit substantial data rearrangement overheads, and DCC accelerates them by $1.70\times$ on average, while it accelerates the compute-heavy GEMV and ATTN kernels by $1.18\times$. These results indicate that DCC significantly alleviates data rearrangement bottlenecks in PIM, while also effectively integrating compute-specific optimizations.

D. Coupled Predictor Accuracy

We run various ML kernels on HBM-PIM and AttAcc with hundreds of different tensor and batch sizes per kernel, representative configurations found on real ML models. For each workload configuration, we use DCC (pruning disabled) to exhaustively generate all tiling drafts, execute all of them on the target PIM backend, and identify the actual best-performing draft. Table II compares the predictor’s selections against the true optimum drafts. The *Total* column shows the number of workload configurations tested per kernel. The *#Best* column shows how many cases the predictor correctly identified the true optimum draft. The *Suboptimal Performance* column shows the geometric mean performance degradation in cases where the predictor selects a suboptimal draft. Our learning-based predictor achieves 89.28% accuracy in correctly identifying the true optimum draft. When suboptimal, the predictor’s selections achieve 96.25% of true optimal performance on average across different kernels, workloads and backends. In AttAcc+ATTN, they have relatively lower accuracy (74.63%), because ATTN fuses GEMV and softmax as a single kernel, however DCC still provides high performance (97.4% of true optimum). Our results demonstrate that even when the predictor fails to identify the true optimum, the selected configuration has negligible performance degradation.

Backend+Kernel	Total	#Best	Suboptimal Performance
AttAcc+ATTN	272	203	97.04% (69 cases)
AttAcc+GEMV	304	290	97.01% (14 cases)
AttAcc+RED	167	155	94.01% (12 cases)
HBM-PIM+GEMV	304	265	95.84% (39 cases)
HBM-PIM+RED	167	154	96.43% (13 cases)
HBM-PIM+VA	167	158	94.94% (9 cases)
HBM-PIM+RELU	167	157	94.48% (10 cases)

TABLE II: Prediction accuracy and performance slowdown of DCC predictor across various ML workloads.

VI. RELATED WORK

To our knowledge, this is the first work to (i) consider data rearrangement strategies and their associated costs during ML

kernel tuning for xPU-integrated PIM devices, and (ii) propose a compiler that co-optimizes them jointly with compute code to minimize end-to-end ML kernel performance.

Compiler Support for PIM. Prior works [14], [32]–[34] design compilation tools for PIM architectures, but lack systematic optimization and auto-tuning capabilities: they target one single ML kernel or are tailored for a single PIM backend. ATiM [31] is a search-based tensor compiler for UPMEM PIM. However, UPMEM’s DDR4-based architecture targets CPU memory channels, thus preventing GPU-PIM co-executions for ML models, and lacks hardware support for floating-point arithmetic. Moreover, ATiM has a *compute-centric* tuning approach that generates data rearrangement strategies **in isolation** from compute code generation. Such compute-centric process yields sub-optimal performance (See § II-B). Instead, DCC has a *unified data-centric* approach that **co-optimizes** compute-data to minimize end-to-end time.

Compiler Support for PUM. OptiPIM [50], MVE [51], and TCCIM [52] are compilation approaches for Processing-Using-Memory (PUM) architectures. PUM architectures are analog-based and have higher hardware design complexity than PIM devices (digital-based). Moreover, PUM systems may not have full precision accuracy in ML workloads.

ML Compilers for GPUs. ML compilers [35]–[45] designed for GPUs cannot be directly used for PIM systems. They can work synergistically with DCC to accelerate ML inference via GPU-PIM co-execution.

PIM Architectures and Accelerators. UPMEM PIM [12], [19] DDR4-based device for CPUs lacks a complete 32×32 -bit integer multiplier and floating-point units, making it unsuitable for our target ML workloads. Samsung HBM-PIM [18] and SK Hynix GDDR6-AiM [16], [17] are 3D memory devices with floating-point units, can be integrated with GPUs, and have been validated in real systems. Numerous research works [20]–[30] enhance near-bank PIM devices to support critical ML primitives (e.g., GEMV, ReLU, Softmax), can be integrated with xPUs, and have floating-point capabilities. DCC can be directly used on them to automate and accelerate ML kernels. Near-rank PIM systems [53]–[56] place cores at the buffer chip of the DIMM with access to all banks. Despite different core placement, DCC can effectively support near-rank PIM designs for ML. Recent works propose hybrid near-rank and near-bank designs [57]–[59] and NPU-integrated PIM devices [60]–[65]. DCC can be easily extended to support them thanks to its multi-layer abstraction. Finally, prior works [54], [66]–[76] design application-specific PIM devices for graph analytics, sparse computations, or data retrieval. While DCC may benefit some kernels in these devices, we mainly focus on xPU-integrated PIM designs that primarily target ML kernels and models.

Software for PIM Systems. Prior works [11], [12], [77]–[91] propose libraries, frameworks, and benchmark suites for the UPMEM PIM spanning linear algebra, graph processing, image processing, machine learning, databases, and concurrent data structure domains. UPMEM PIM is primarily designed for CPUs and has limited hardware multiplication support. DCC is designed for PIM devices that efficiently support ML kernels.

Communication and System Integration for PIM. Prior works [10], [92]–[101] design efficient data transfers, memory management, synchronization, virtualization of PIM, and simulation tools. PIMCARE [97] is a compiler-assisted scheduler to allocate the correct amount of PIM devices for a target application.

VII. CONCLUSION

We observe that Host xPU processor and PIM cores require different data layouts to fully leverage their respective memory bandwidth, necessitating data rearrangements that pose significant performance and programmability challenges. We also find that compute code optimization and data rearrangements are interdependent, requiring joint optimization for efficient ML kernel execution on PIM devices. To this end, we design DCC, a data-centric ML compiler for PIM systems. DCC *co-optimizes* compute code and data rearrangement strategies in a unified tuning process to minimize end-to-end execution time. Our evaluations across diverse ML kernels demonstrate that DCC significantly improves performance on HBM-PIM up to 7.68 \times speedup (2.7 \times average) over GPU and on AttAcc up to 13.17 \times speedup (5.75 \times average) over GPU in ML kernels. DCC on AttAcc accelerates end-to-end LLM inference up to 7.71 \times speedup (4.88 \times average). We hope our work encourages further research on compilation tools for ML kernels on PIM systems. We hope our work encourages further research on compilation and performance tuning tools to improve programmability and performance for emerging ML operators and models on PIM architectures.

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