



Ahsanullah University of Science and Technology (AUST)
Department of Computer Science and Engineering

Course No: CSE 3110

Course Title: Digital System Design

Submitted To- Md. Raqibul Hasan & Anika Rahman

Date of Submission - 05/02/2023

Submitted By-
Lab Group – 03(A2)

Aurprita Mahmood(20200104035)
Meherin Sultana(20200104036)
Sumaiya Shejin(20200104043)
Yasir Arafah Prince(20200104042)
Ziyan Shirin Raha(20200104033)

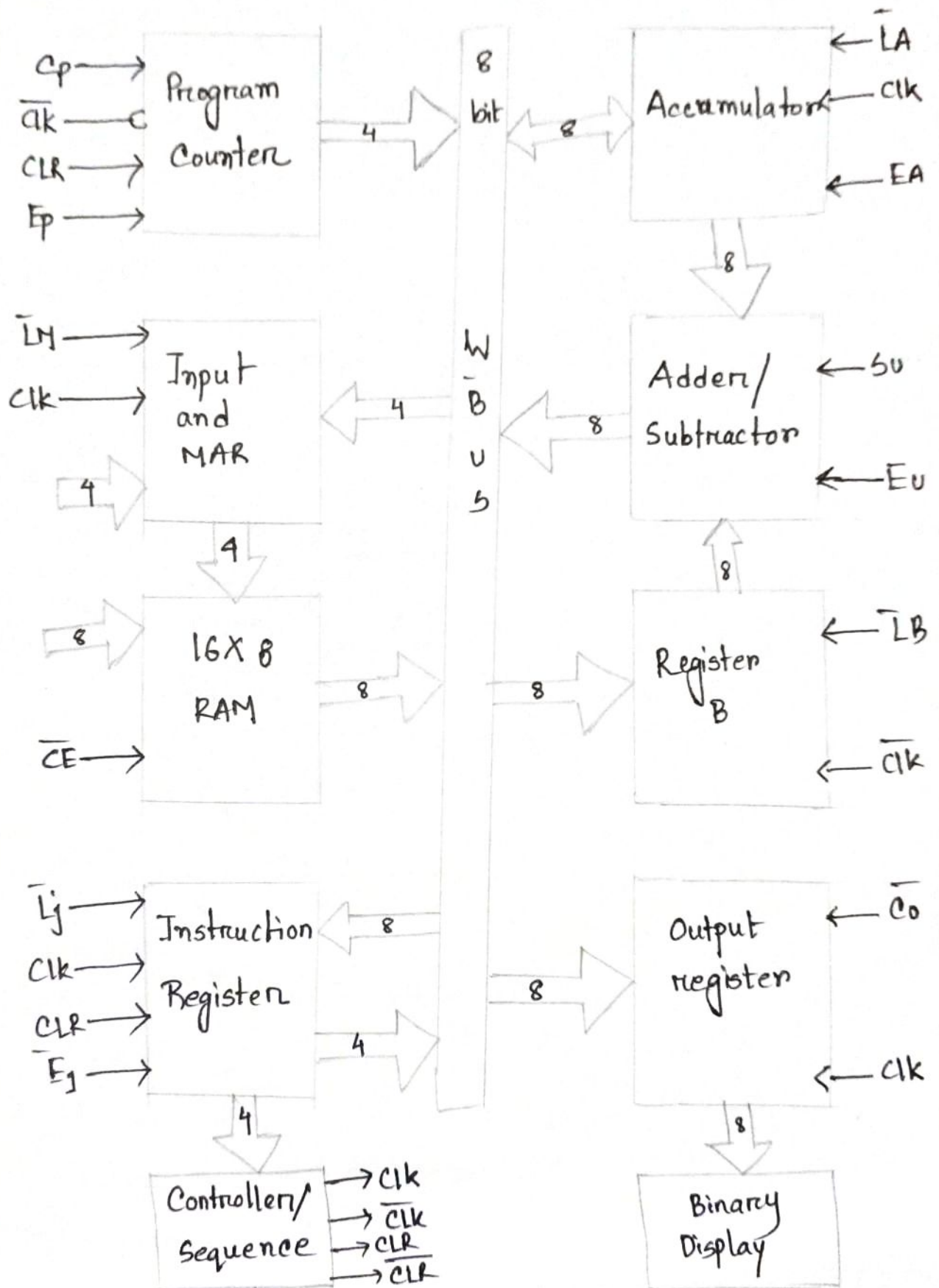
Year- 3rd
Semester- 1st
Section- A

Department- CSE

Name of the Experiment : Implementation of SAP-1.

Introduction : SAP-1 is the first stage in the evolution towards modern computers. The main purpose of SAP is to introduce all the crucial ideas behind computer operations. Being a simple computer, SAP-1 also covers many advanced concepts. SAP-1 is a bus organized computer. All registers are connected to W bus with the help of tri-state buffers. The abbreviation of SAP is 'simple as possible'.

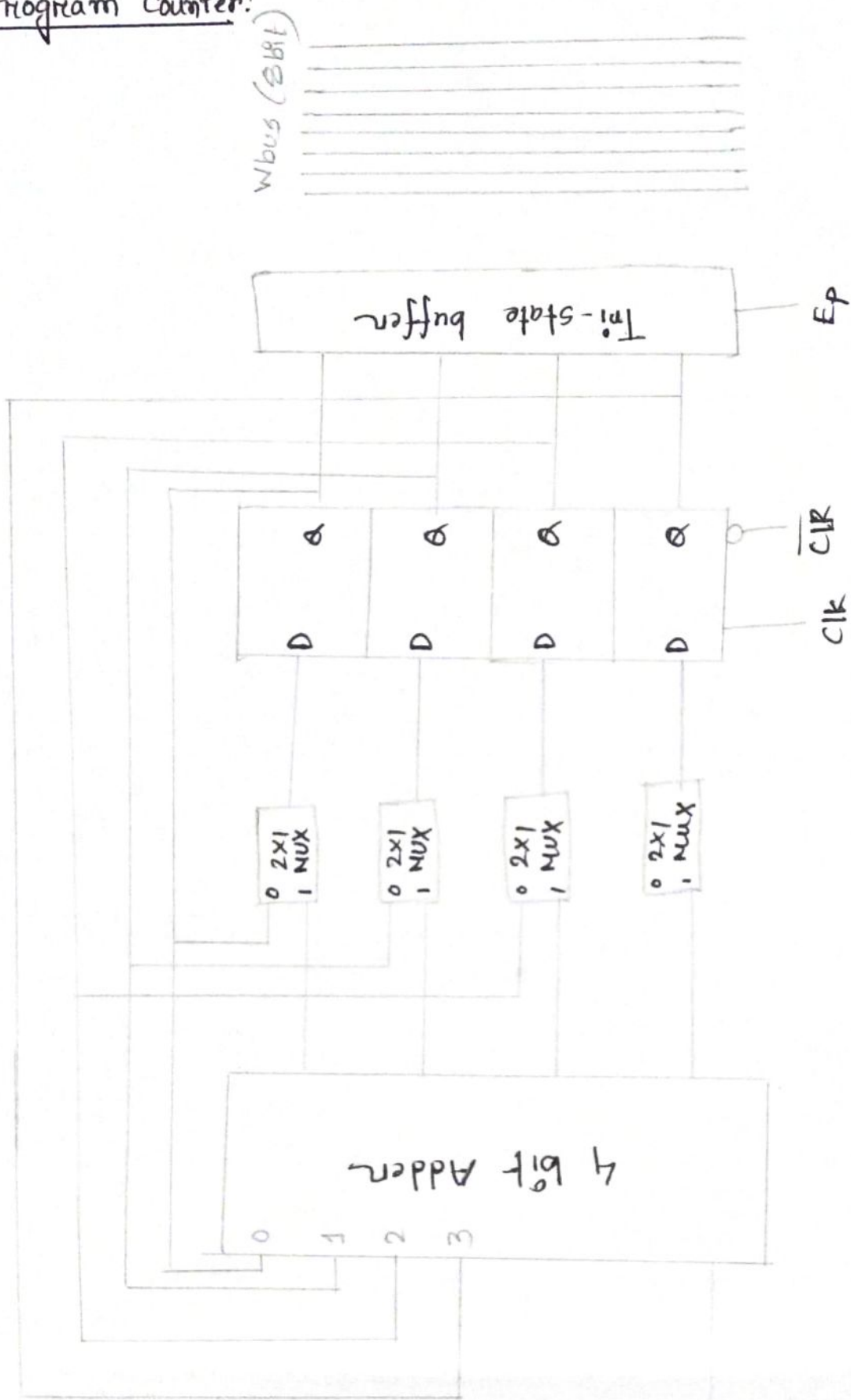
Block Diagram :



$C_p, E_p, \overline{L_M}, \overline{CE}, \overline{L_j}, \overline{E_j}, \overline{L_A}, E_A, S_u, E_u, \overline{L_B}, \overline{L_o}$

Fig- Sap-1

Program Counter:



Memory Address Register (MAR):-

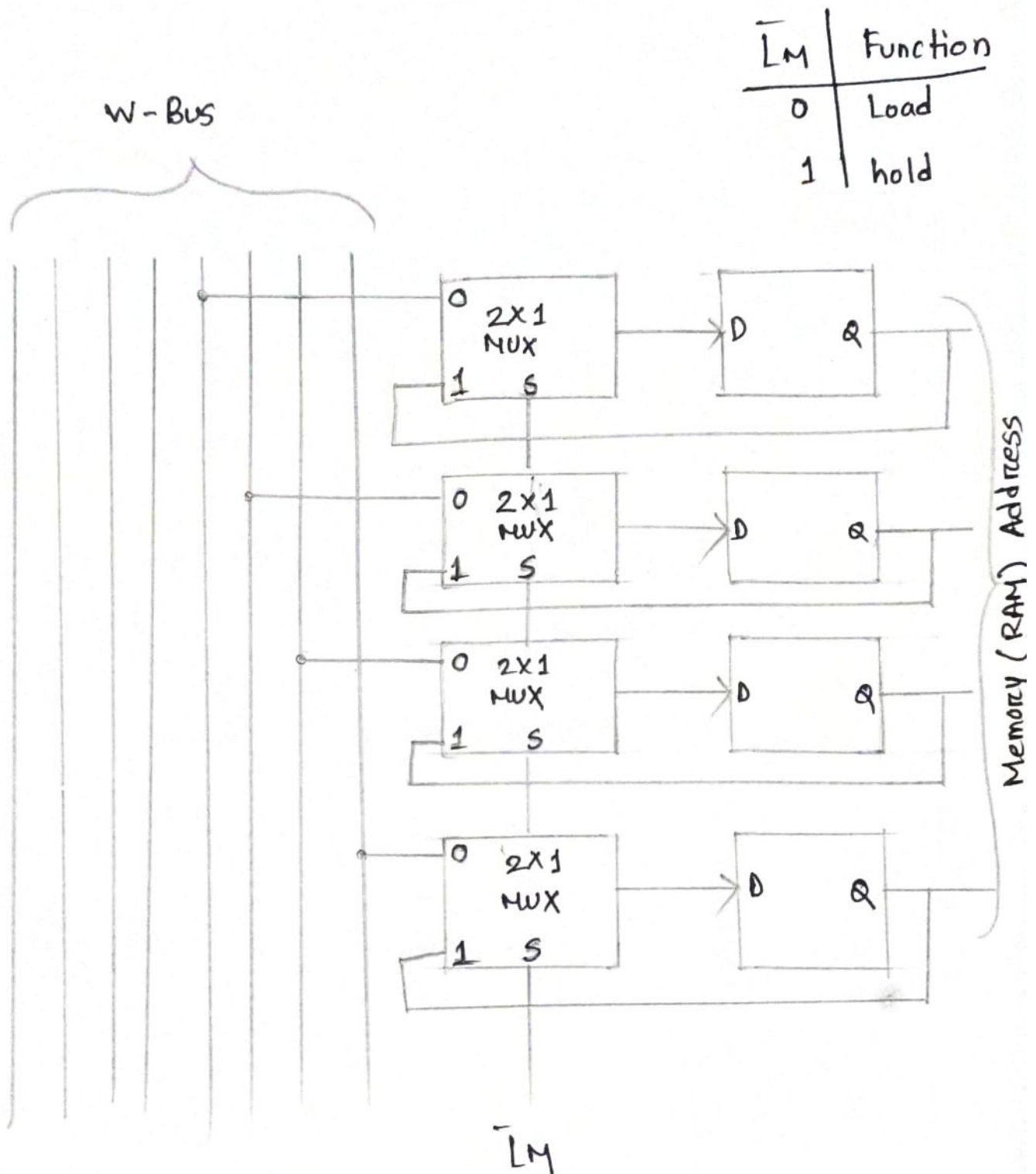
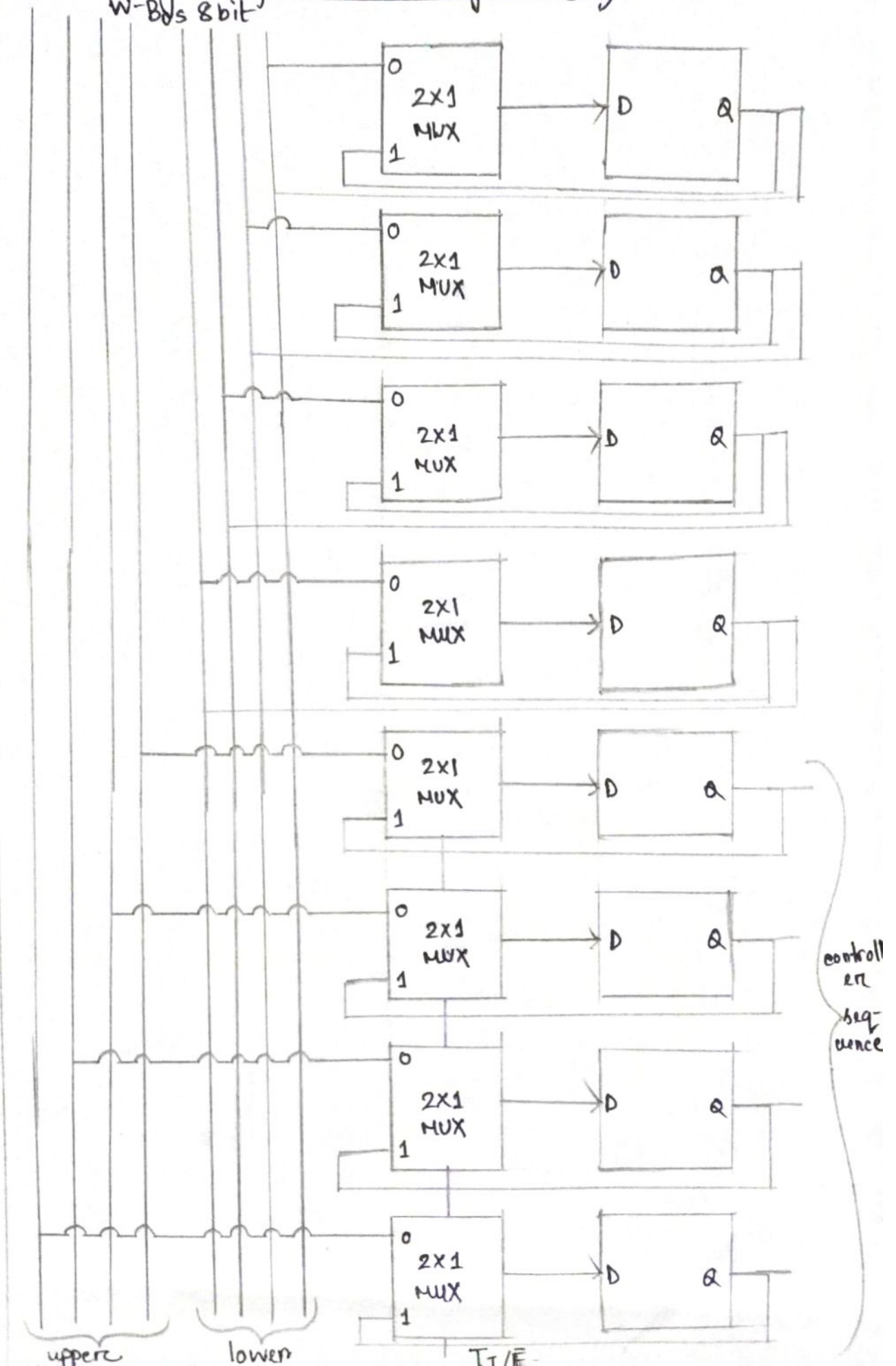
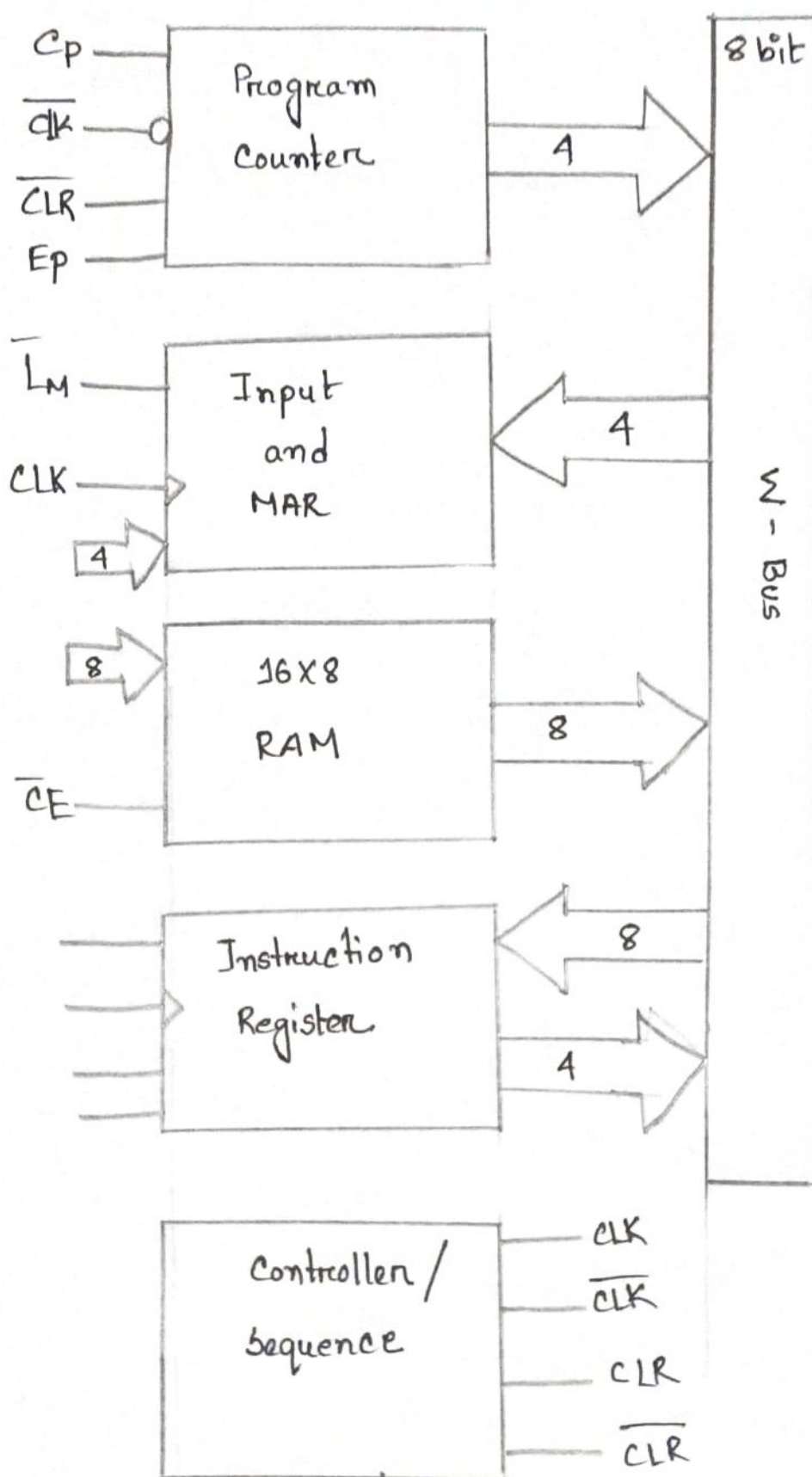


Fig: MAR

Circuit Diagram of Instruction Register (IR):- W-Bus 8 bit





C_p , E_p , \overline{L}_M , \overline{CE} , \overline{L}_i , \overline{E}_i , \overline{L}_A , E_A , S_u , E_v , \overline{L}_0 , \overline{L}_0

Control Unit :

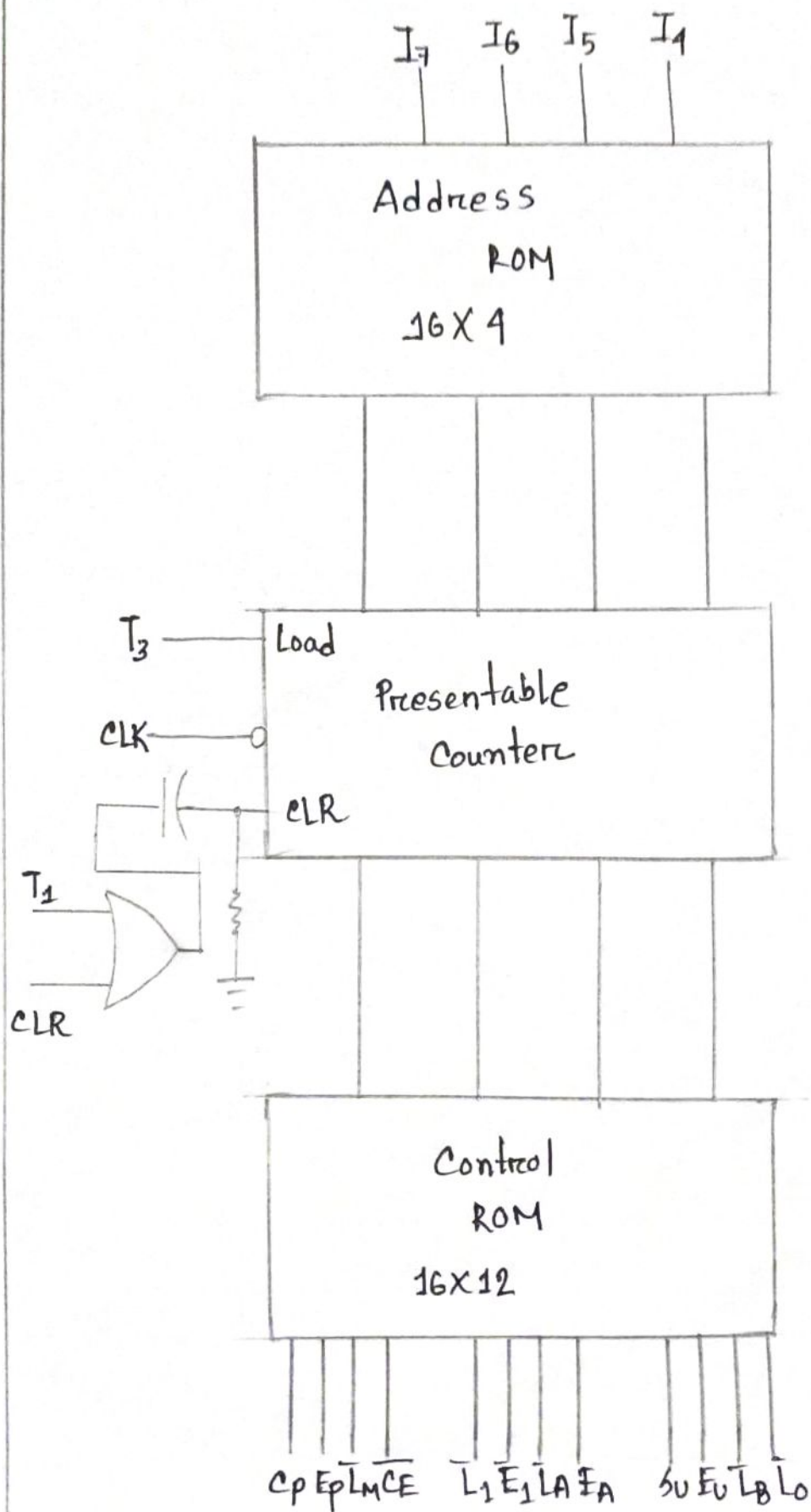
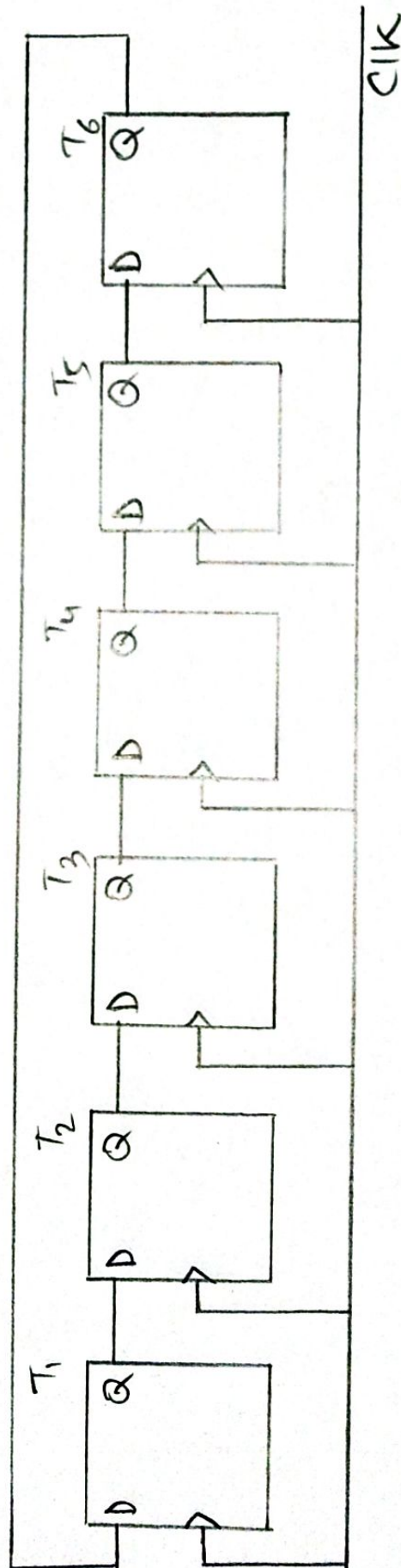
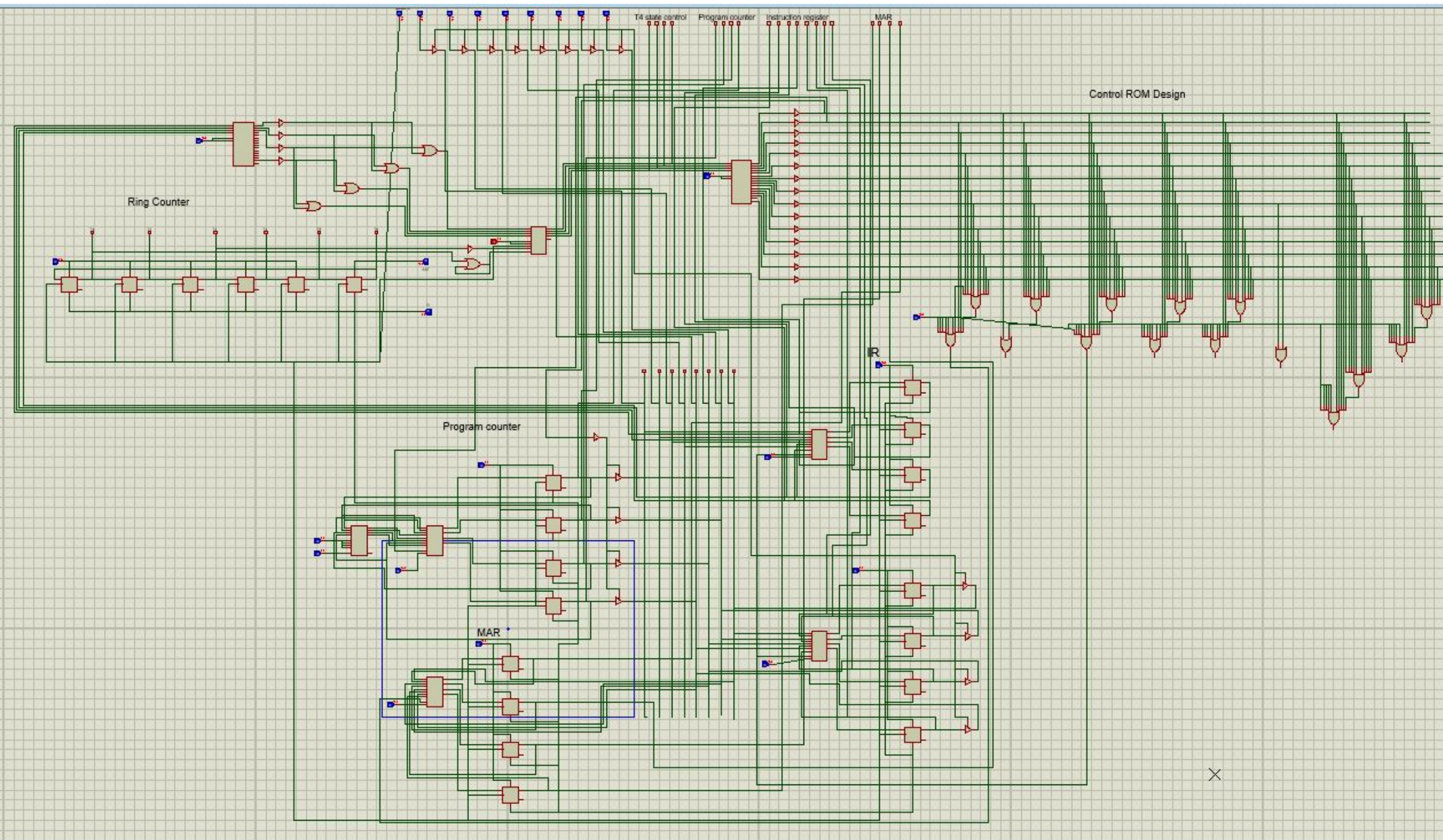


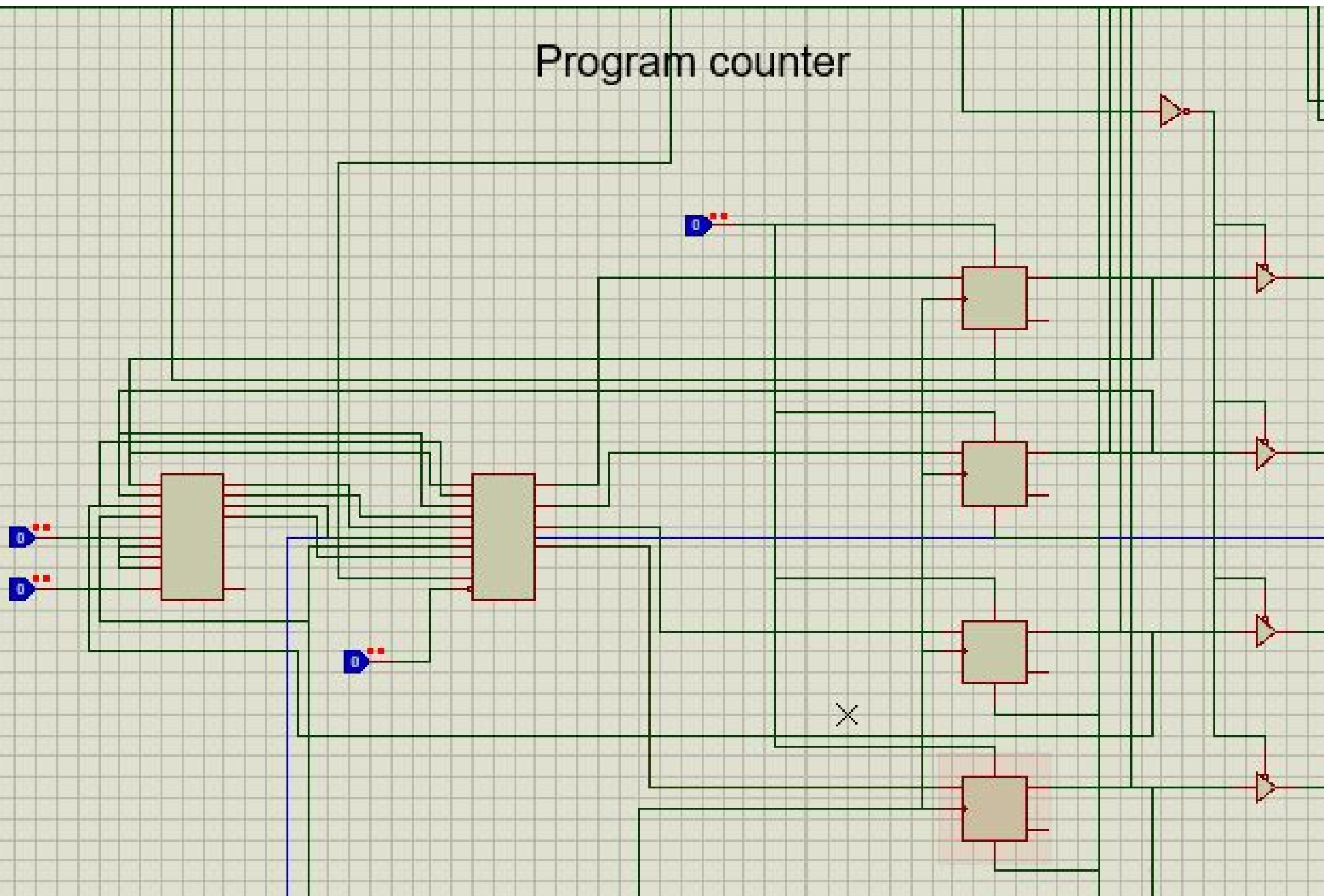
Figure: Microprogrammed control of SAP-1.

Circuit Diagram for ring counter





Program counter



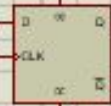
MAR

0

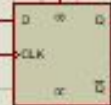
U9:A



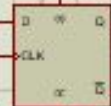
U9:B



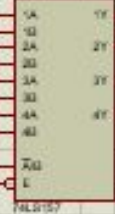
U10:A

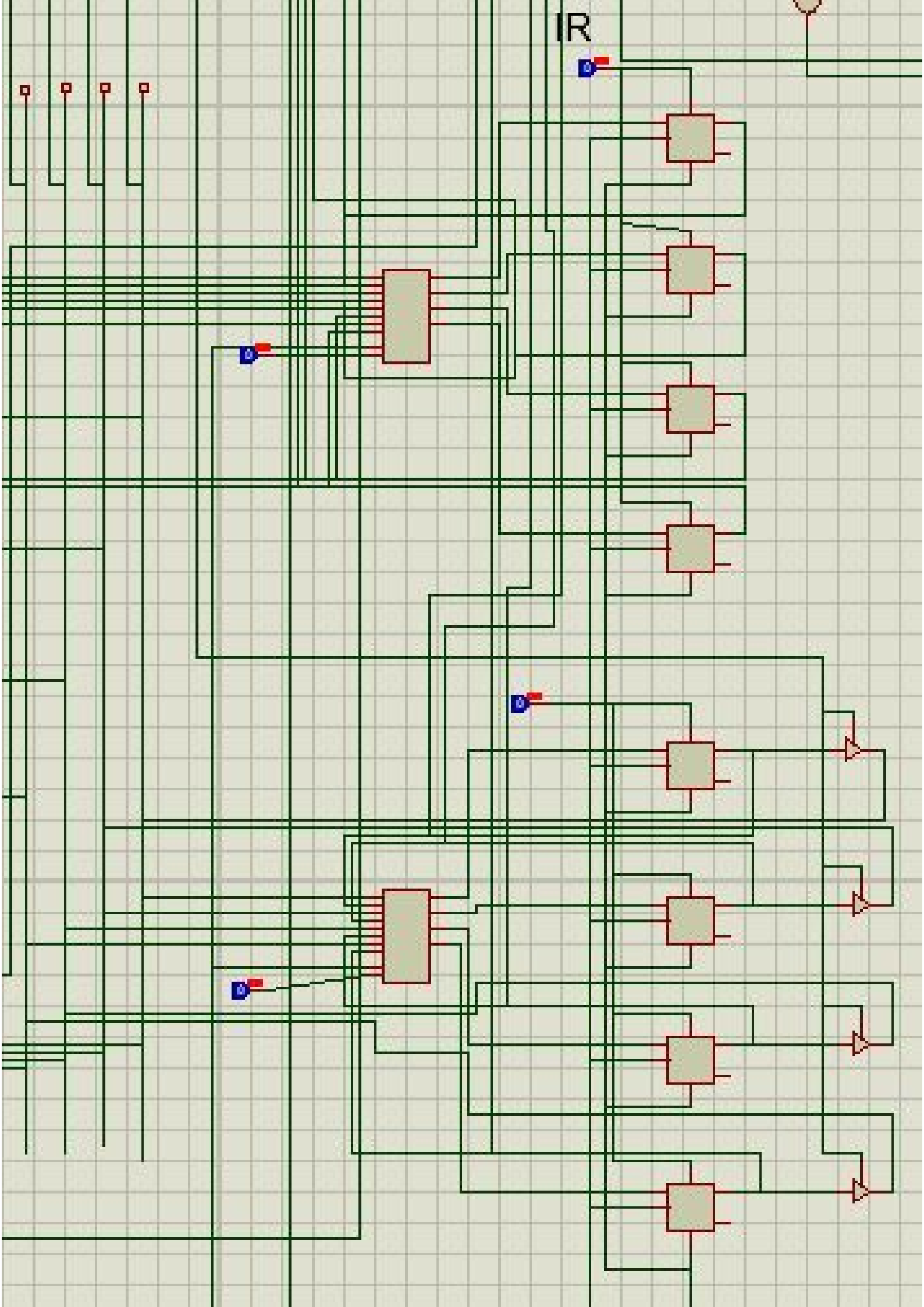


U10:B

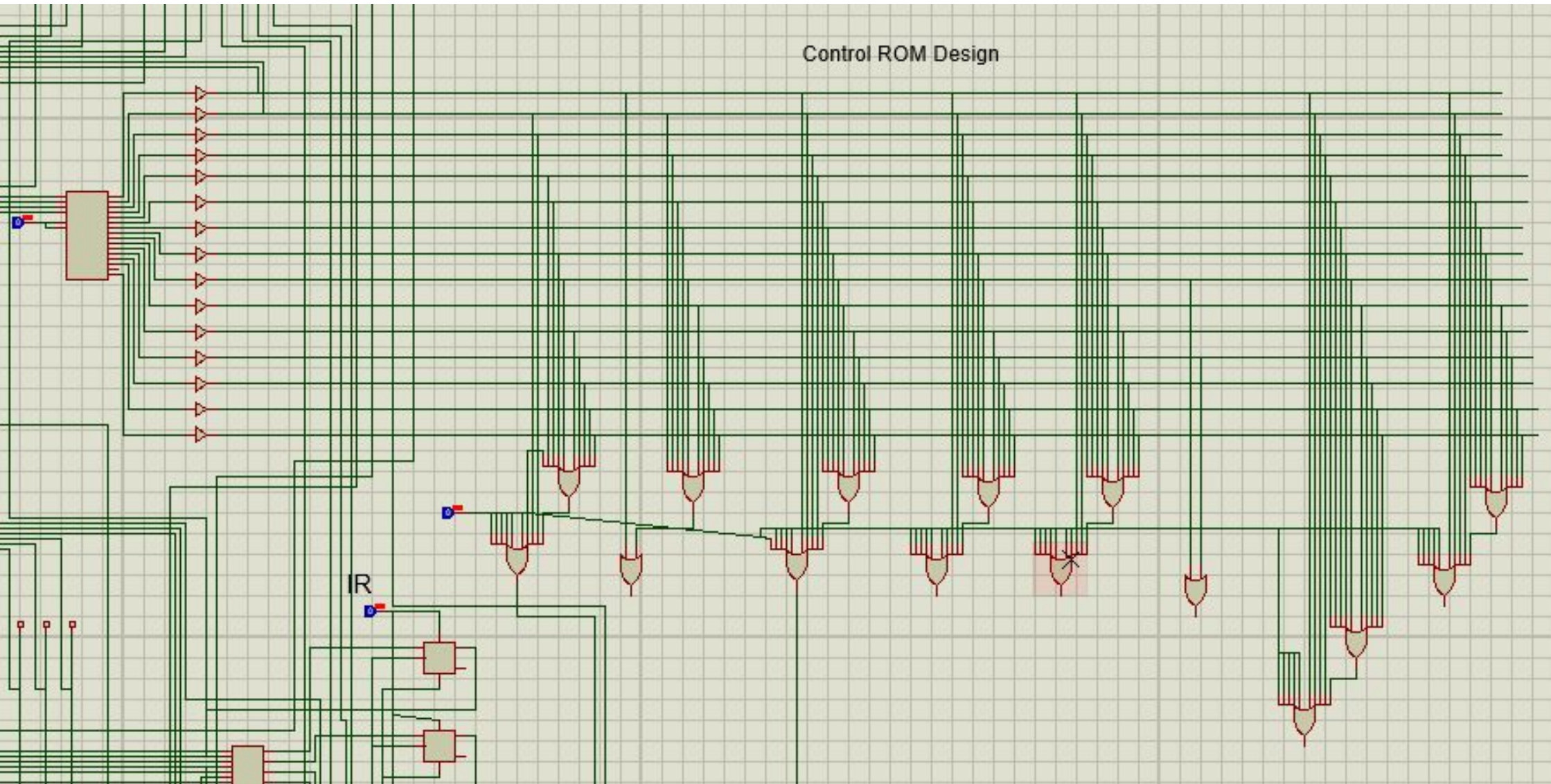


U8

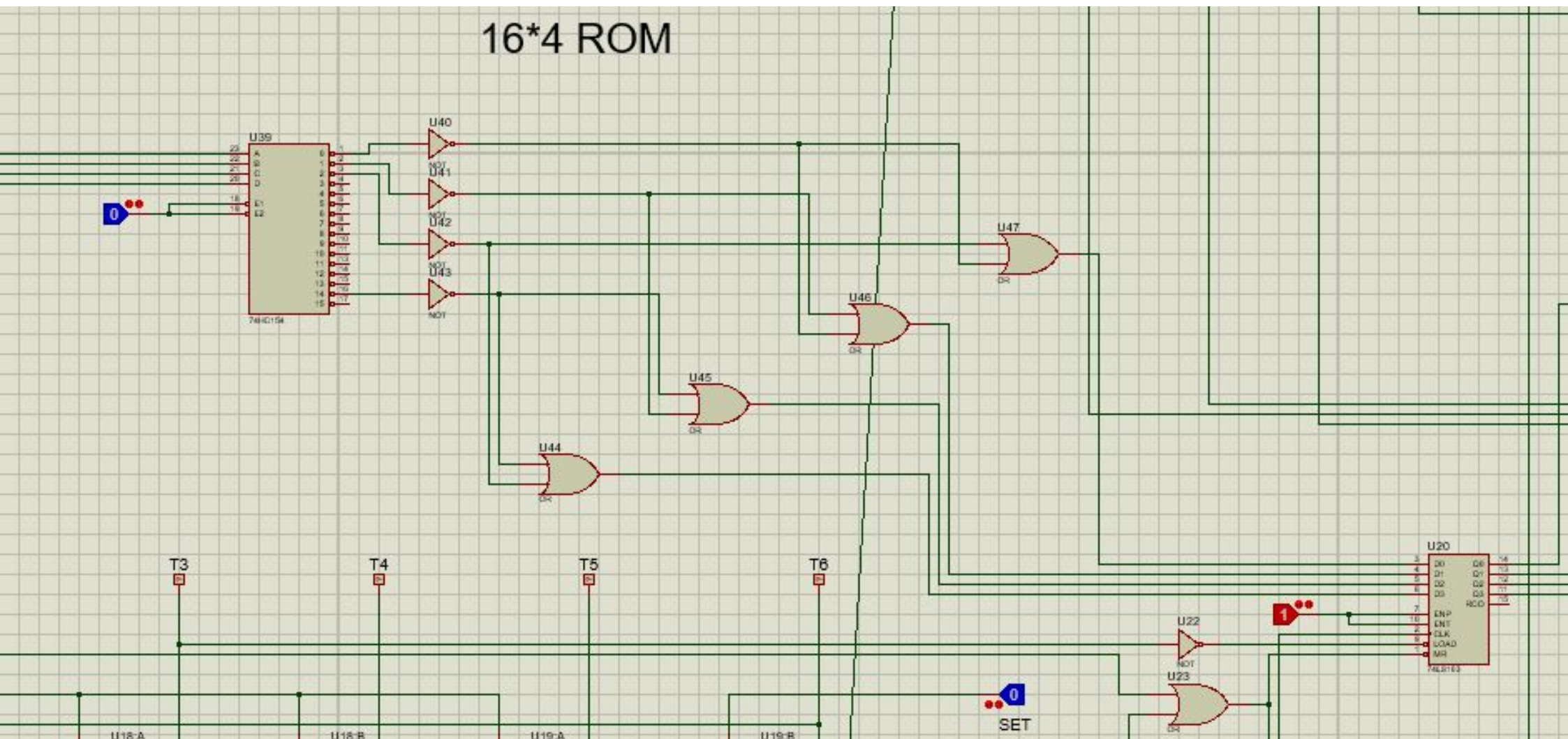




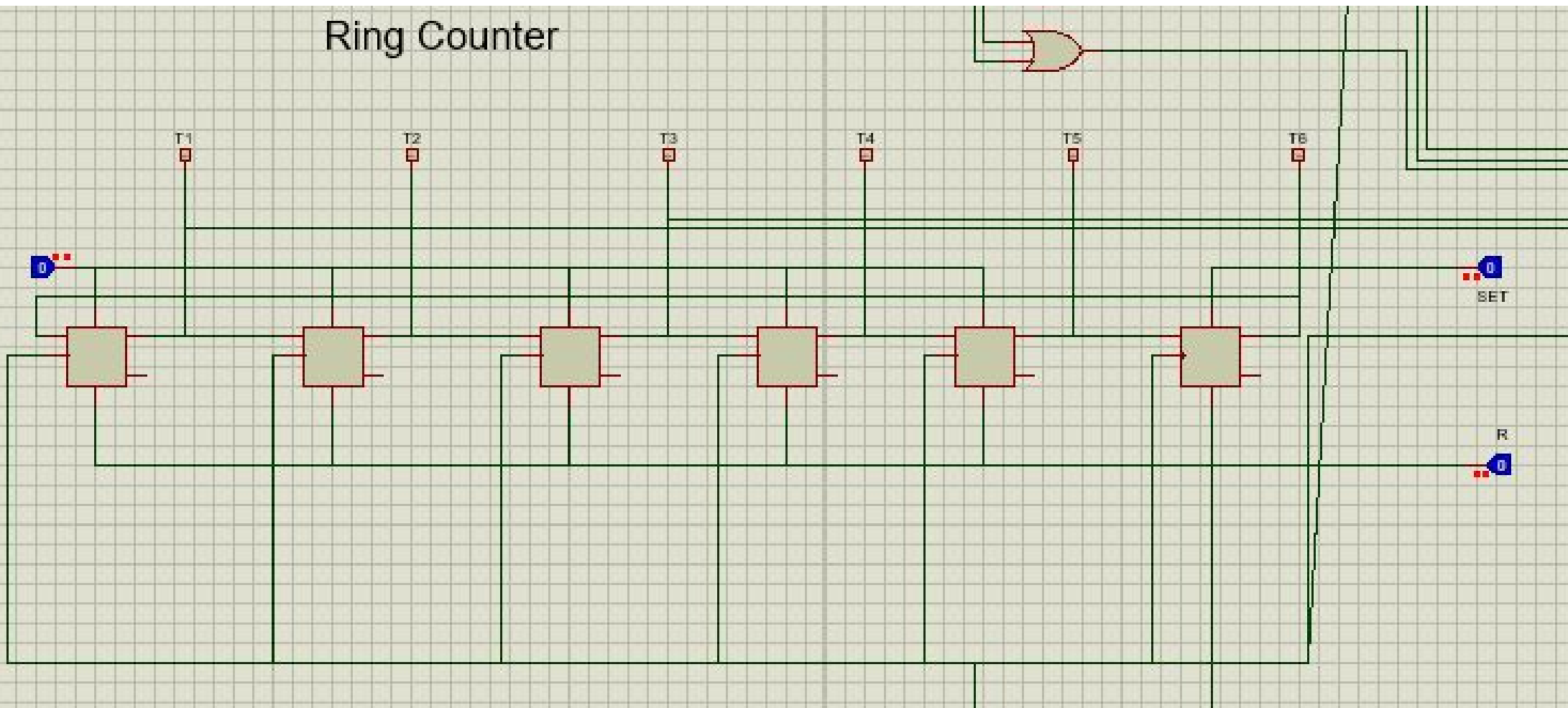
Control ROM Design



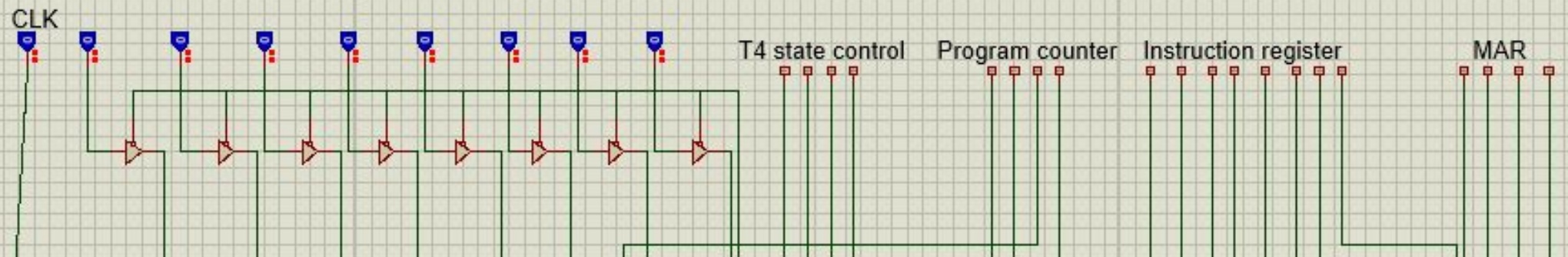
16*4 ROM

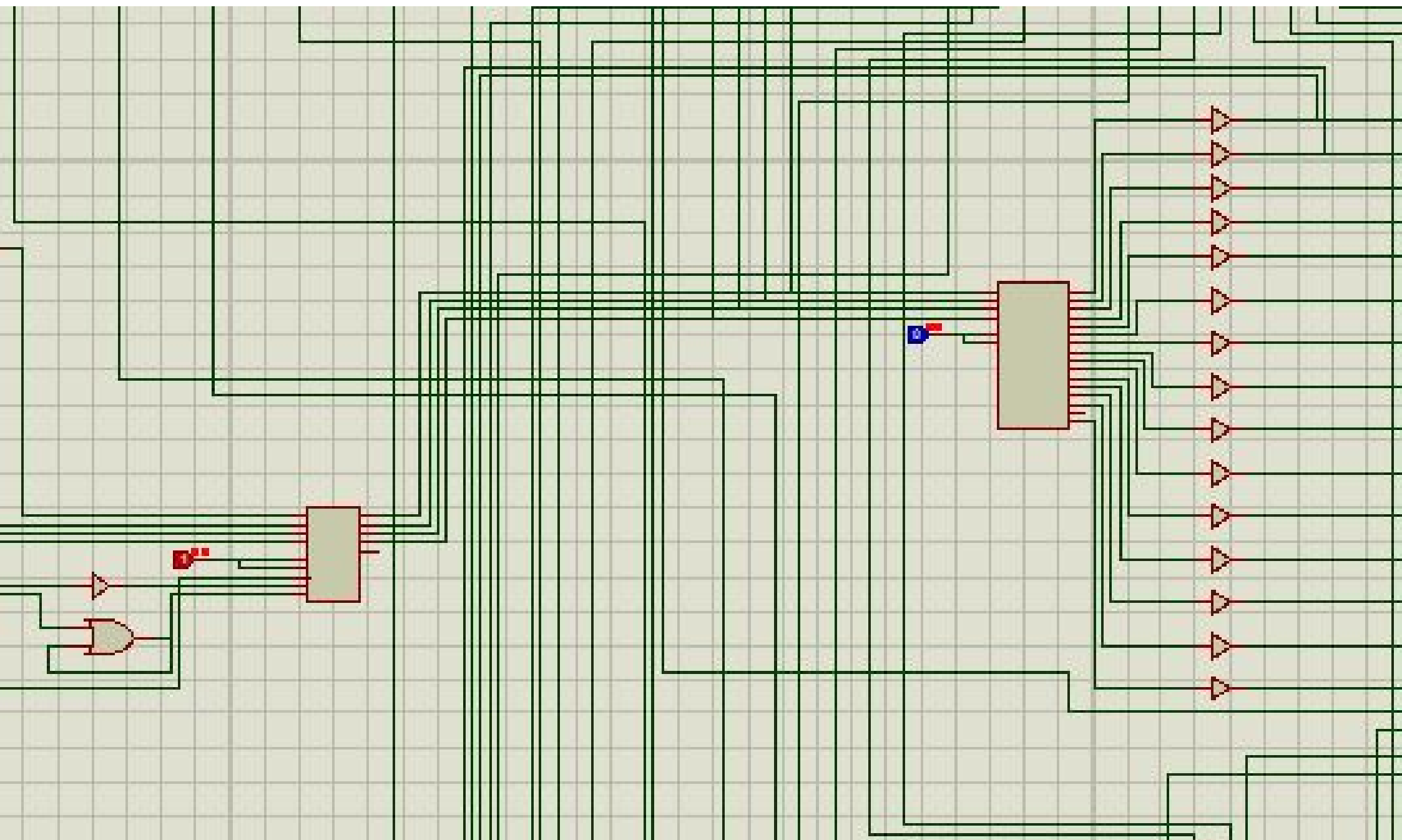


Ring Counter



Input & Output





Conclusion: There are some advantages of SAP-1 like flexibility. The architecture of SAP-1 is 8 bits of data bus and comprised of 16×8 memory. Therefore 16 memory location having 8 bits in each location. It needs 4 address lines which either comes from PC during computer run phase or may come from the 4 addresses switches during the program phase. These features of SAP-1 allows to make complex operations done.