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PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table of Contents	N/A	N/A
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A
3	4	BOM TABLES	N/A	N/A
4	6	SOC: MAIN	N/A	N/A
5	7	SOC: I/OS	N/A	N/A
6	8	SOC: NAND	N/A	N/A
7	9	SOC: DP,MIPI	N/A	N/A
8	10	SOC: DDR	N/A	N/A
9	11	SOC: IO POWER	N/A	N/A
10	12	SOC: SRAM POWER	N/A	N/A
11	13	SOC: CPU POWER	N/A	N/A
12	14	DDR: CHANNEL 0 AND 1	N/A	N/A
13	15	SOC: MISC & ALIASES	N/A	N/A
14	16	NAND: NAND	N/A	N/A
15	17	AUDIO: L81 CODEC	N/A	N/A
16	18	AUDIO: HP/DMIC FLEX CONNS	N/A	N/A
17	19	AUDIO: SPEAKER AMPS RIGHT	N/A	N/A
18	20	AUDIO: SPEAKER AMPS LEFT	N/A	N/A
19	24	SENSOR: OSCAR, GYRO, ACCEL	N/A	N/A
20	25	SENSOR: HALL EFFECT	N/A	N/A
21	26	IO: BUTTON FLEX CONN	N/A	N/A
22	27	CAMERA: FF AND ALS CONN	N/A	N/A
23	28	CAMERA: REAR CONN	N/A	N/A
24	29	SENSOR: COMPASS	N/A	N/A
25	30	CELL: SYSTEM & DEBUG CONNECTORS	RADIO_MLB_72_B7	06/03/2013

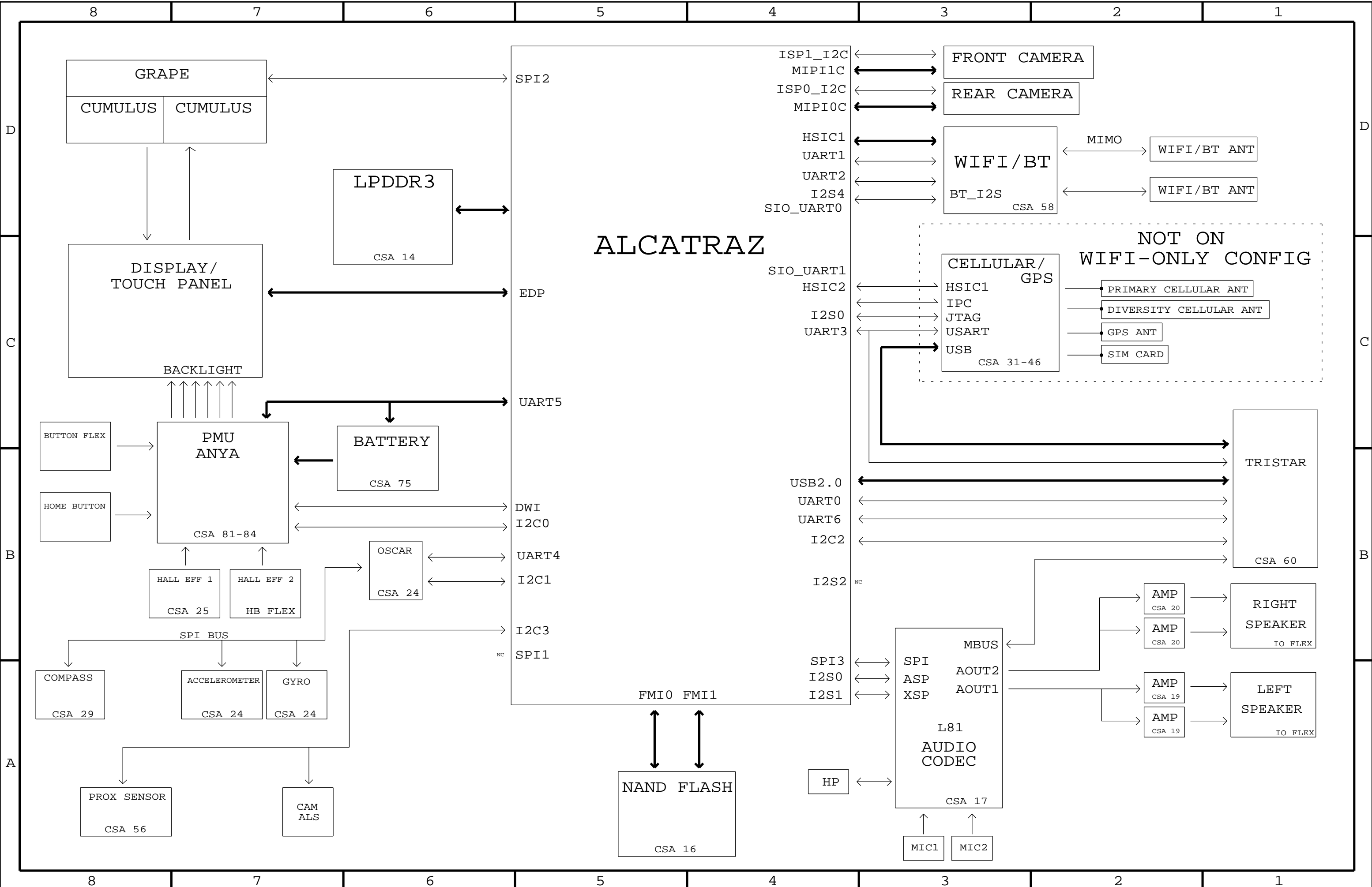
PDF	CSA	CONTENTS	SYNC MASTER	DATE
26	32	CELL: BASEBAND PMU (1 OF 2)	RADIO_MLB_72_B7	06/03/2013
27	33	CELL: BASEBAND PMU (2 OF 2)	RADIO_MLB_72_B7	06/03/2013
28	34	CELL: BASEBAND (1 OF 2)	RADIO_MLB_72_B7	06/03/2013
29	35	CELL: BASEBAND(2 OF 2)	RADIO_MLB_72_B7	06/03/2013
30	36	CELL: TRANSCEIVER (1 OF 2)	RADIO_MLB_72_B7	06/03/2013
31	37	CELL: TRANSCEIVER (2 OF 2)	RADIO_MLB_72_B7	06/03/2013
32	38	CELL: TRANSCEIVER MATCHING	RADIO_MLB_72_B7	06/03/2013
33	39	CELL: SAW BANK	RADIO_MLB_72_B7	06/03/2013
34	40	CELL: BAND 1/4 PAT	RADIO_MLB_72_B7	06/03/2013
35	41	CELL: BAND 2/3 PAD	RADIO_MLB_72_B7	06/03/2013
36	42	CELL: BAND 20 PAD	RADIO_MLB_72_B7	06/03/2013
37	43	CELL: BAND 5/8 PAD	RADIO_MLB_72_B7	06/03/2013
38	44	CELL: BAND 13/17 PAD	RADIO_MLB_72_B7	06/03/2013
39	45	CELL: PA DC/DC CONVERTER	RADIO_MLB_72_B7	06/03/2013
40	46	CELL: 2G FEM	RADIO_MLB_72_B7	06/03/2013
41	47	CELL: RX DIVERSITY	RADIO_MLB_72_B7	06/03/2013
42	48	CELL: GPS	RADIO_MLB_72_B7	06/03/2013
43	49	CELL: ANTENNA FEEDS	RADIO_MLB_72_B7	06/03/2013
44	51	CELL: SIM FLEX CONN	N/A	N/A
45	56	SENSOR: PROX AD7149	N/A	N/A
46	58	WIFI/BT: MODULE	WIFI_DEV	05/21/2013
47	60	IO: TRISTAR	N/A	N/A
48	61	IO: FILTERING	N/A	N/A
49	62	IO: FLEX HOTBAR PADS	N/A	N/A
50	63	IO: HOME BUTTON FILTERS	N/A	N/A

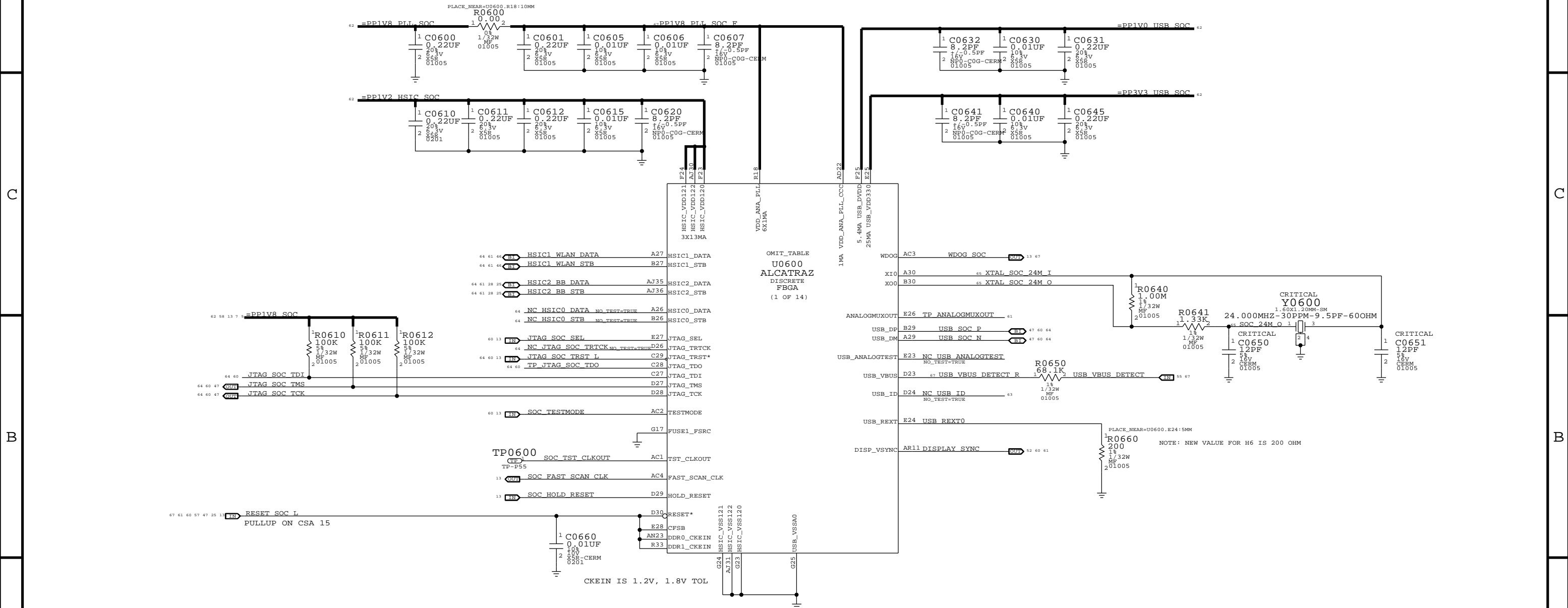
PDF	CSA	CONTENTS	SYNC MASTER	DATE
51	65	GRAPE: 1V8 POWER SWITCH	N/A	N/A
52	66	GRAPE: CUMULUS	N/A	N/A
53	70	DISPLAY: EDP CONN	N/A	N/A
54	75	POWER: BATTERY CONNECTOR	N/A	N/A
55	81	PMU: ANYA PAGE 1	N/A	N/A
56	82	PMU: ANYA PAGE 2	N/A	N/A
57	83	PMU: ANYA PAGE 3	N/A	N/A
58	84	PMU: ANYA PAGE 4	N/A	N/A
59	90	SOC: DEBUG	N/A	N/A
60	93	TEST: TP/HOLES/FIDUCUALS	N/A	N/A
61	94	TEST: EE TP/PP	N/A	N/A
62	121	POWER: ALIASES	N/A	N/A
63	150	CONSTRAINTS: MLB RULES	N/A	N/A
64	151	CONSTRAINTS: LOW SPEED BUS	N/A	N/A
65	152	CONSTRAINTS: DISPLAY/AUDIO	N/A	N/A
66	153	CONSTRAINTS: DDR/FMI	N/A	N/A
67	154	CONSTRAINTS: POWER / GND	N/A	N/A
68	157	CONSTRAINTS: RF	N/A	N/A
69	158	CONSTRAINTS: WIFI/BT	WIFI_DEV	05/21/2013

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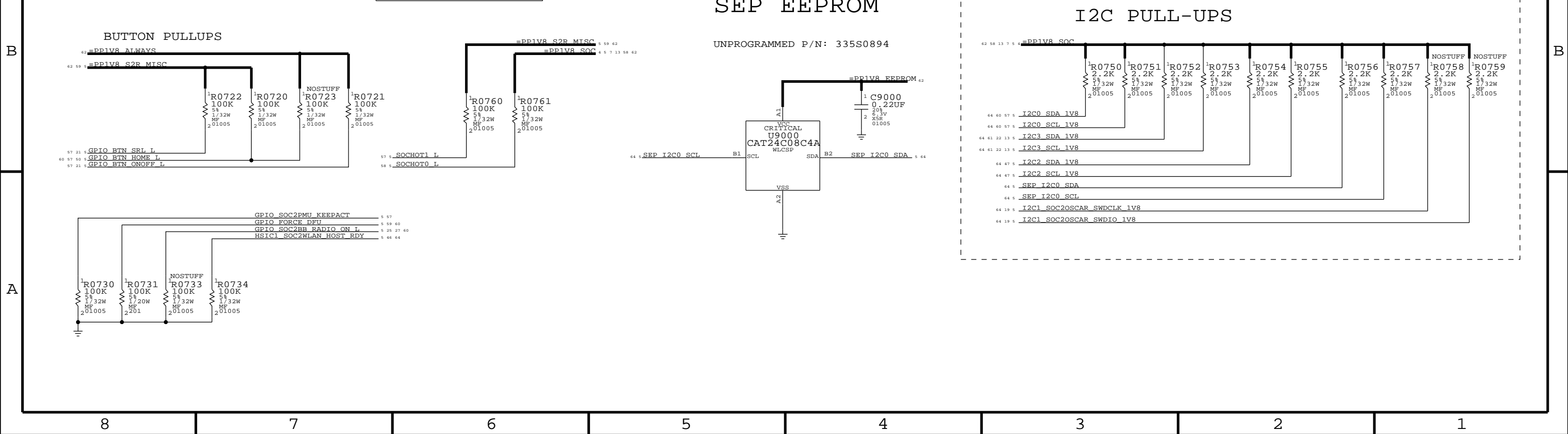
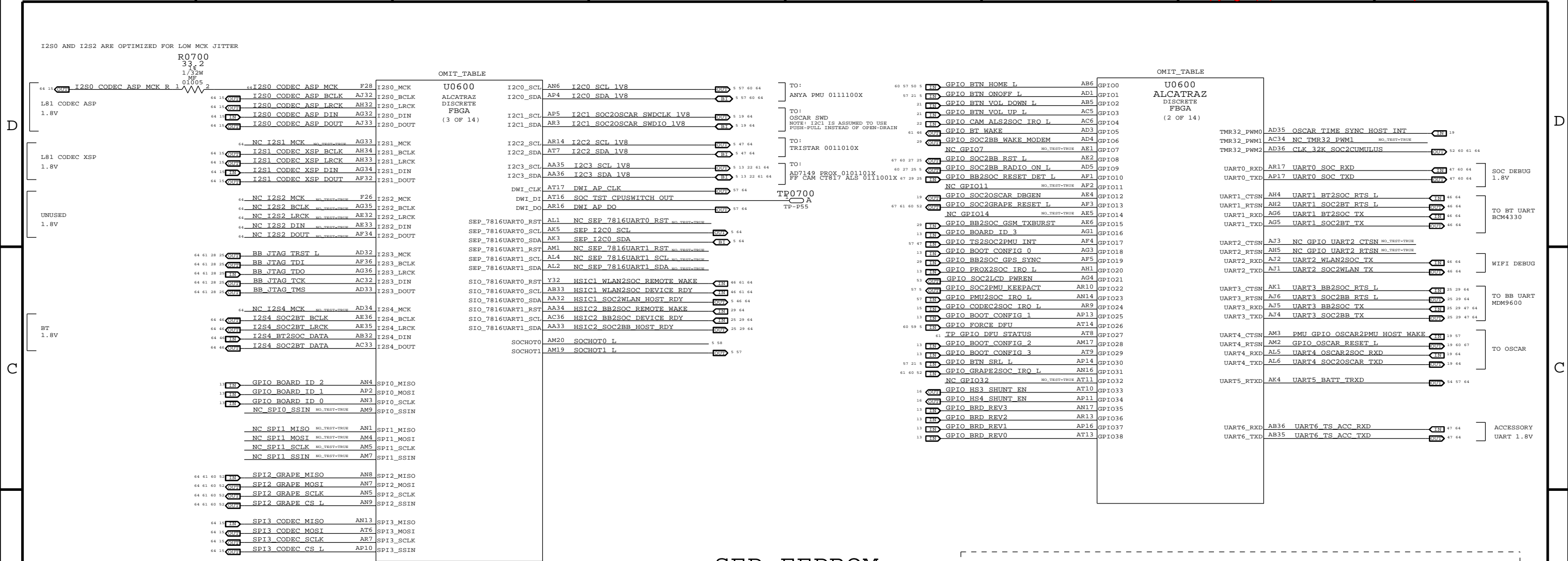
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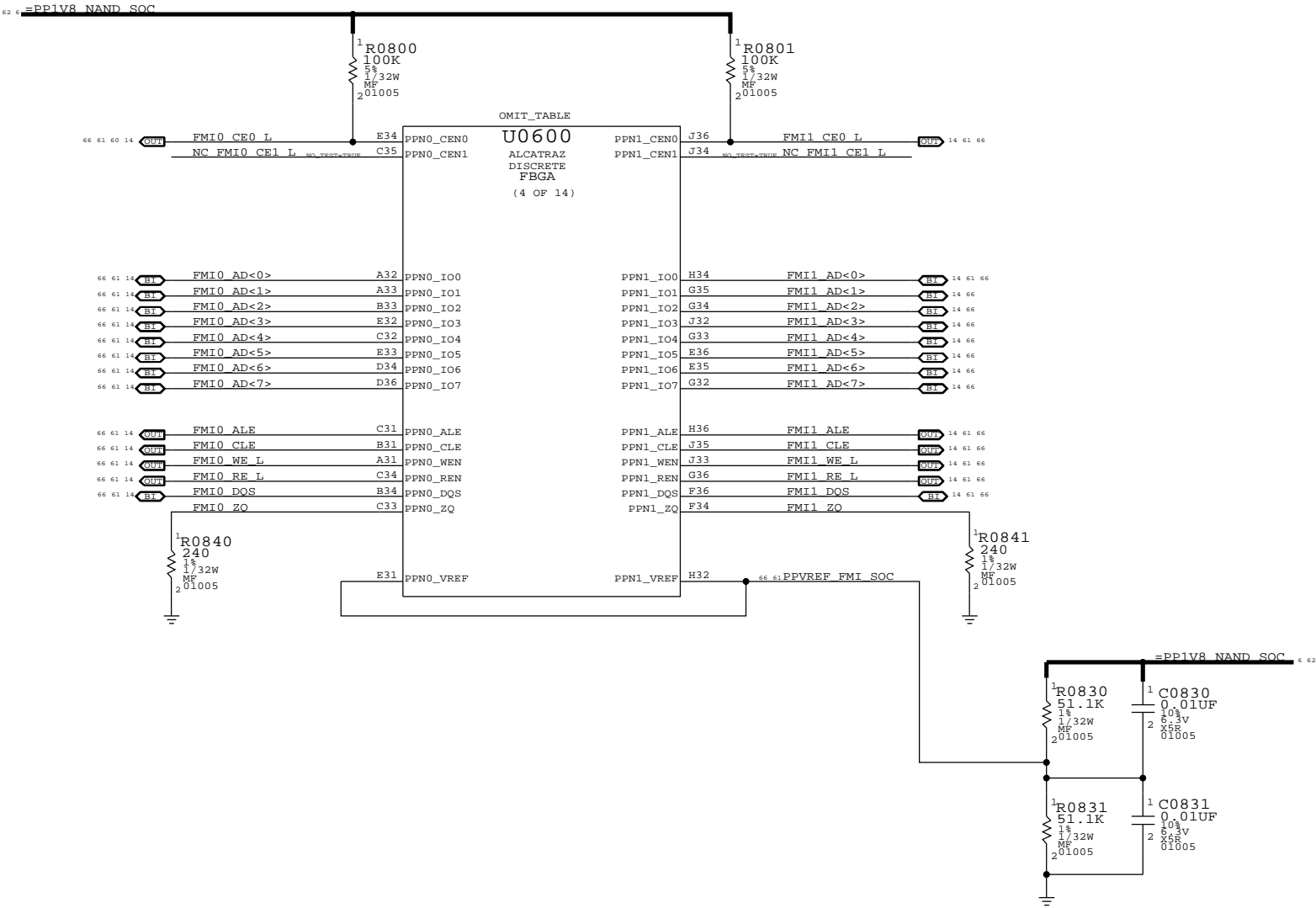
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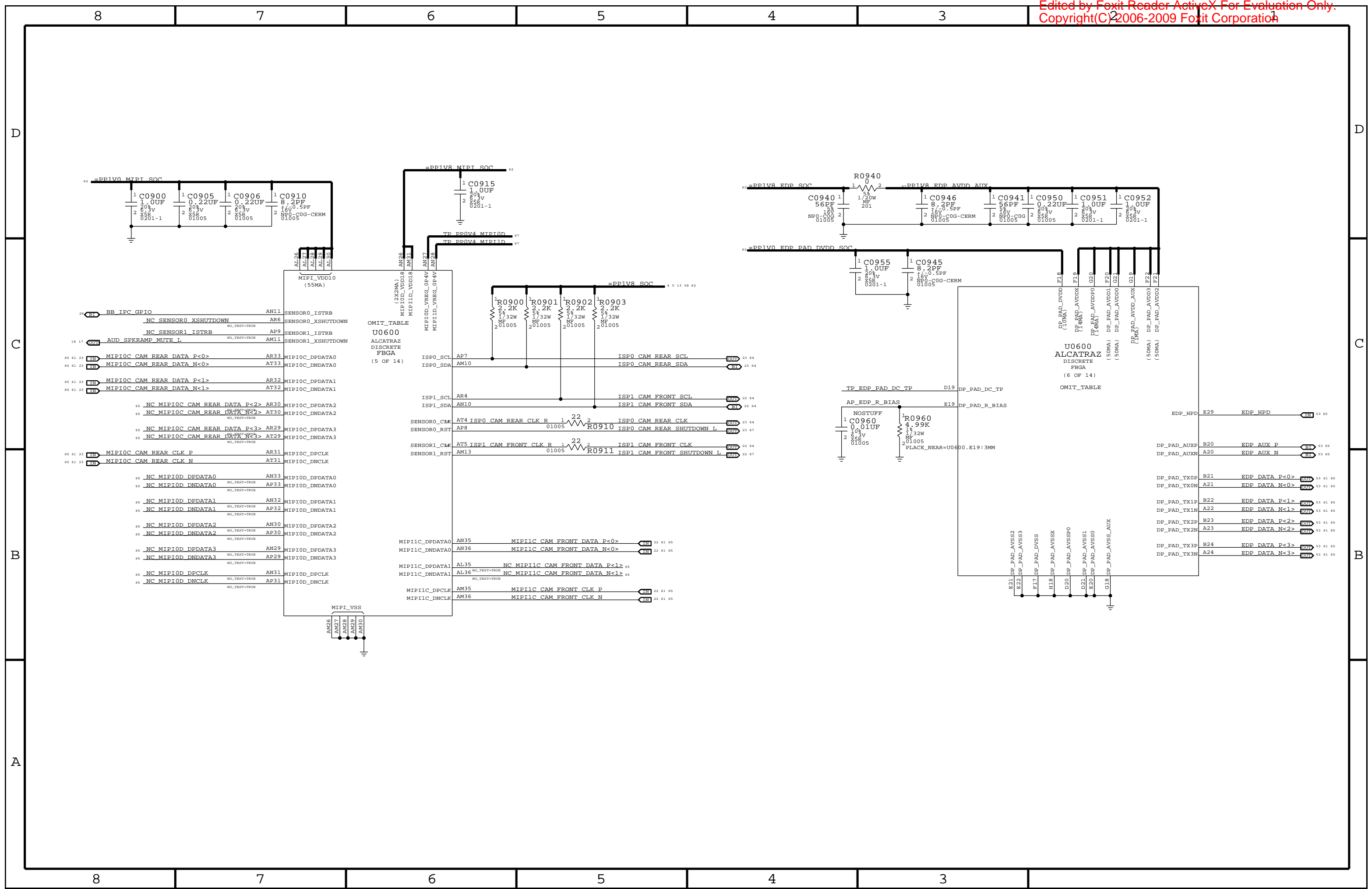
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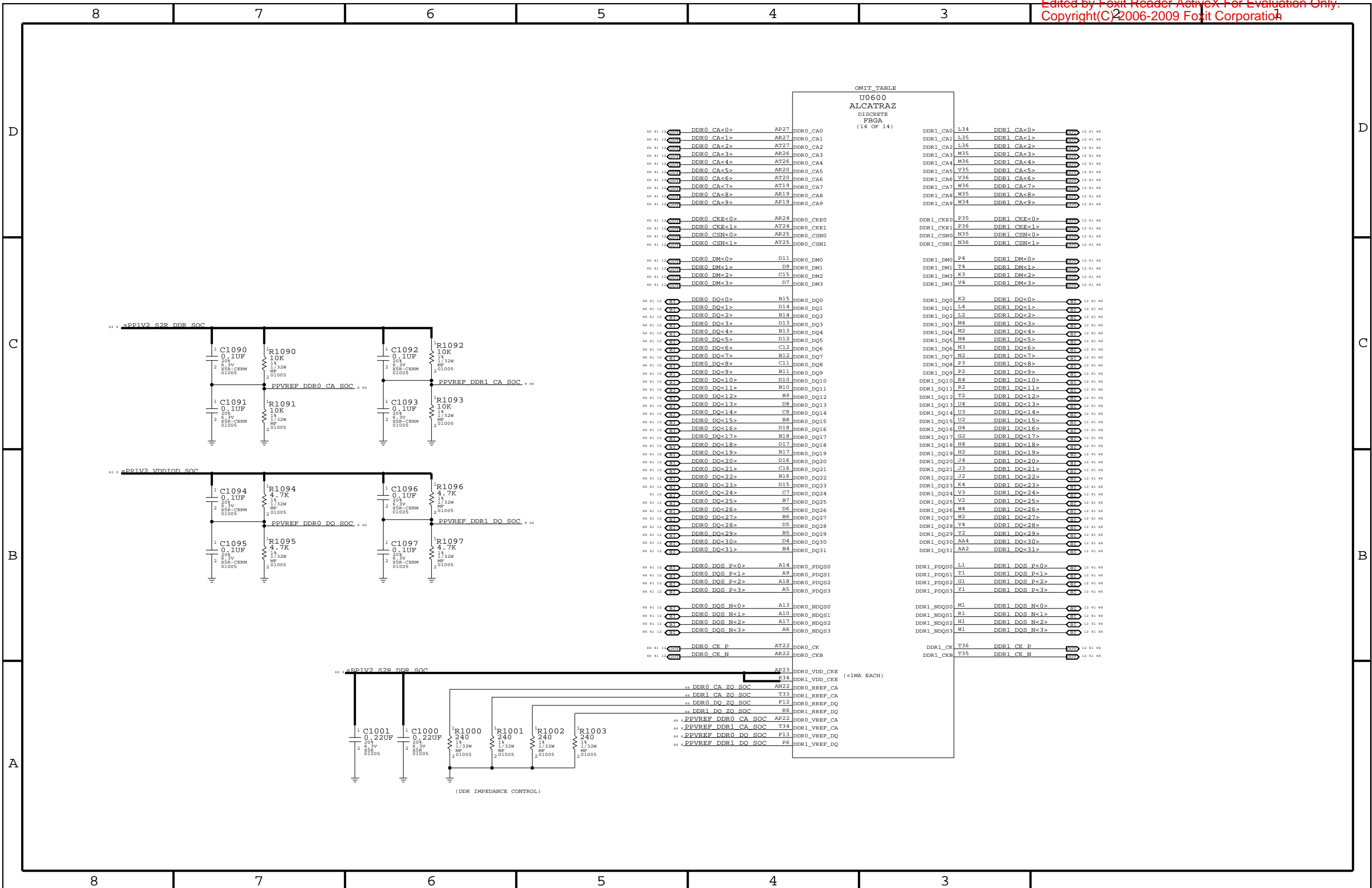
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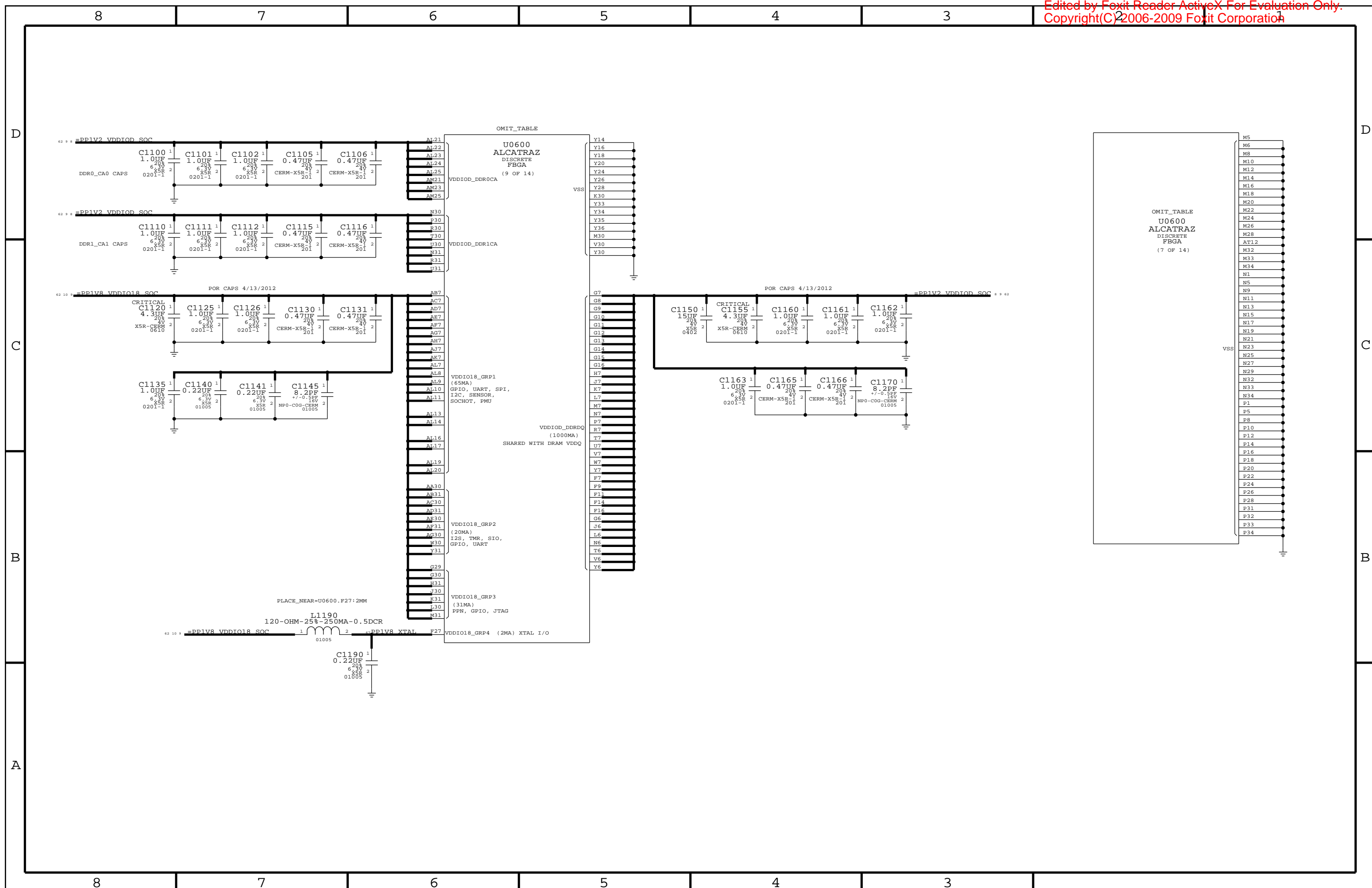
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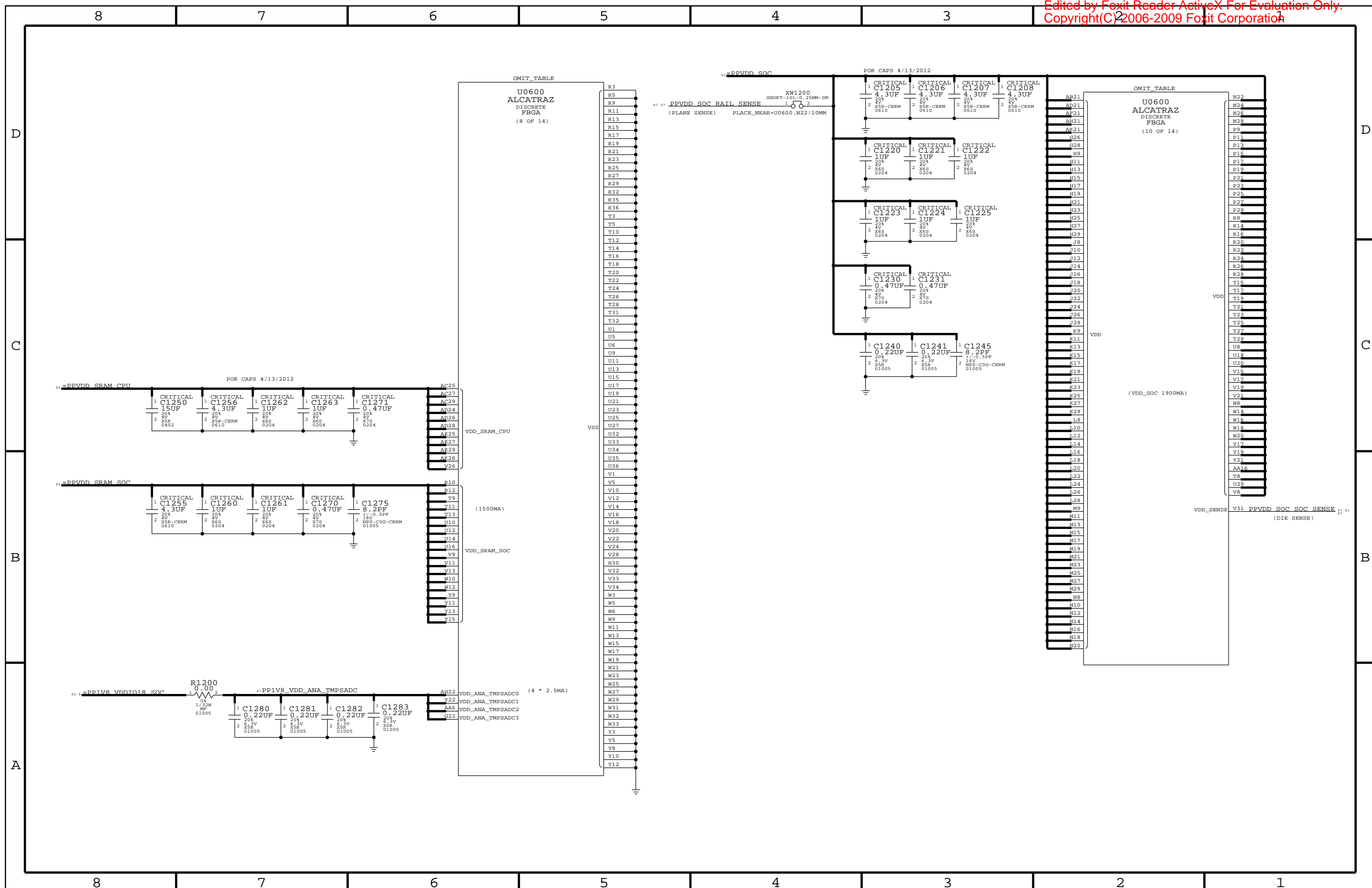


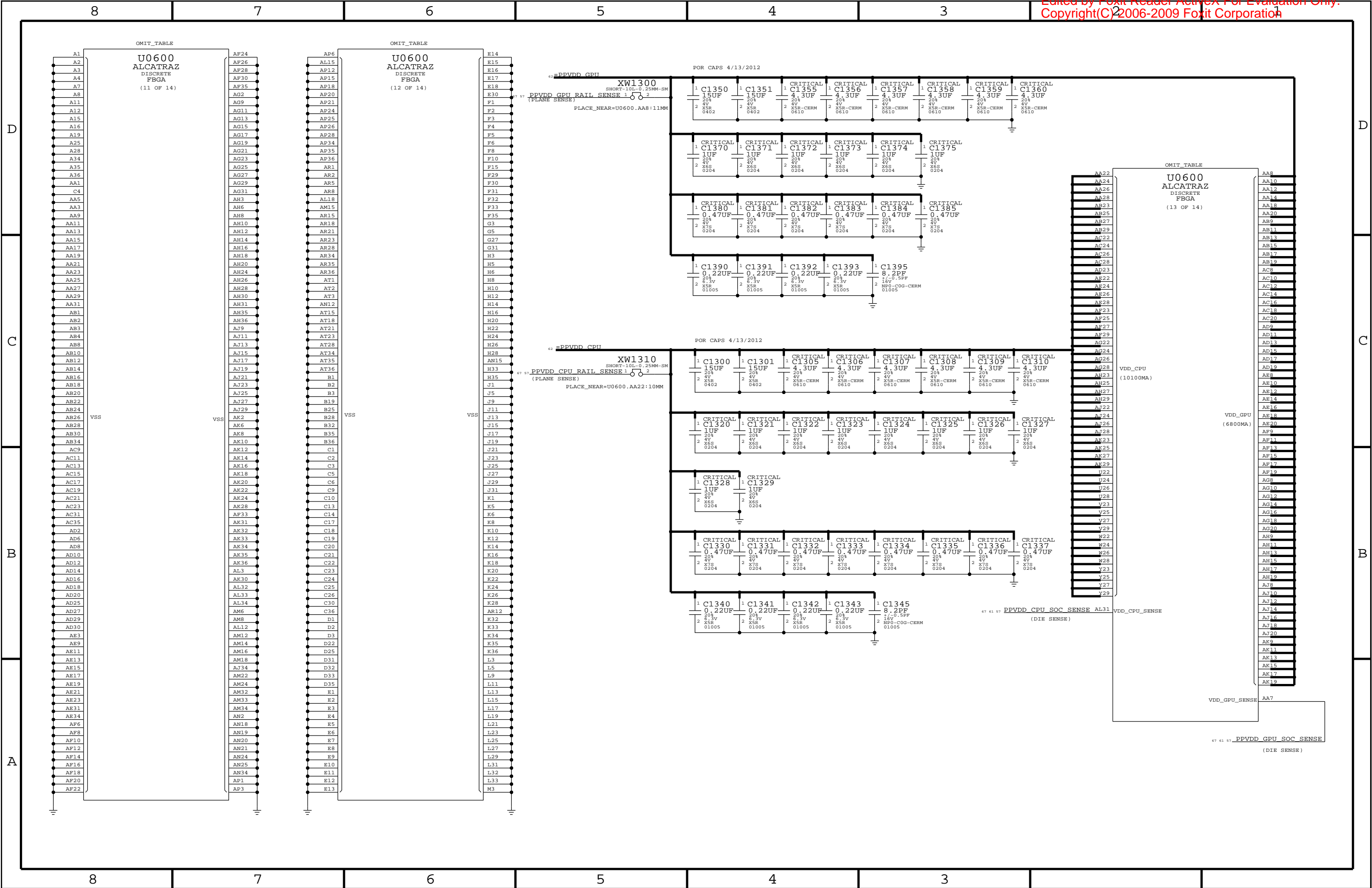


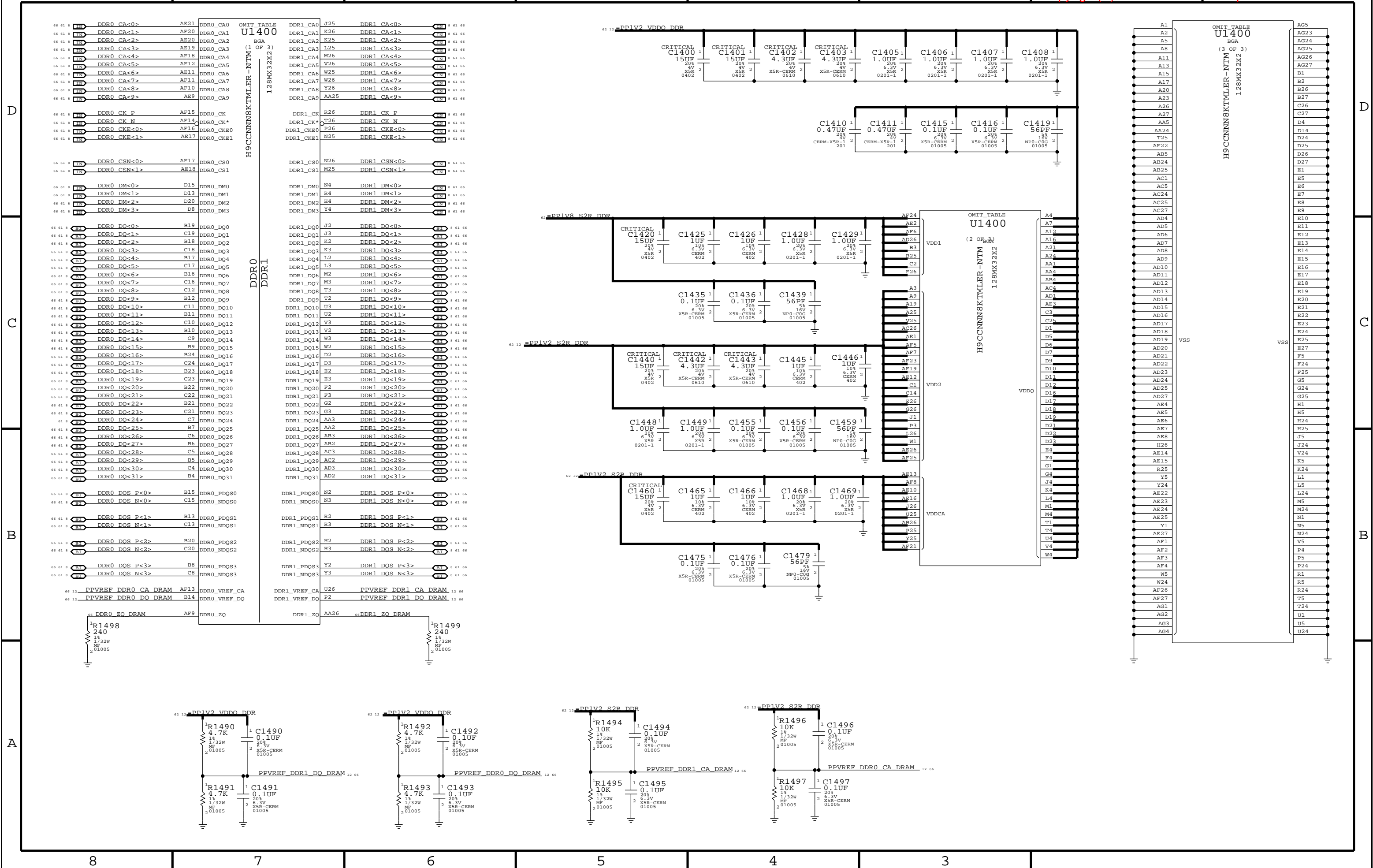


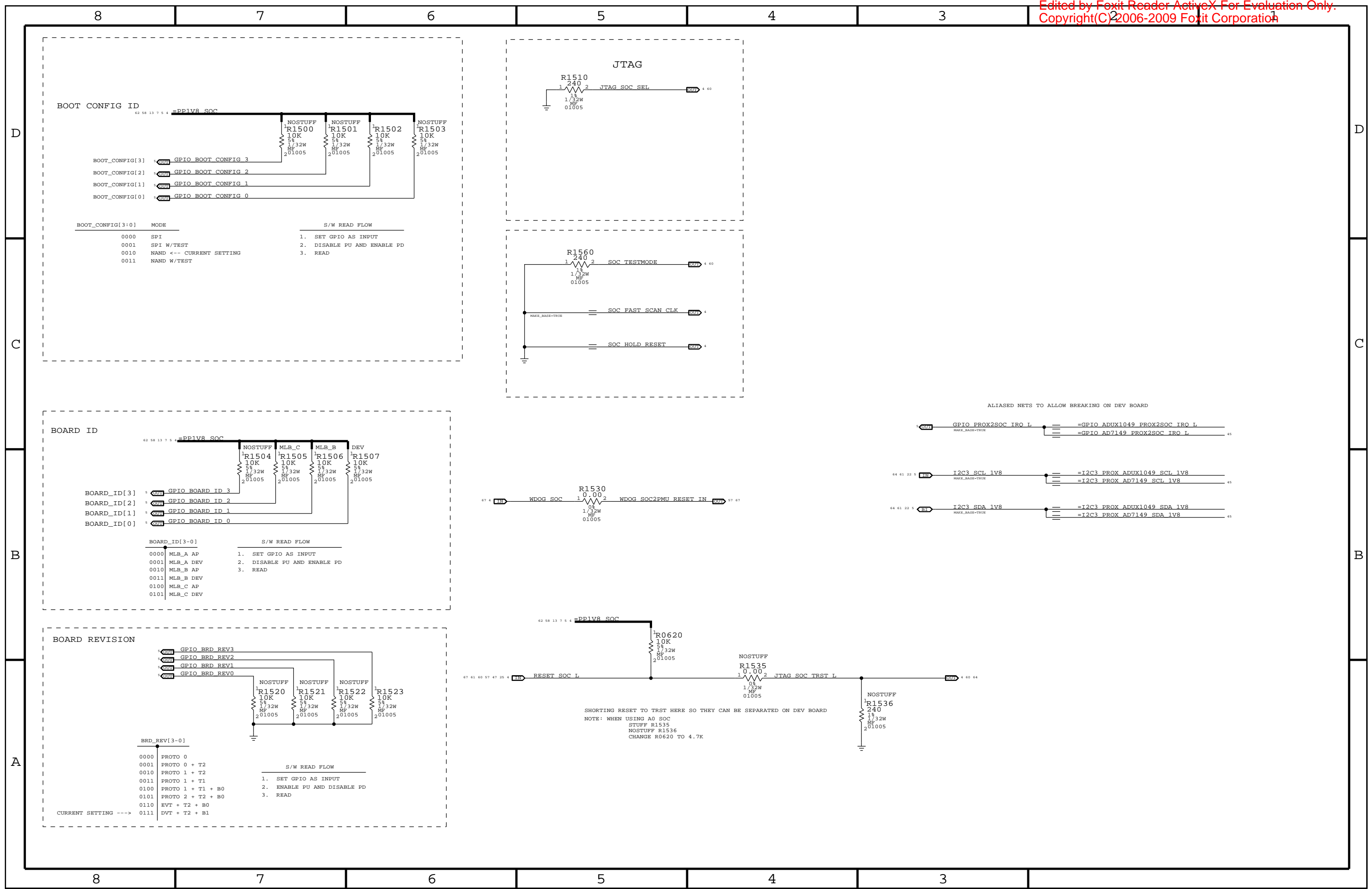




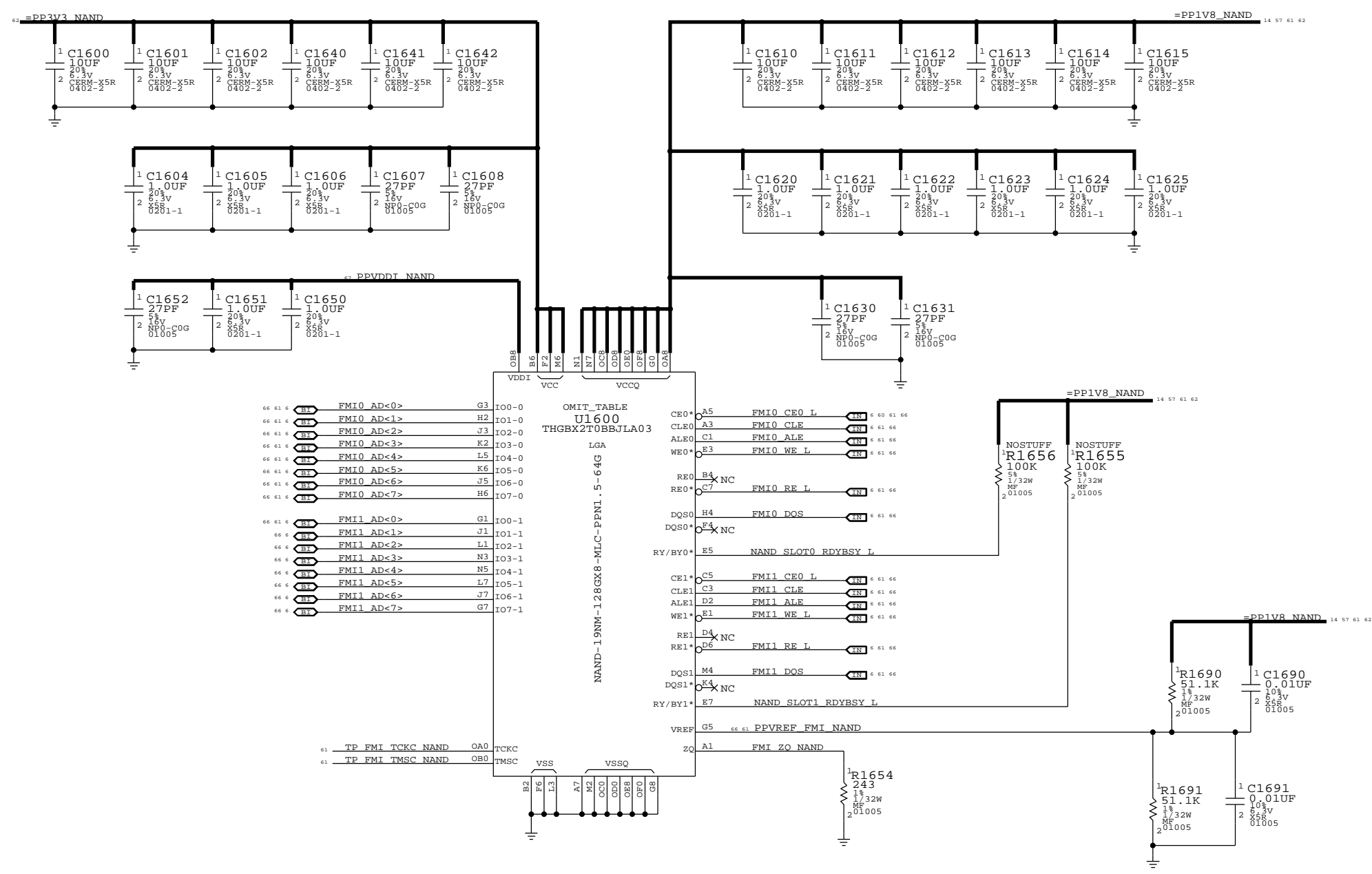


















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SPEAKER AMPLIFIER

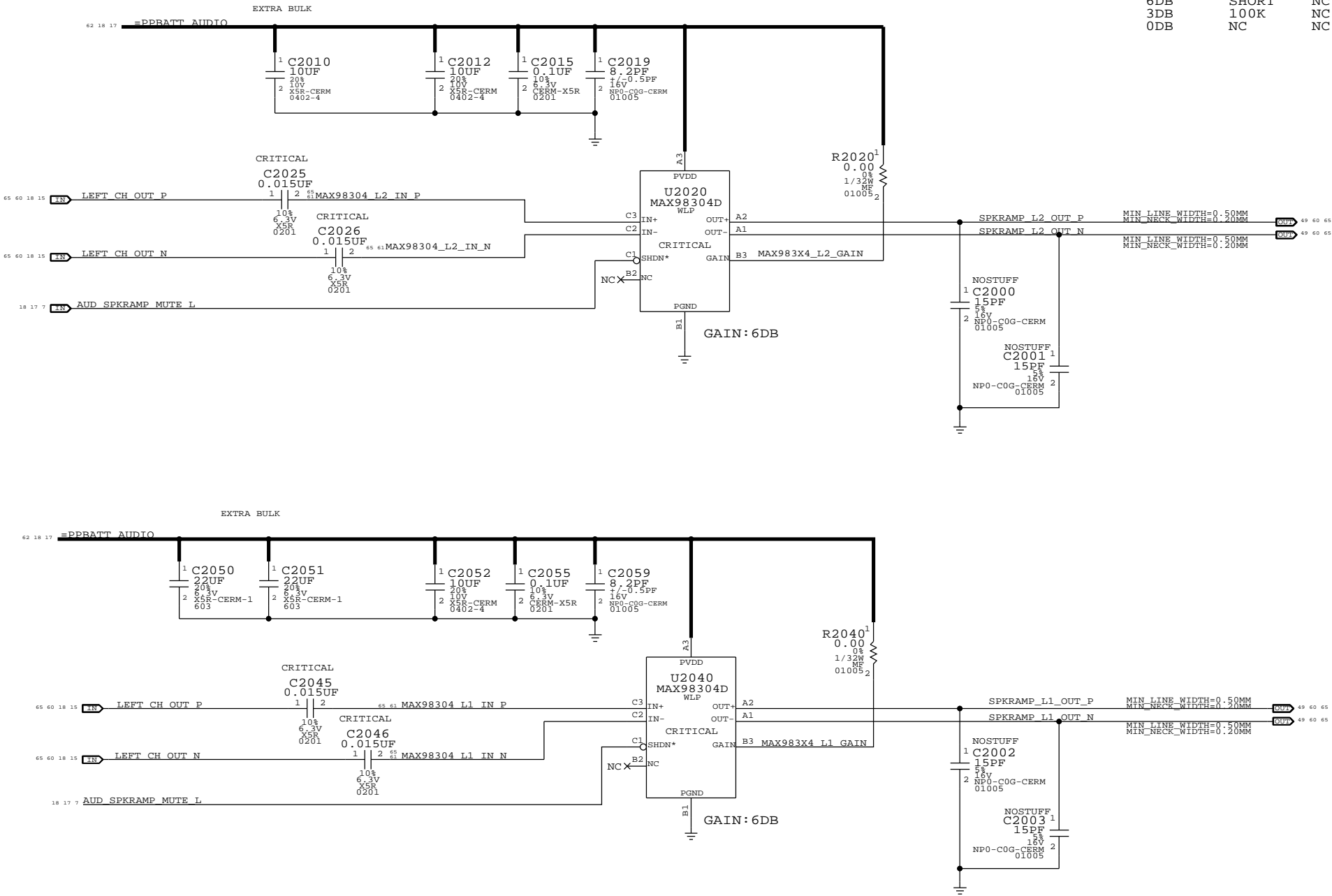
APN: 353S3445

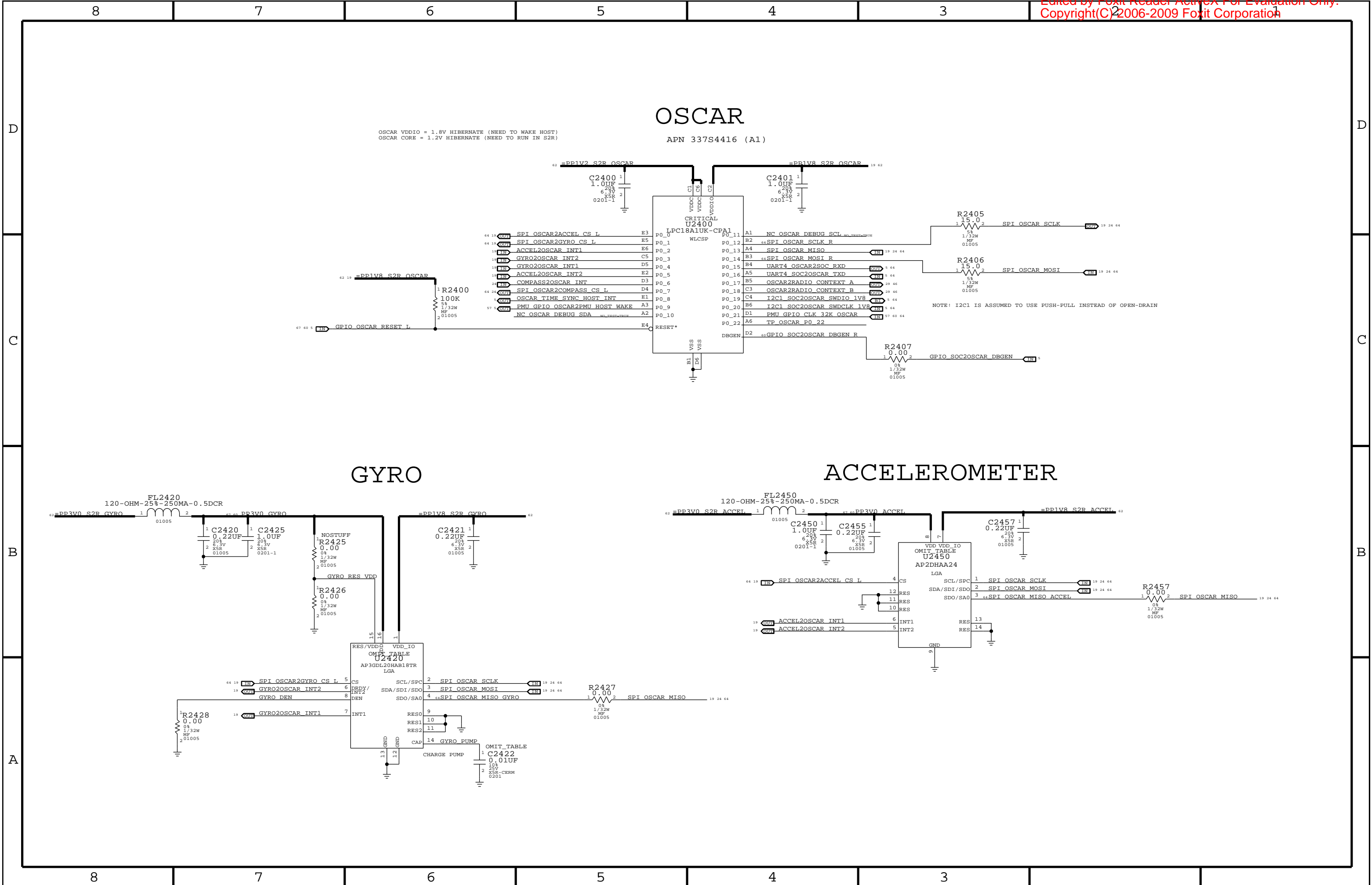
TURN ON TIME: 3.5MS

75HZ +/- XXX%

TURN ON DELAY: ?MS

GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC







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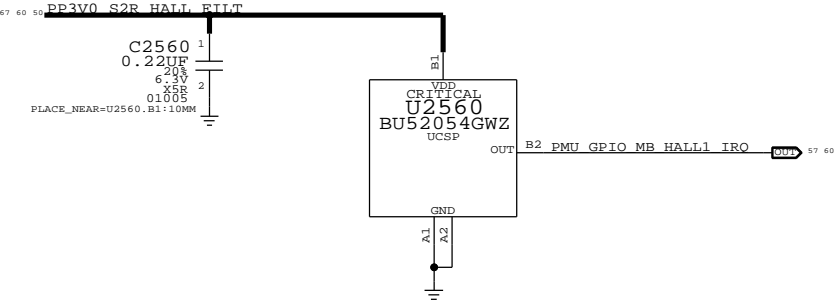
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# HALL EFFECT

BIPOLAR ONE OUTPUT APN 353S3687

C-PANEL HALL EFFECT SENSOR  
(B-PANEL HALL EFFECT SENSOR ON HB)



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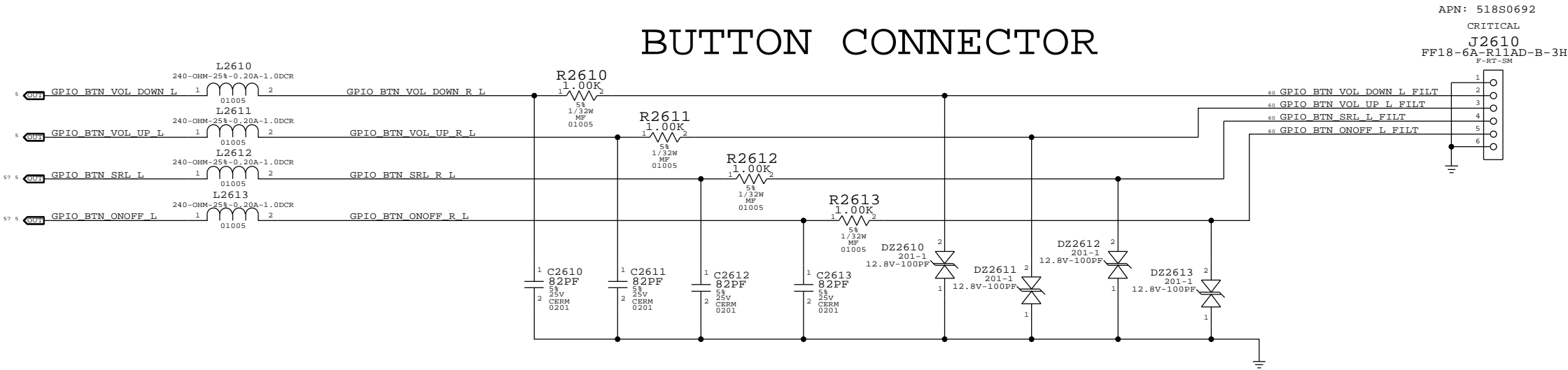
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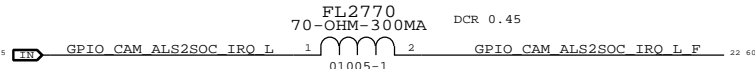
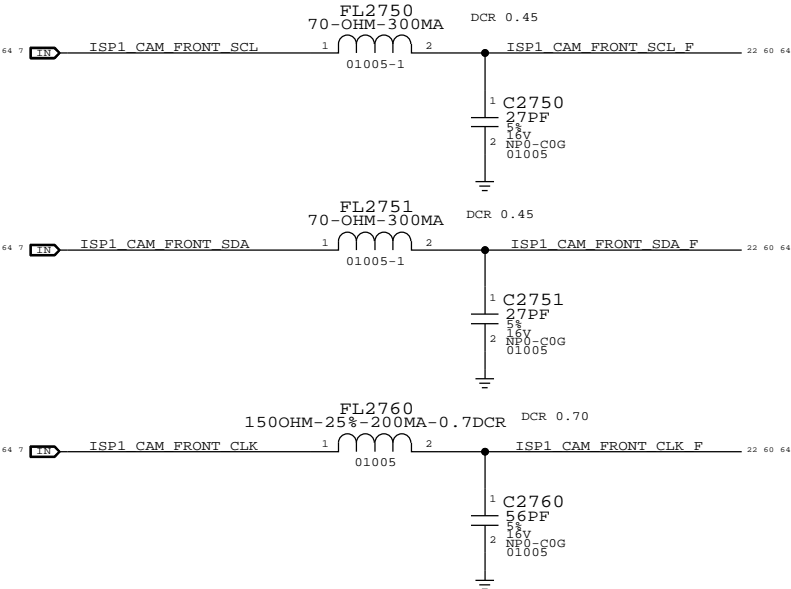
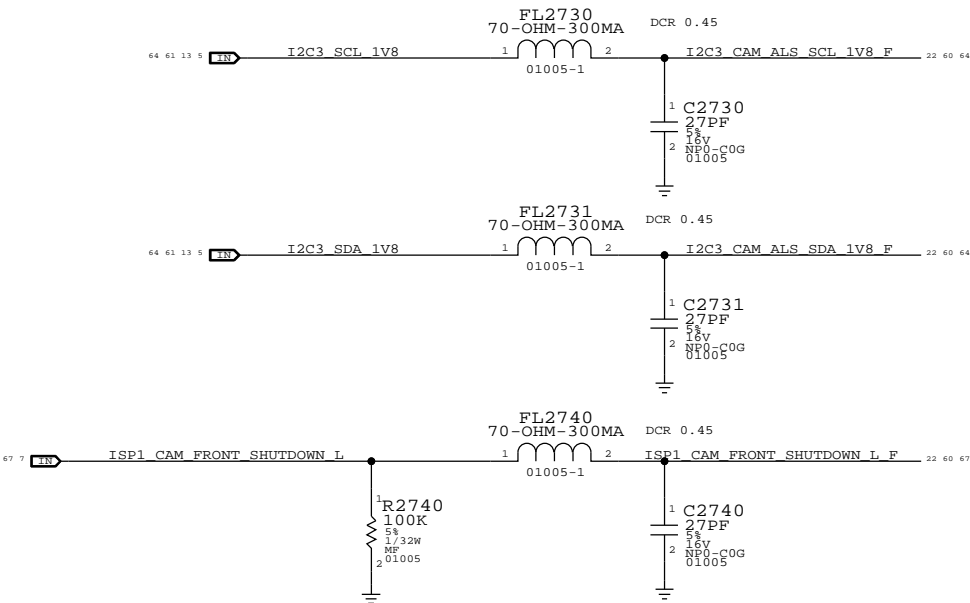
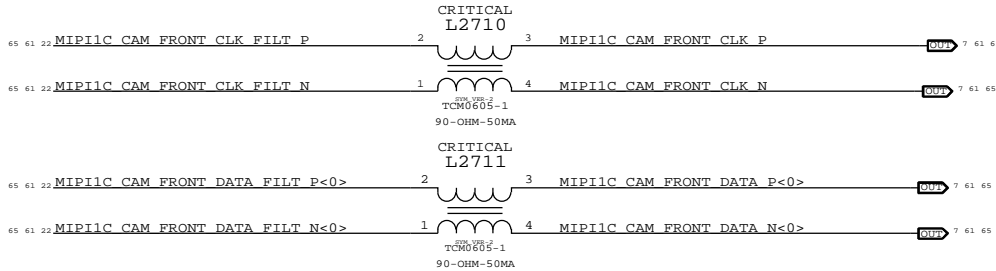
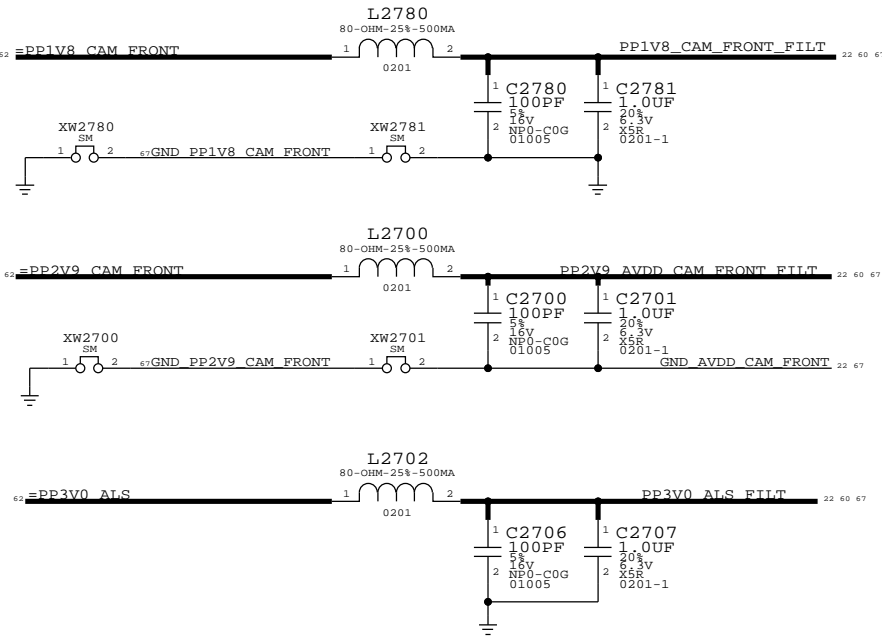
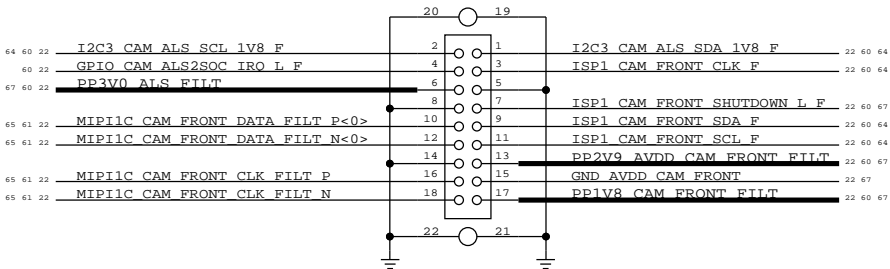


FRONT CAMERA CONNECTOR

J65 CAMERA CONNECTOR

APN:MLB 516S0876  
APN:FLEX 516S0869

CRITICAL  
J2700  
503548-1820  
F-ST-SM



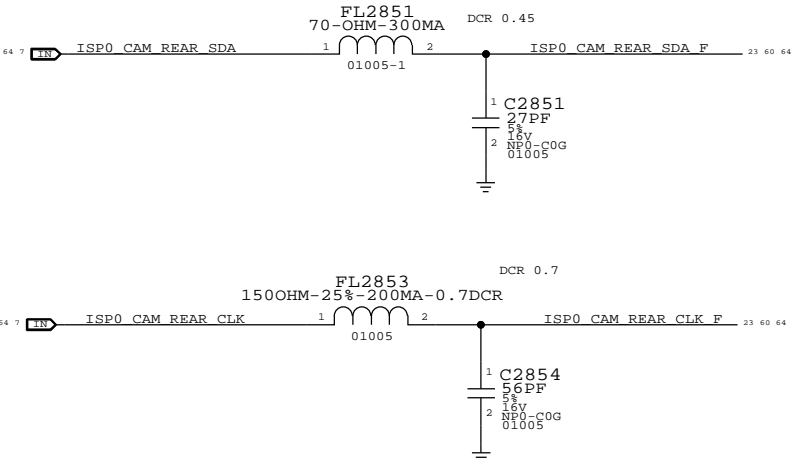
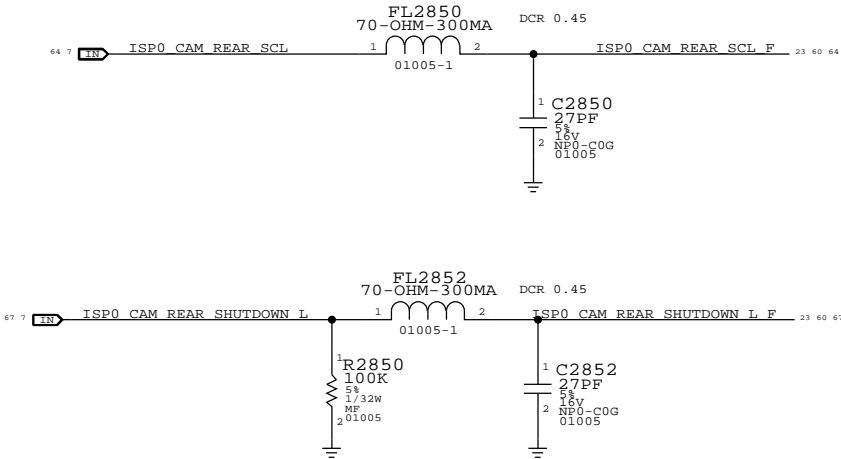
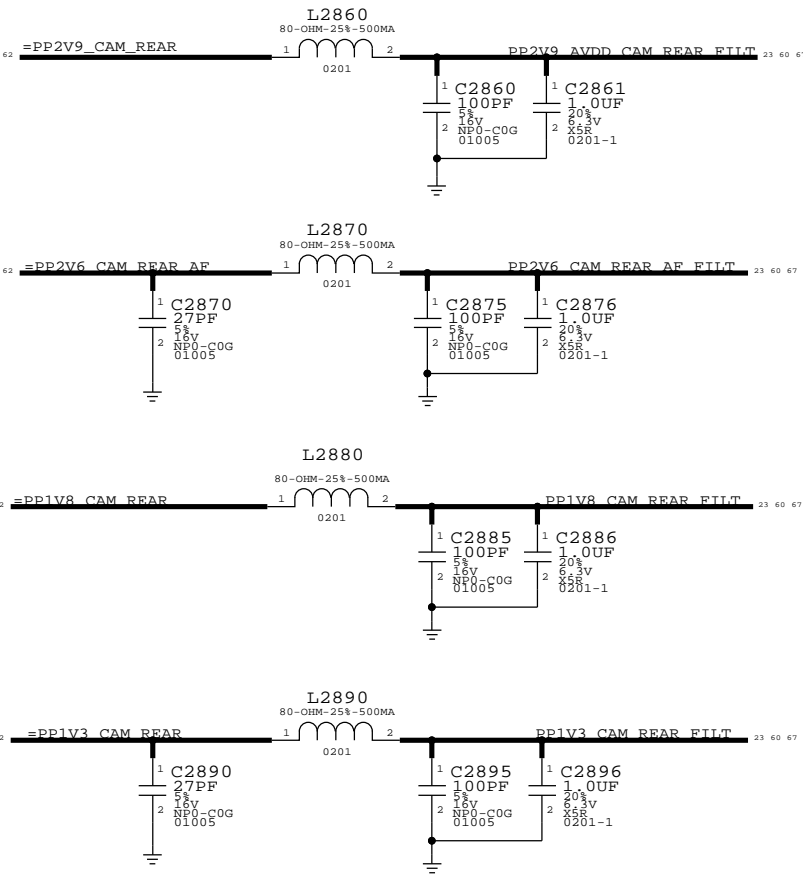
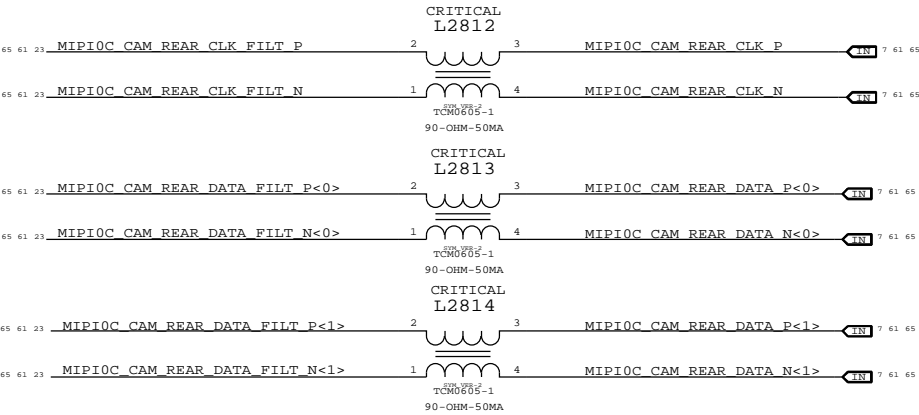
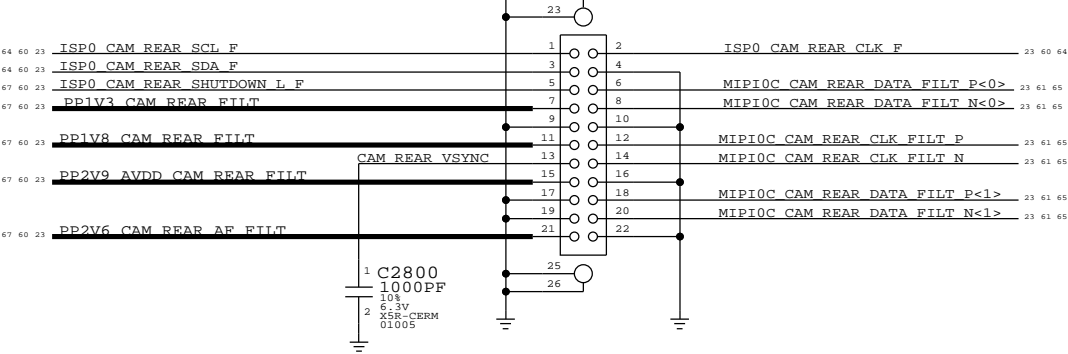
# REAR CAMERA CONNECTOR

FLEX: 516S0974

MLB: 516S0973

CRITICAL  
J2800  
AA07-S022VA1

F-ST-SM



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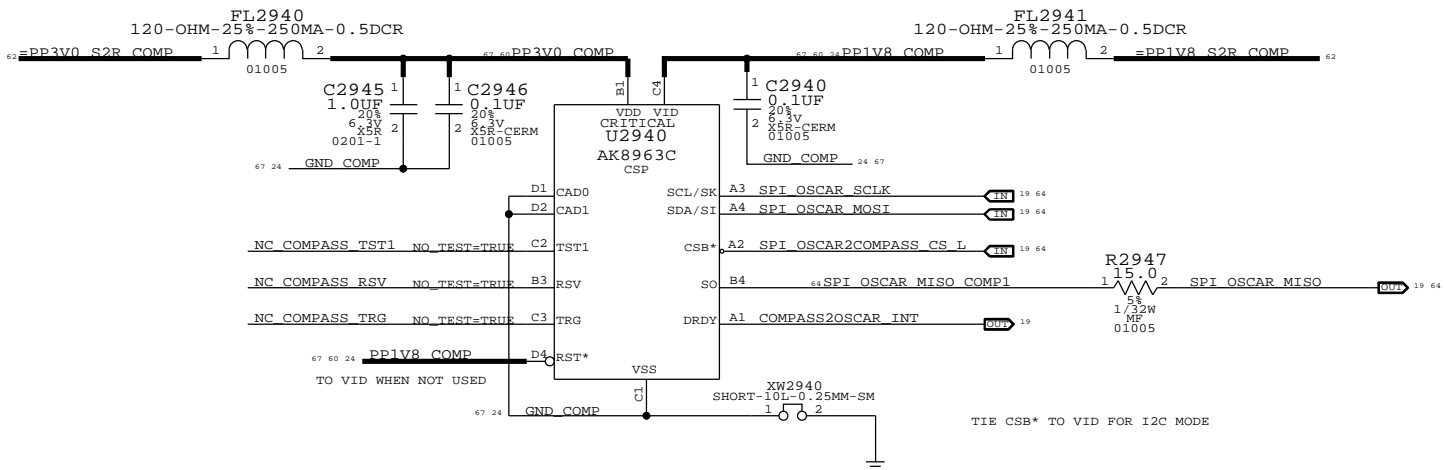
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# COMPASS

APN 338S1014

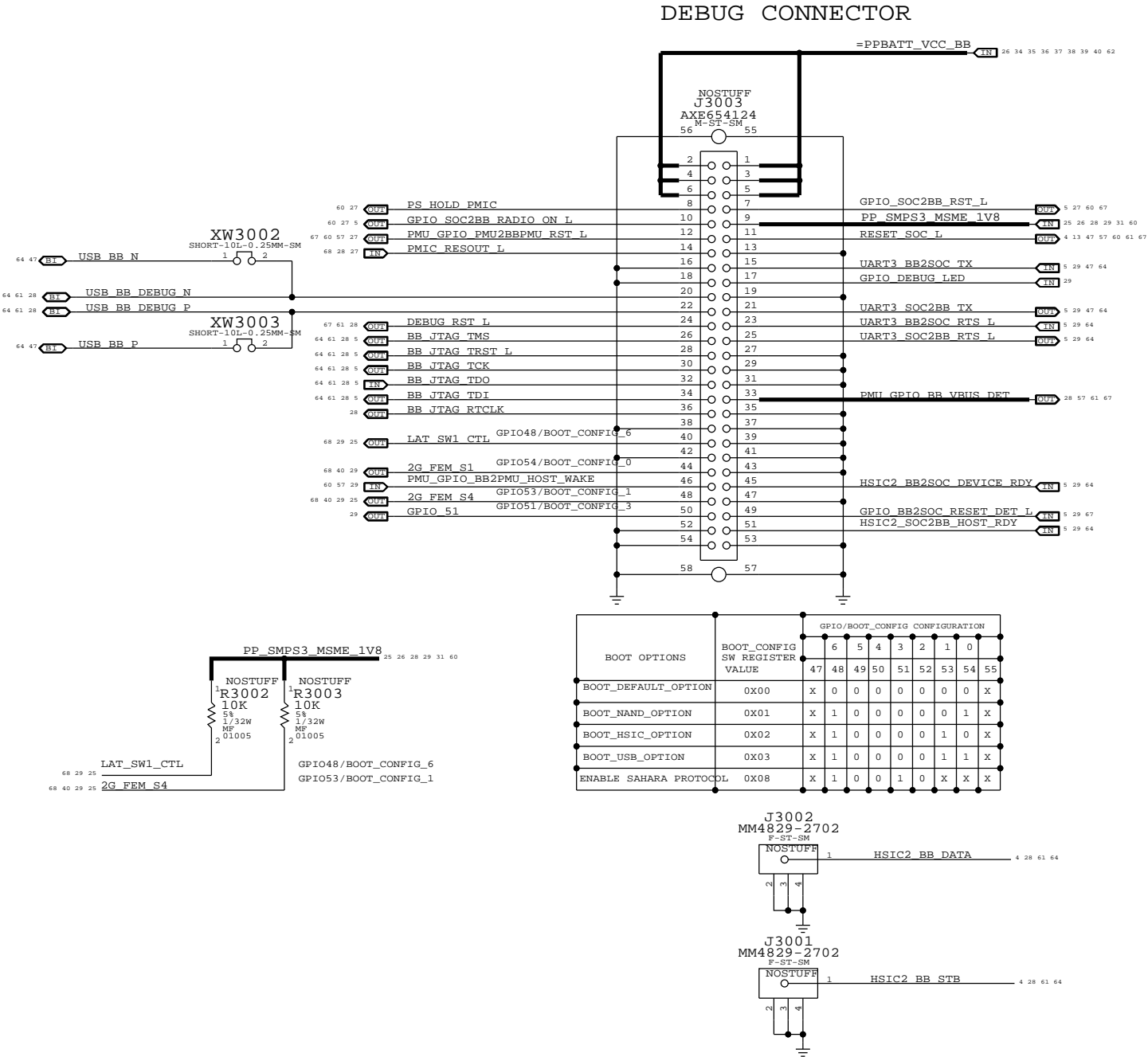


# AP INTERFACE & DEBUG CONNECTOR

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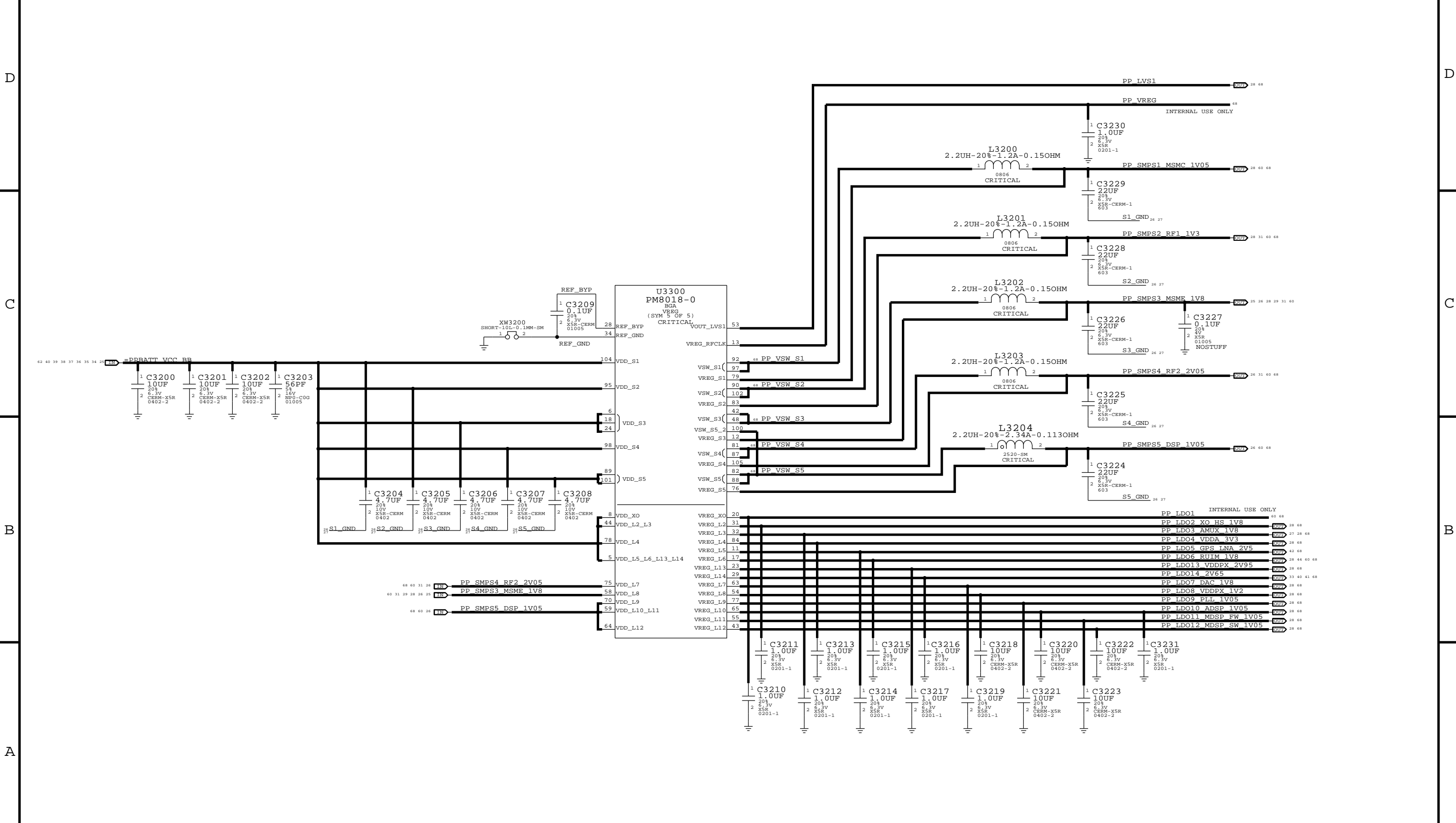
## PROBE POINTS

- PP3000  
P4MM  
SN  
EP 1 BB\_ERROR\_FLAG 29 68
- PP3001  
P4MM  
SN  
EP 1 SLEEP\_CLK\_32K 27 28 68
- PP3002  
P4MM  
SN  
EP 1 PMIC\_SSBI 27 28 68
- PP3003  
P4MM  
SN  
EP 1 19P2M\_MDM 27 28 68
- PP3008  
P4MM  
SN  
EP 1 WTR\_SSBI\_TX\_GPS 29 30
- PP3009  
P4MM  
SN  
EP 1 WTR\_SSBI\_PRX\_DRX 29 30
- PP3010  
P4MM  
SN  
EP 1 WTR\_RX\_ON 29 30 68
- PP3011  
P4MM  
SN  
EP 1 WTR\_RF\_ON 29 30 68
- PP3012  
P4MM  
SN  
EP 1 UART\_WLAN2BB\_LTE\_COEX 29 46
- PP3013  
P4MM  
SN  
EP 1 UART\_BB2WLAN\_LTE\_COEX 29 46





BASEBAND PMU ( 1 OF 2 )



# BASEBAND PMU ( 2 OF 2 )

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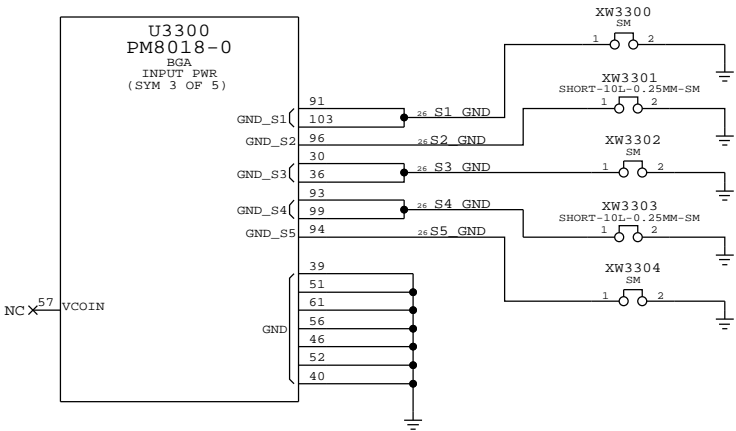
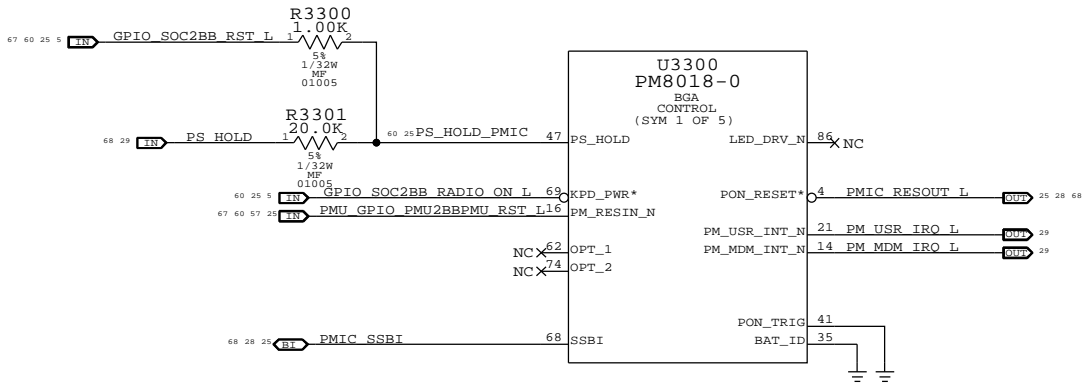
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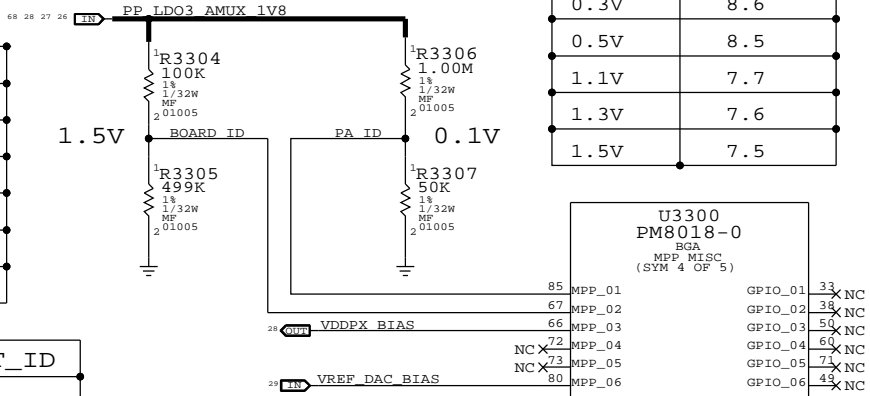
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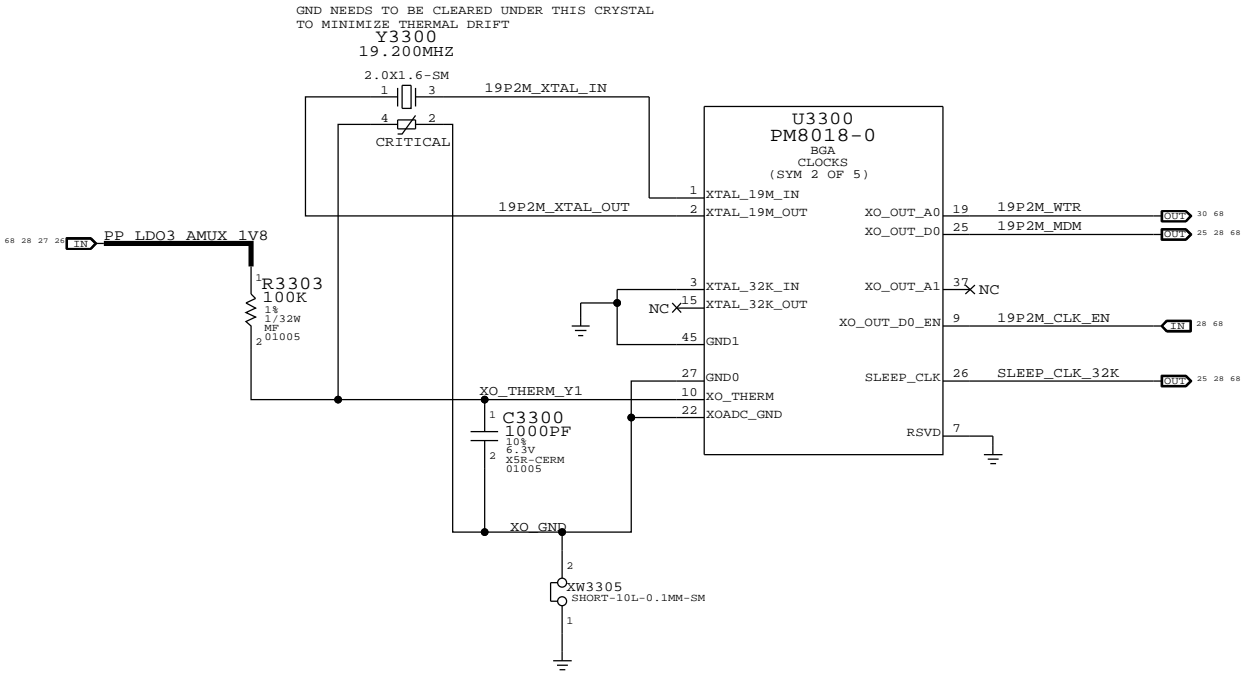


BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT

BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX



PA THERMISTOR REMOVED TO MATCH N41, AP SECTION  
NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.



# BASEBAND (1 OF 2)

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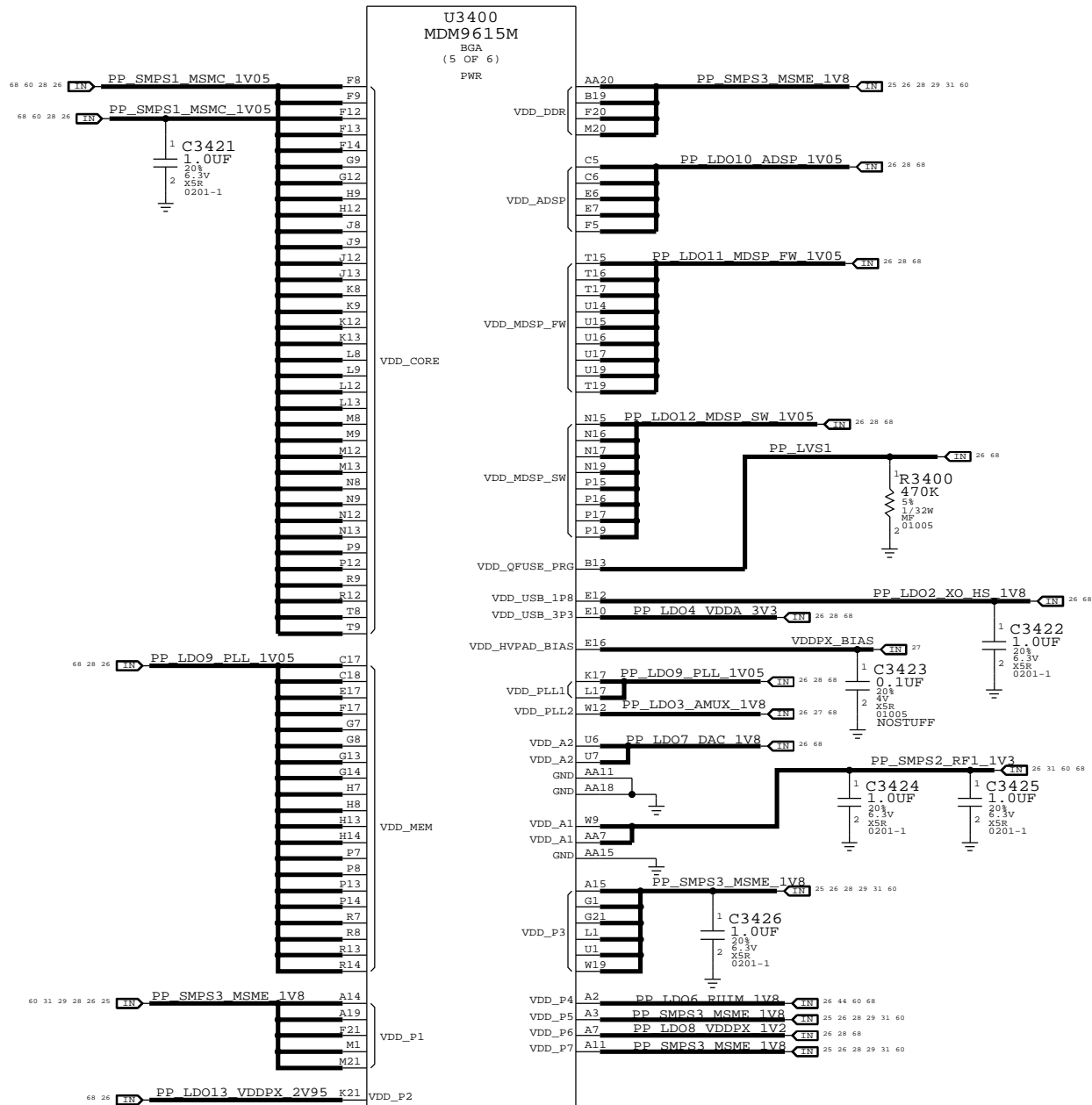
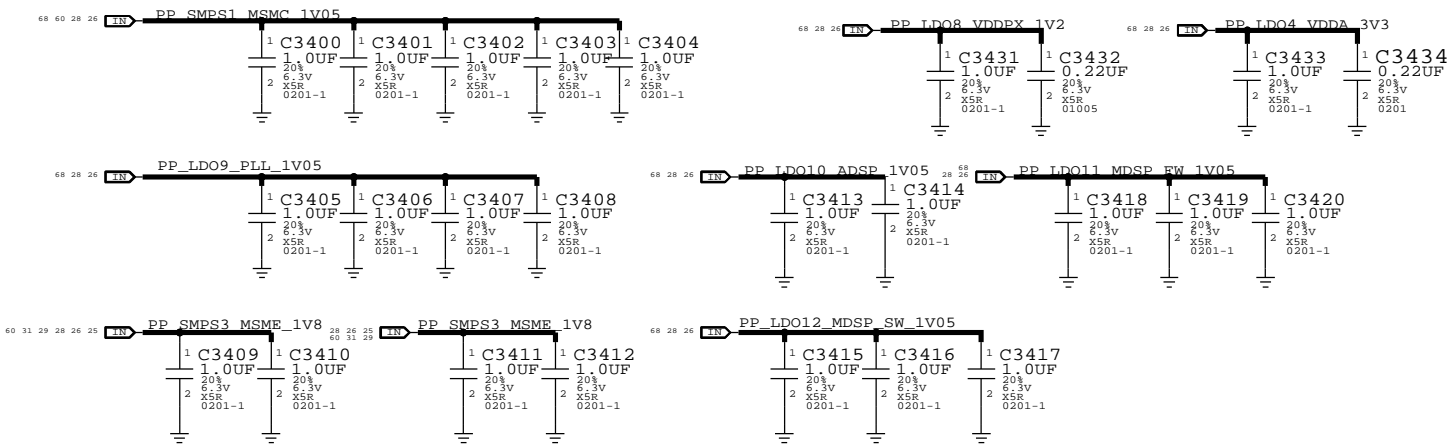
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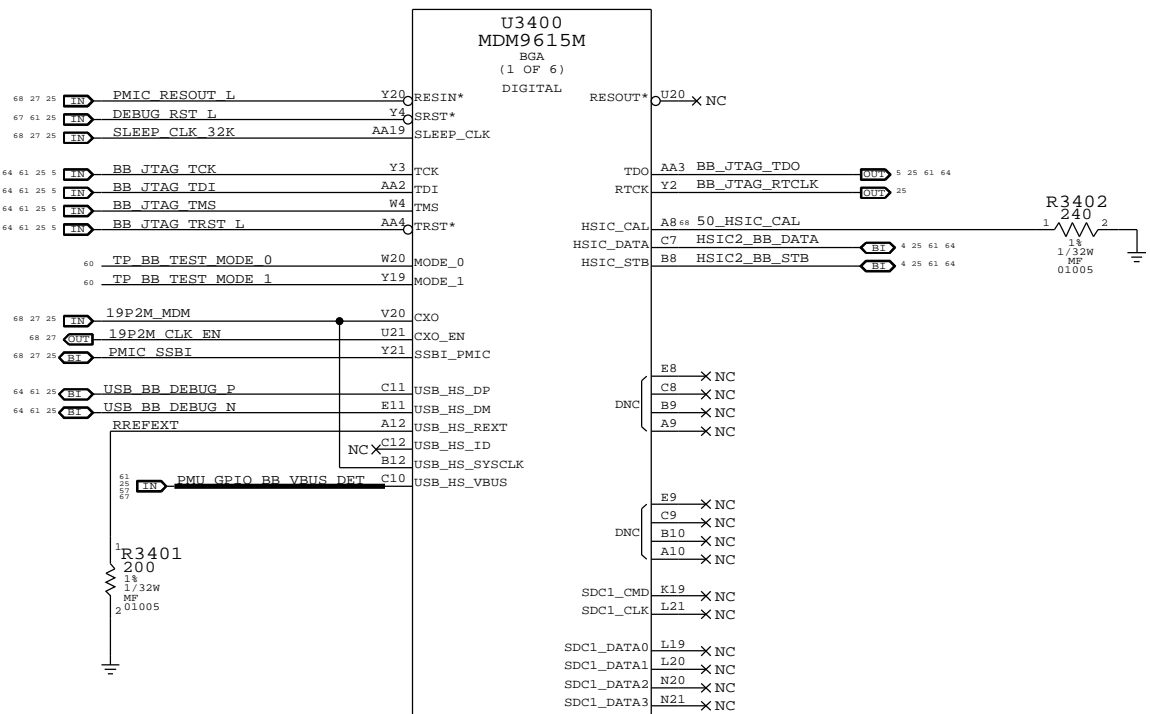
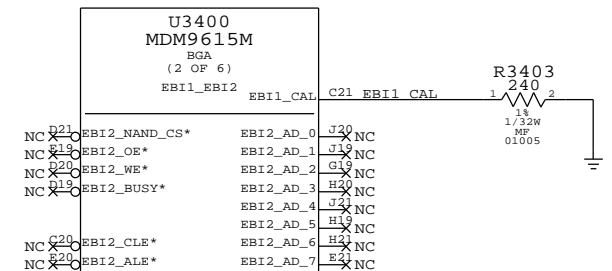
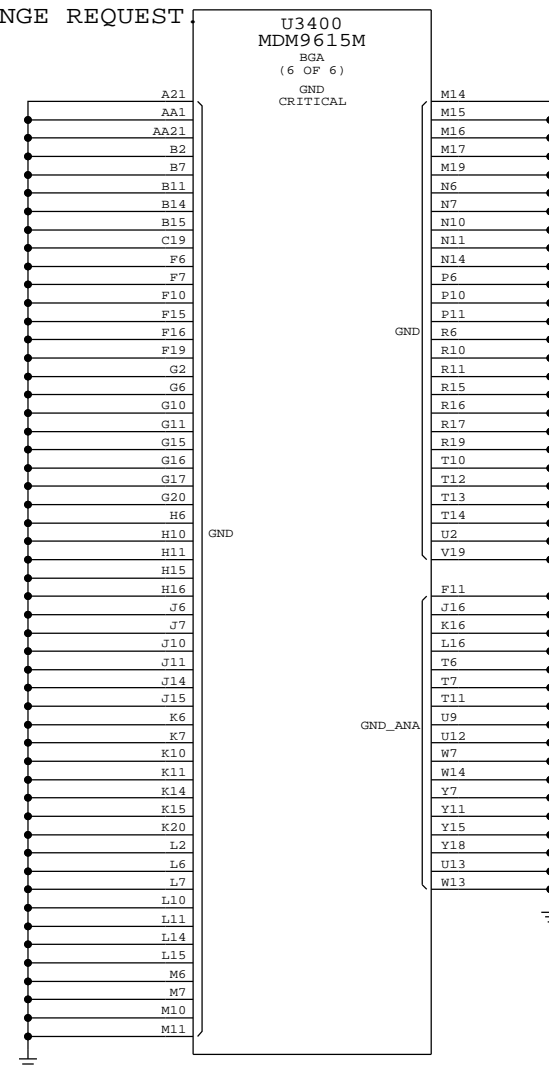
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BASEBAND ( 2 OF 2 )

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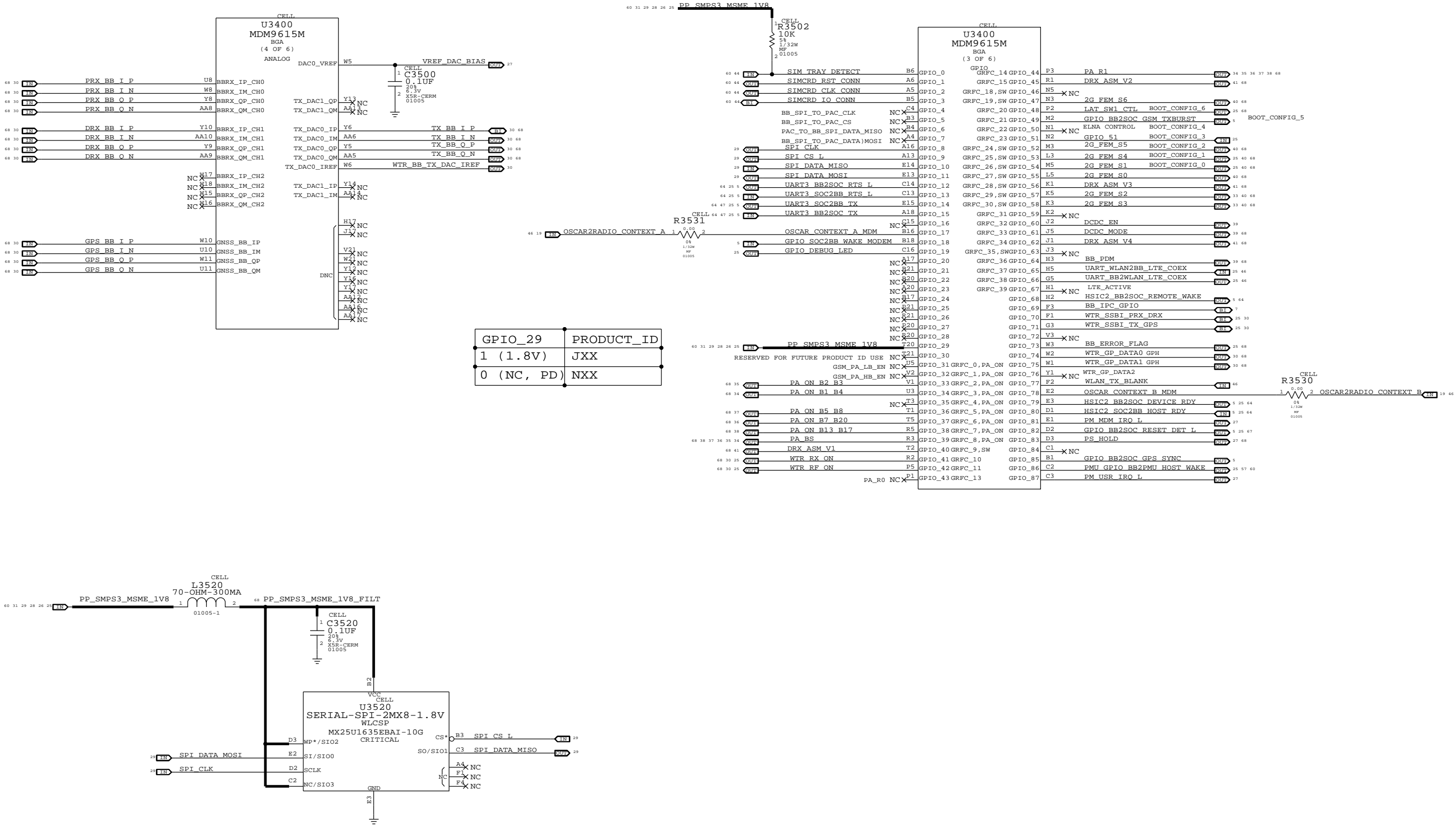
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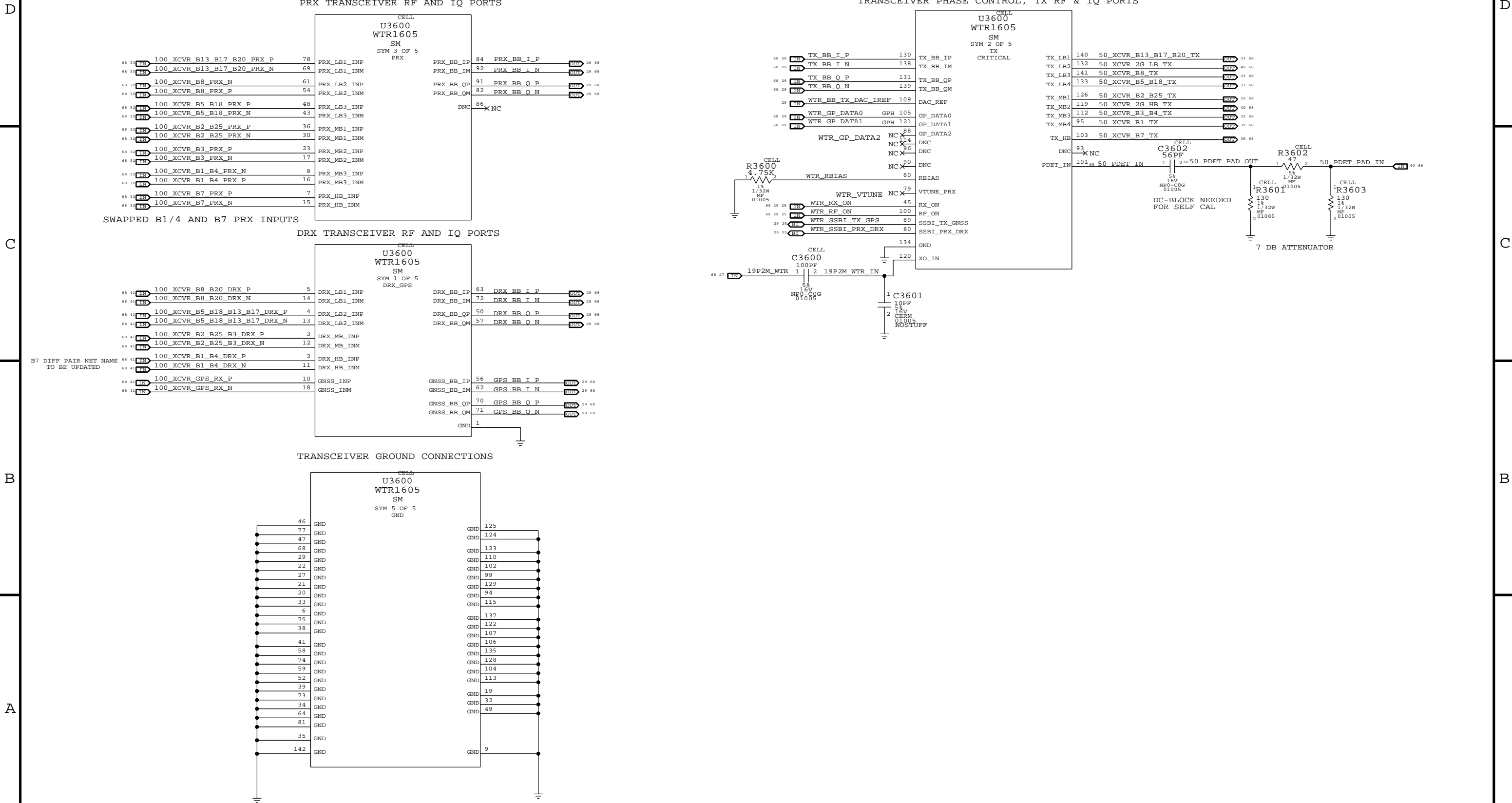
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## RF TRANSCEIVER ( 1 OF 2 )

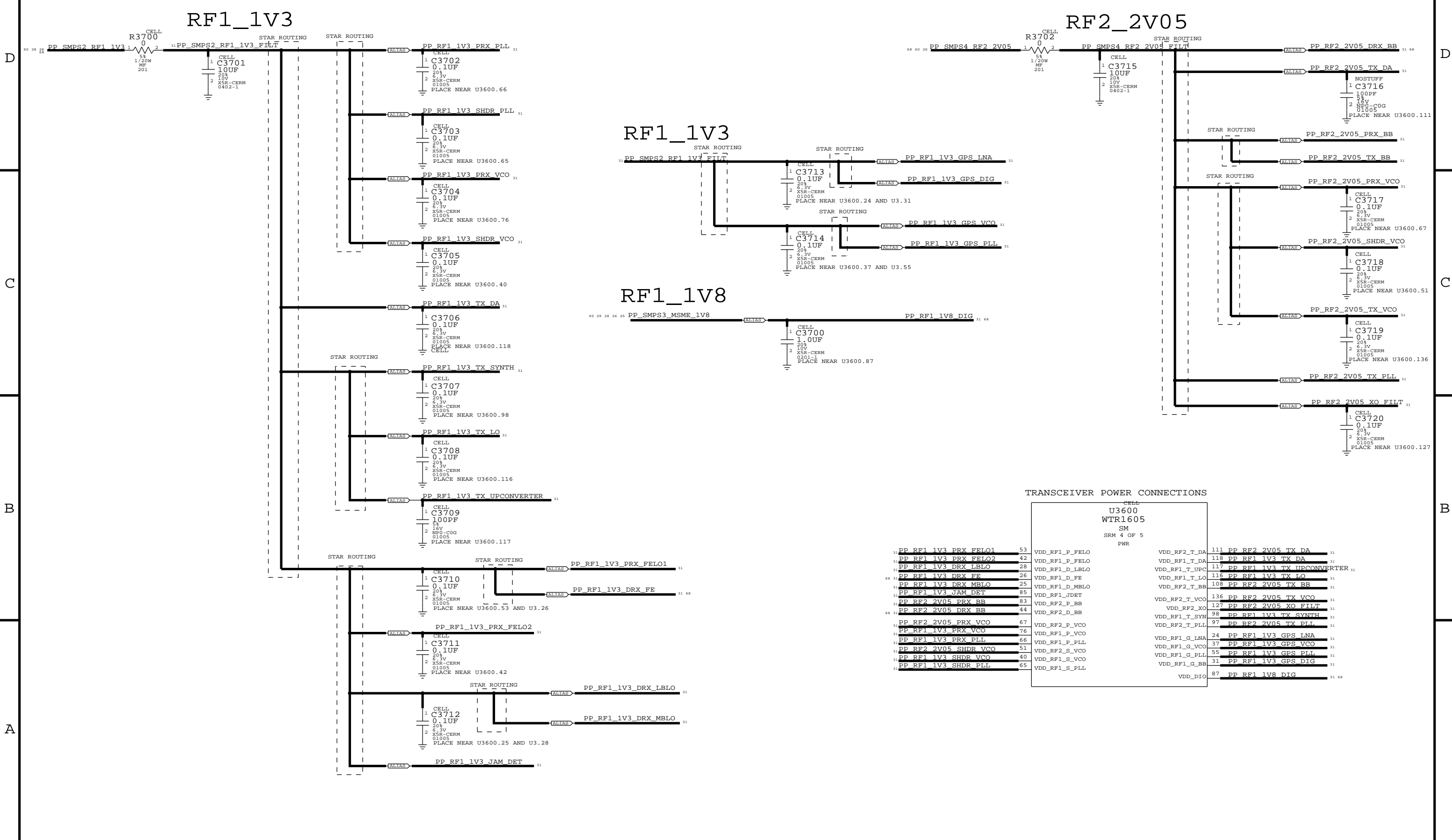
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RF TRANSCEIVER ( 2 OF 2 )

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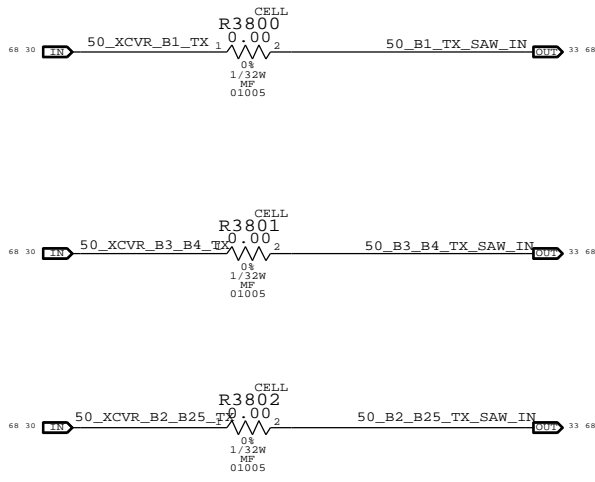
**TRANSCEIVER POWER CONNECTIONS**

<b>U3600</b> <b>WTR1605</b> <b>SM</b> <b>SRM 4 OF 5</b> <b>PWR</b>			
31	<b>PP RF1 1V3 PRX FELO1</b>	53	<b>VDD_RF1_P_FELO</b>
31	<b>PP RF1 1V3 PRX FELO2</b>	42	<b>VDD_RF1_P_FELO</b>
31	<b>PP RF1 1V3 DRX LBLO</b>	28	<b>VDD_RF1_D_LBLO</b>
68	<b>PP RF1 1V3 DRX FE</b>	26	<b>VDD_RF1_D_FE</b>
31	<b>PP RF1 1V3 DRX MBLO</b>	25	<b>VDD_RF1_D_MBLO</b>
31	<b>PP RF1 1V3 JAM DET</b>	85	<b>VDD_RF1_JDET</b>
31	<b>PP RF2 2V05 PRX BB</b>	83	<b>VDD_RF2_P_BB</b>
68	<b>PP RF2 2V05 DRX BB</b>	44	<b>VDD_RF2_D_BB</b>
31	<b>PP RF2 2V05 PRX VCO</b>	67	<b>VDD_RF2_P_VCO</b>
31	<b>PP RF1 1V3 PRX VCO</b>	76	<b>VDD_RF1_P_VCO</b>
31	<b>PP RF1 1V3 PRX PLL</b>	66	<b>VDD_RF1_P_PLL</b>
31	<b>PP RF2 2V05 SHDR VCO</b>	51	<b>VDD_RF2_S_VCO</b>
31	<b>PP RF1 1V3 SHDR VCO</b>	40	<b>VDD_RF1_S_VCO</b>
31	<b>PP RF1 1V3 SHDR PLL</b>	65	<b>VDD_RF1_S_PLL</b>
31		87	<b>VDD_DIO</b>
31		111	<b>PP RF2 2V05 TX DA</b>
31		118	<b>PP RF1 1V3 TX DA</b>
31		117	<b>PP RF1 1V3 TX UPCONVERTER</b>
31		116	<b>PP RF1 1V3 TX LO</b>
31		108	<b>PP RF2 2V05 TX BB</b>
31		136	<b>PP RF2 2V05 TX VCO</b>
31		127	<b>PP RF2 2V05 XO FILT</b>
31		98	<b>PP RF1 1V3 TX SYNTH</b>
31		97	<b>PP RF2 2V05 TX PLL</b>
31		24	<b>PP RF1 1V3 GPS LNA</b>
31		37	<b>PP RF1 1V3 GPS VCO</b>
31		55	<b>PP RF1 1V3 GPS PLL</b>
31		31	<b>PP RF1 1V3 GPS DIG</b>
68		87	<b>PP RF1 1V8 DIG</b>

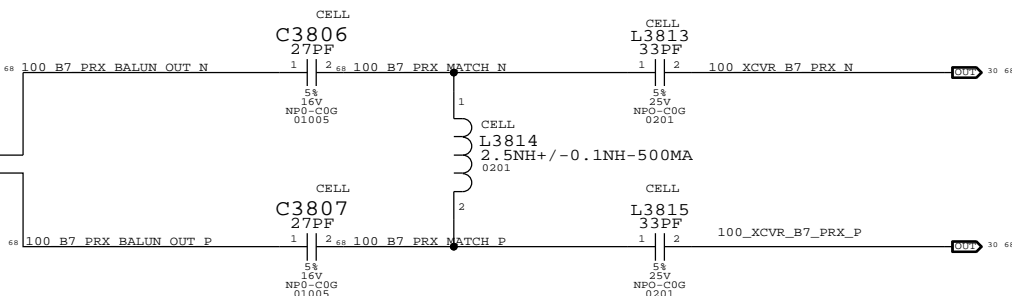
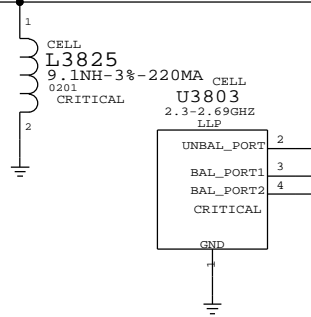


# TRANSCEIVER TX AND RX MATCHING NETWORKS

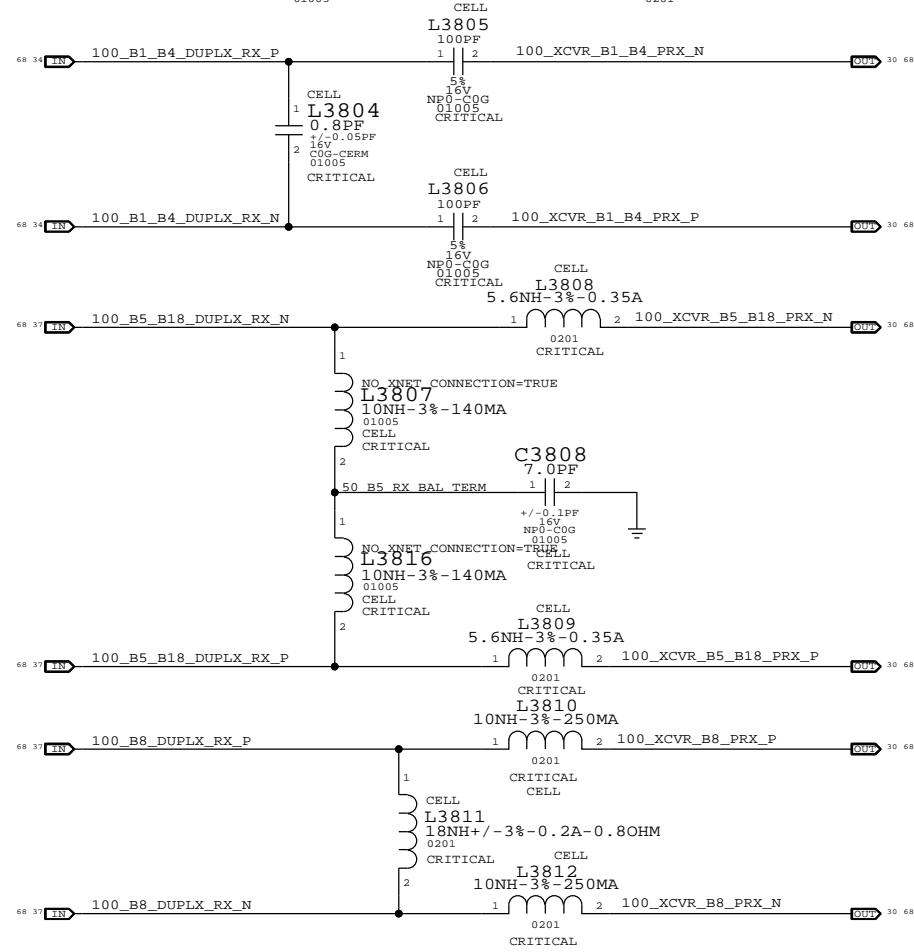
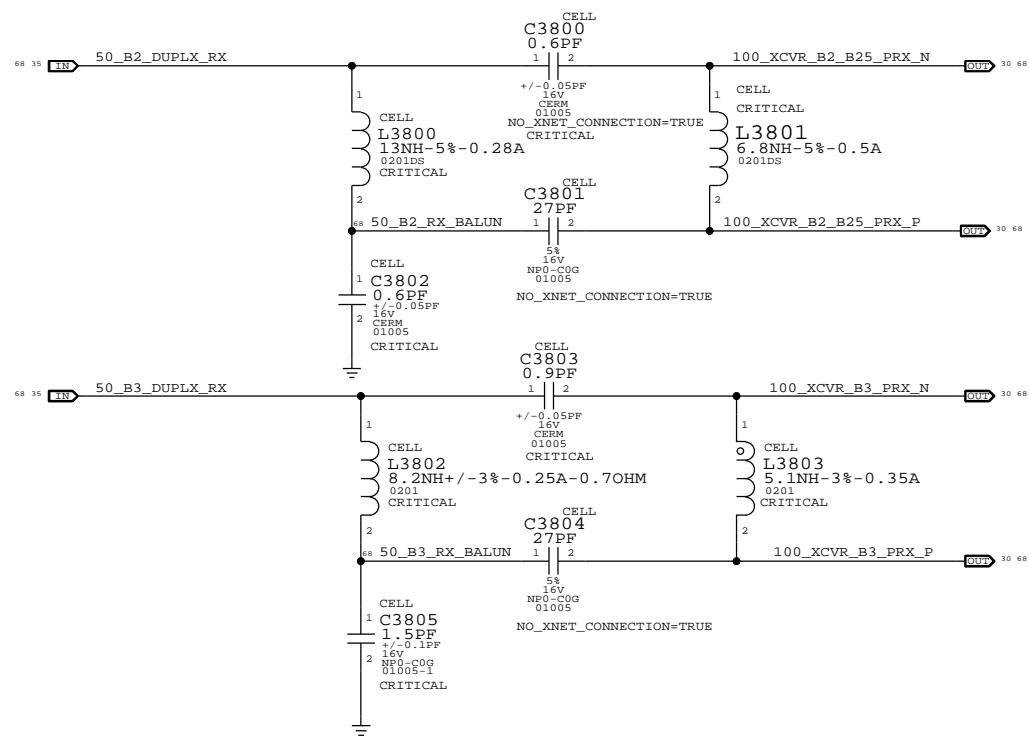
## TX MATCHING NETWORKS



50 B7 DUPLX RX



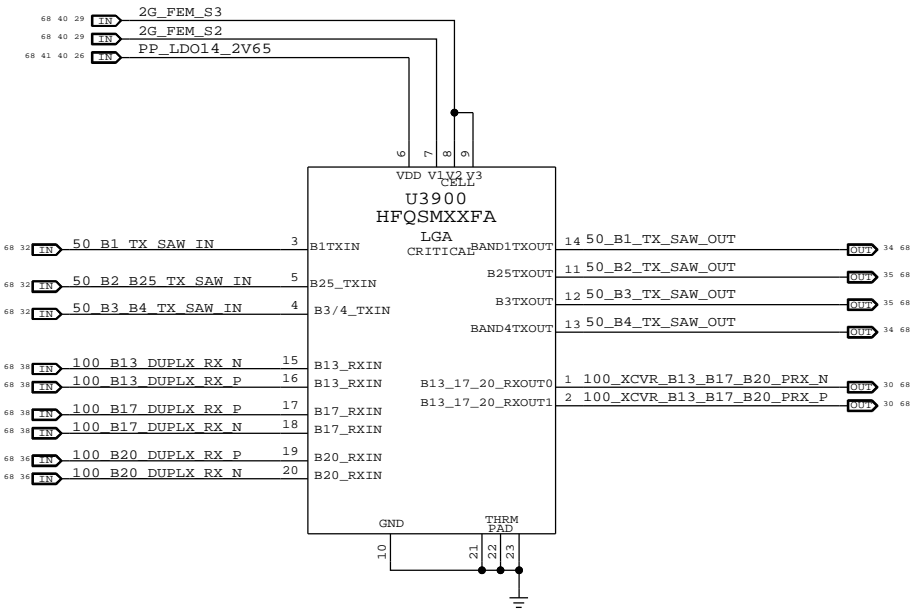
## RX MATCHING NETWORKS



# SAW BANK

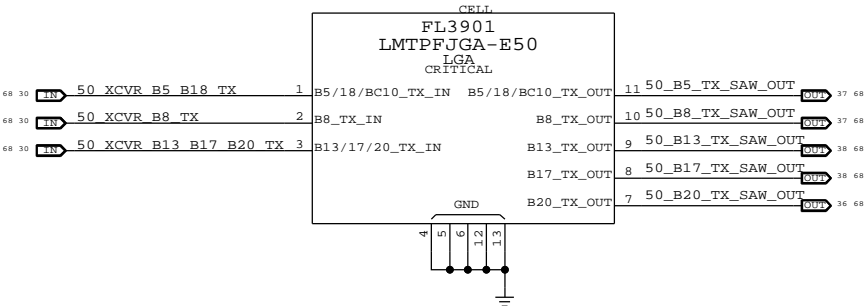
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

## HB TX SAW BANK + B13/B17/B20 DP6T SWITCH AND MATCHING



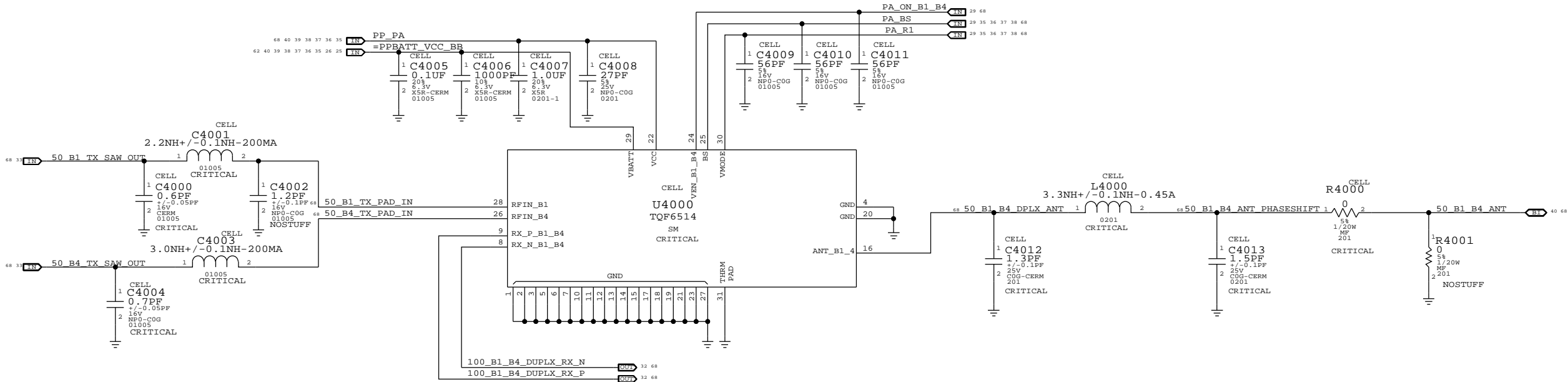
BAND	V3=V2	V1
B3 TX	HIGH	X
B4 TX	LOW	X
B13 RX	HIGH	HIGH
B17 RX	HIGH	LOW
B20 RX	LOW	HIGH

## LB TX SAW BANK



# BAND 1 / 4 PAD

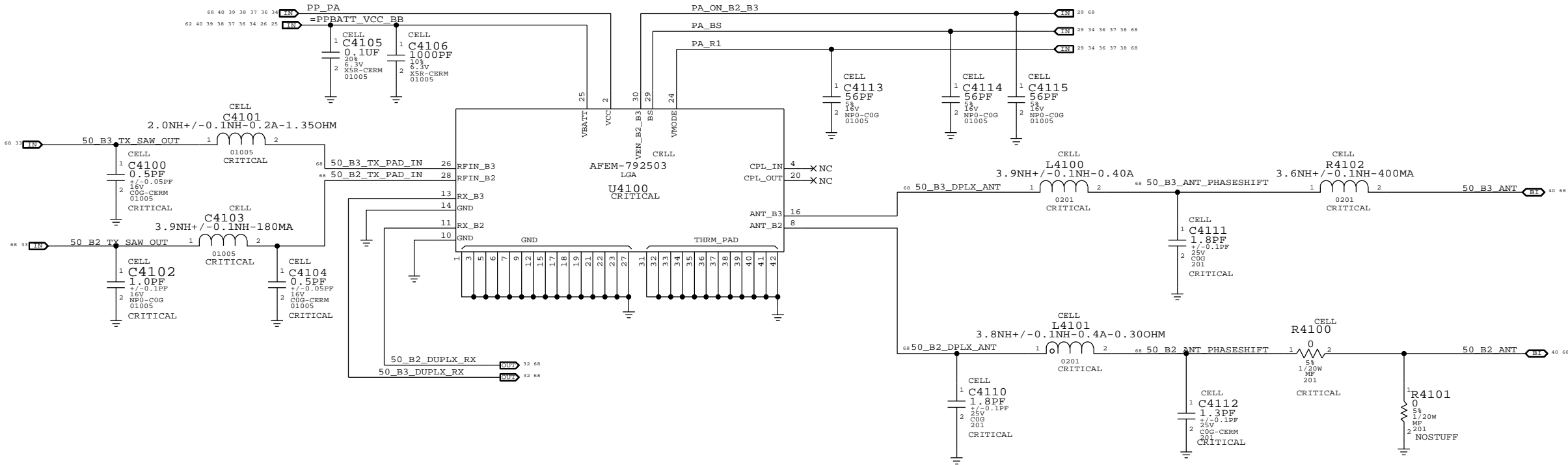
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA	POWER	MODE	PA_BS	PA_ON_B1_B4	PA_R1
=====	=====	=====	=====	=====	=====	=====
POWER DOWN		X		0	0	0
STANDBY		X		X	0	X
B4		HPM		0	1	0
B4		LPM		0	1	1
B1		HPM		1	1	0
B1		LPM		1	1	1

# BAND 2 / 3 PAD

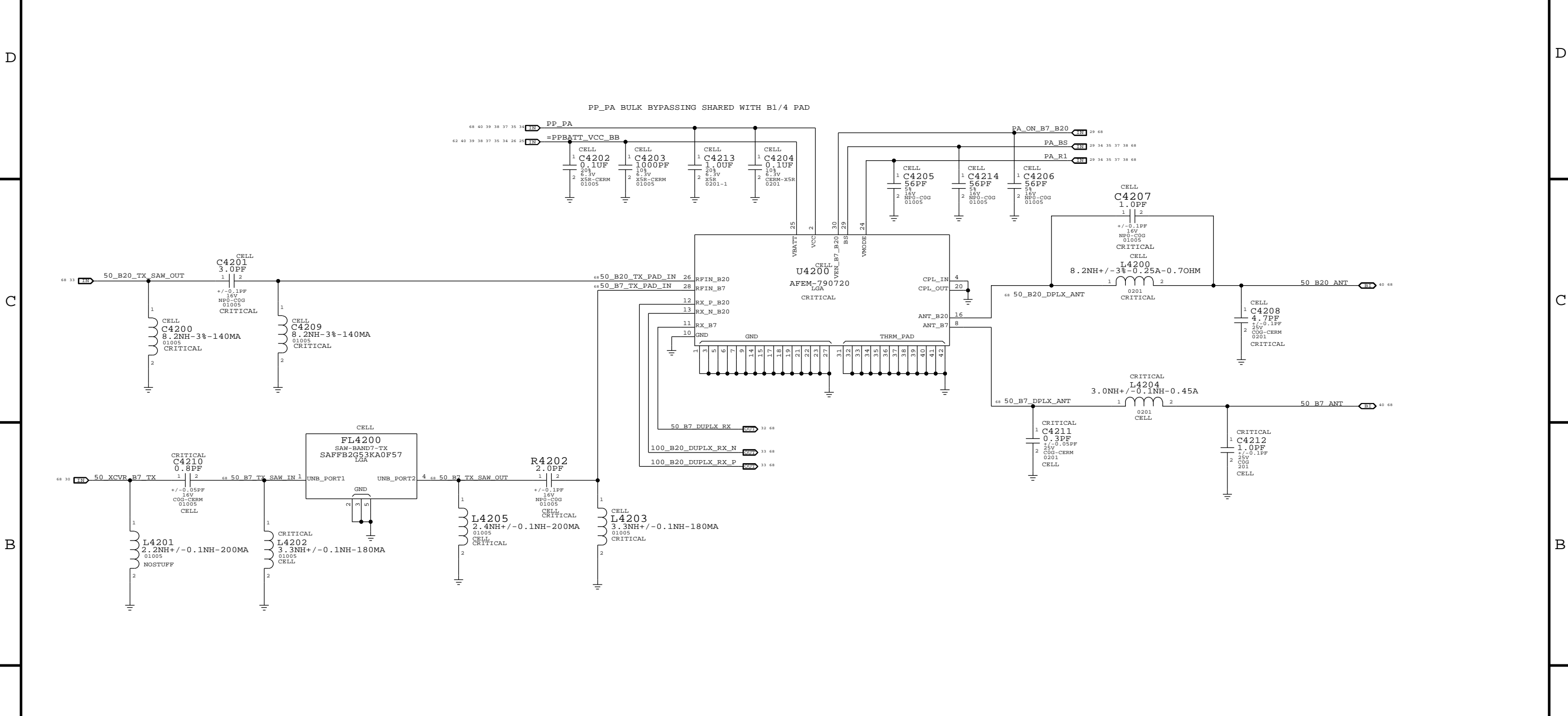
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA	POWER	MODE	PA_BS	PA_ON_B2_B3	PA_R1
=====	=====	=====	=====	=====	=====	=====
POWER DOWN		X		0	0	0
STANDBY		X		X	0	X
B3		HPM		0	1	0
B3		LPM		0	1	1
B2		HPM		1	1	0
B2		LPM		1	1	1

BAND 20/7 PAD

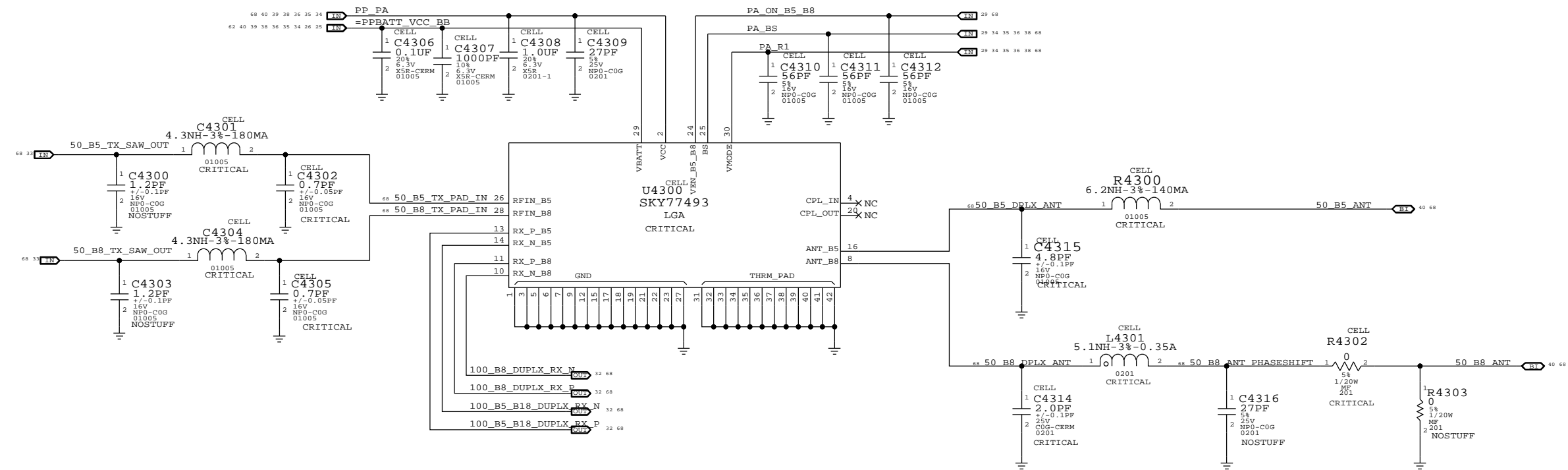
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA_ON_B20	PA_R1
POWER DOWN	LPM	0	0
STANDBY	X	0	X
B20	HPM	1	0
B20	LPM	1	1

# BAND 5 / 8 PAD

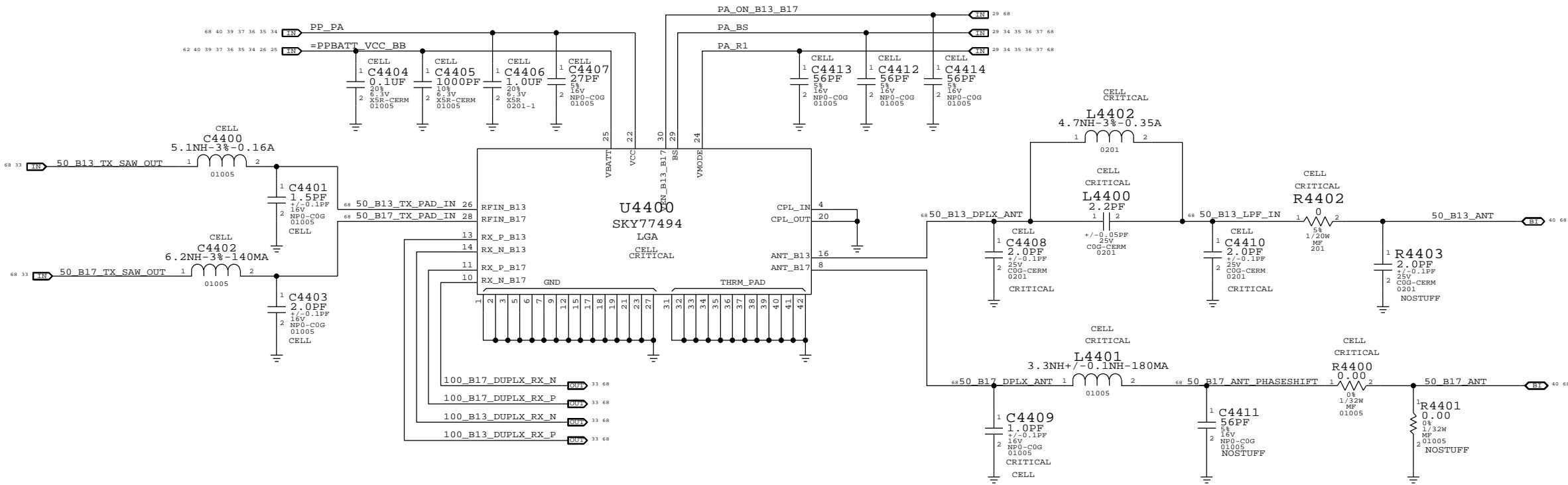
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA	POWER	MODE	PA_BS	PA_ON_B5_B8	PA_R1
=====	=====	=====	=====	=====	=====	=====
POWER DOWN		X		0	0	0
STANDBY		X		X	0	X
B5		HPM		0	1	0
B5		LPM		0	1	1
B8		HPM		1	1	0
B8		LPM		1	1	1

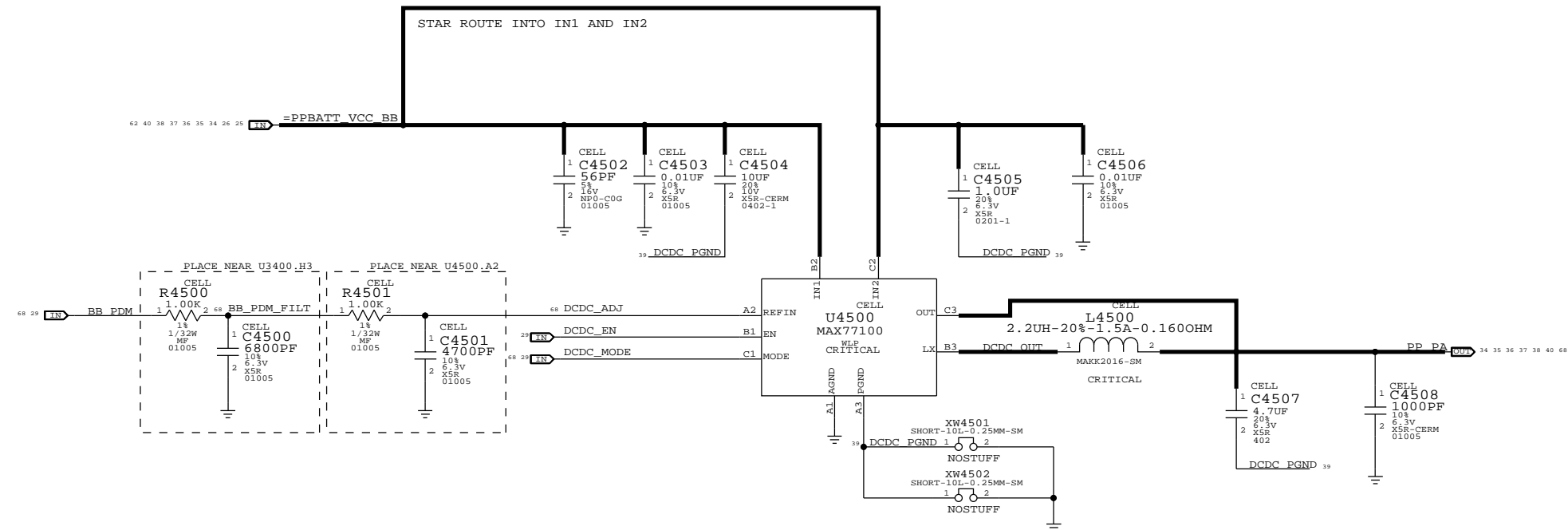
# BAND 13/17 PAD

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA_BS	PA_ON_B13_B17	PA_R1
=====	=====	=====	=====	=====
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B17	HPM	0	1	0
B17	LPM	0	1	1
B13	HPM	1	1	0
B13	LPM	1	1	1

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

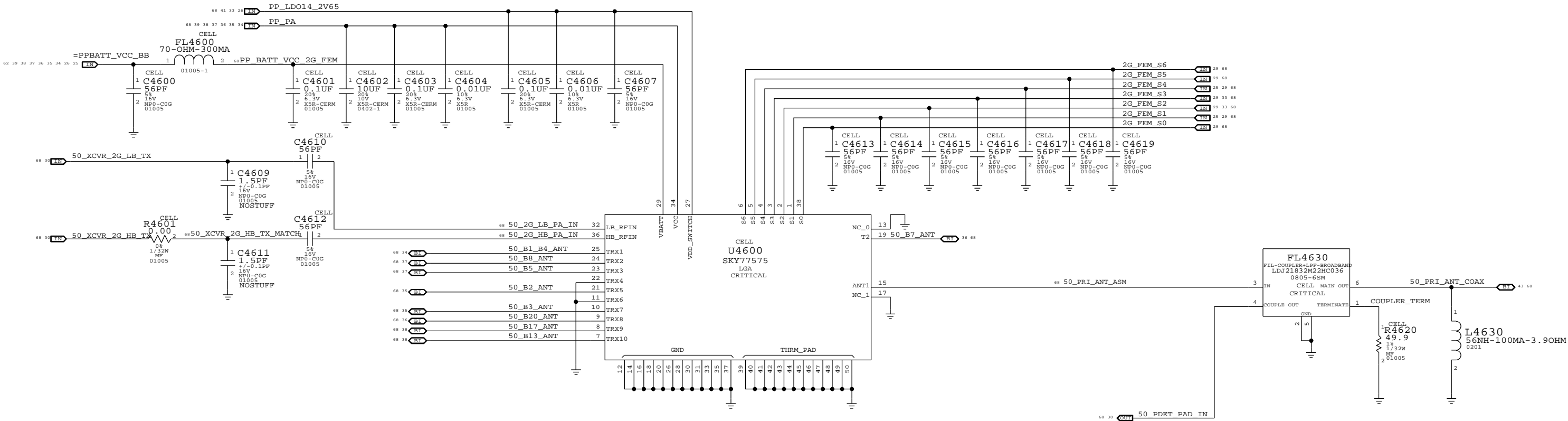




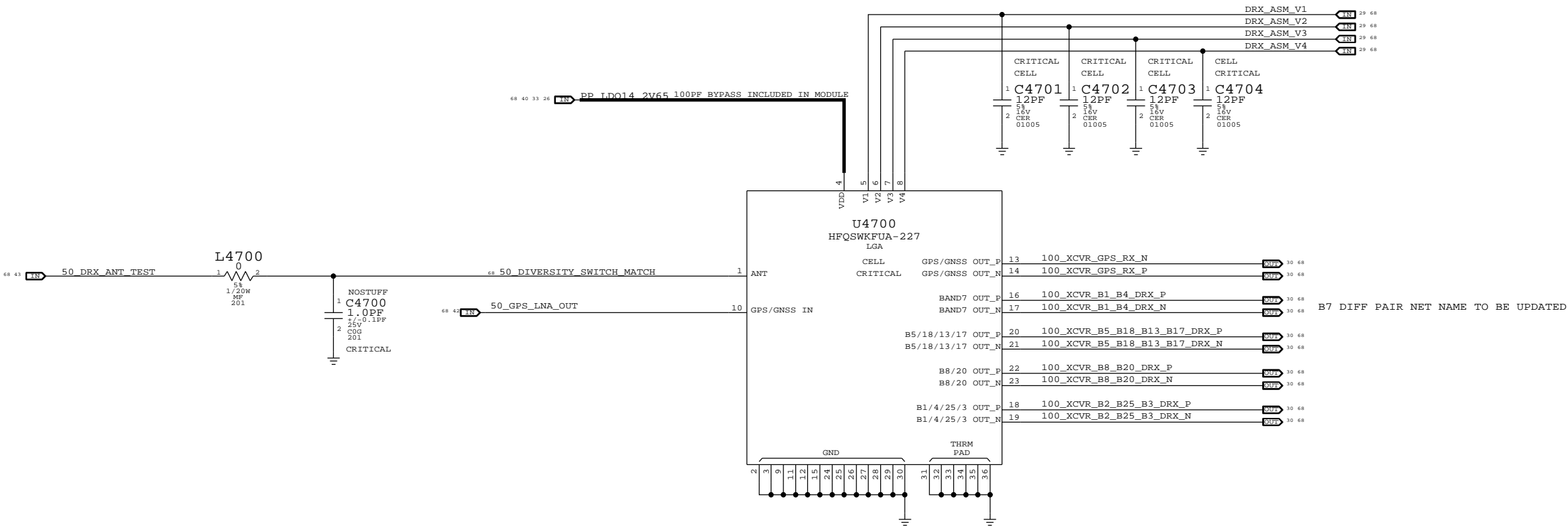
# 2G FEM

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

## 2G FEM



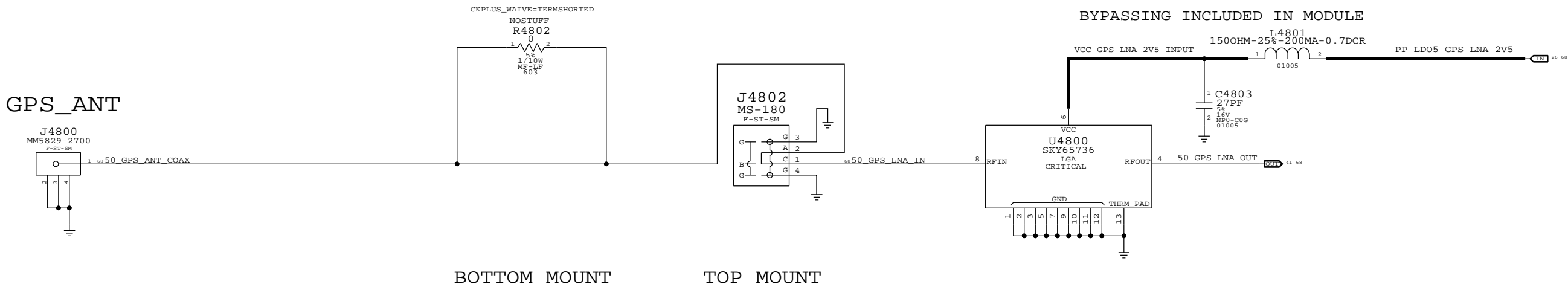
# RX DIVERSITY



NEED TO UPDATE

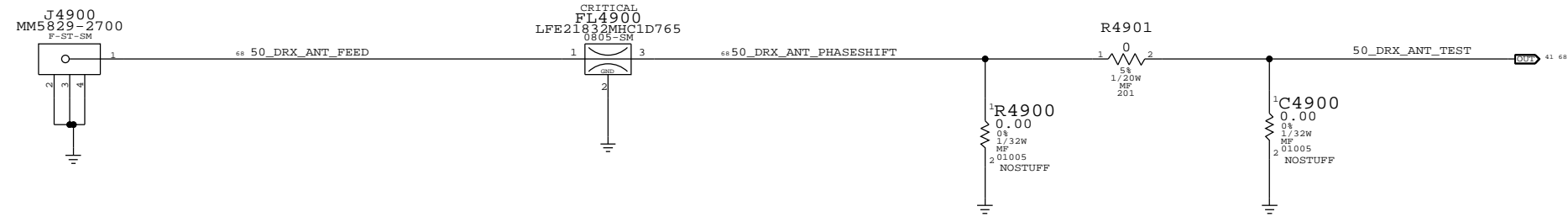
BAND	DRX_ASM_V4	DRX_ASM_V3	DRX_ASM_V2	DRX_ASM_V1
B1/B4	LOW	LOW	LOW	LOW
B2/25	LOW	HIGH	LOW	LOW
B3	HIGH	LOW	LOW	LOW
B5/6/18	LOW	LOW	HIGH	LOW
B8	LOW	LOW	LOW	HIGH
B13/17	LOW	HIGH	HIGH	HIGH
B20	LOW	HIGH	HIGH	LOW
OFF	LOW	LOW	HIGH	HIGH
SWITCH IS TERMINATED IN ALL OTHER POSSIBLE STATES				

GPS

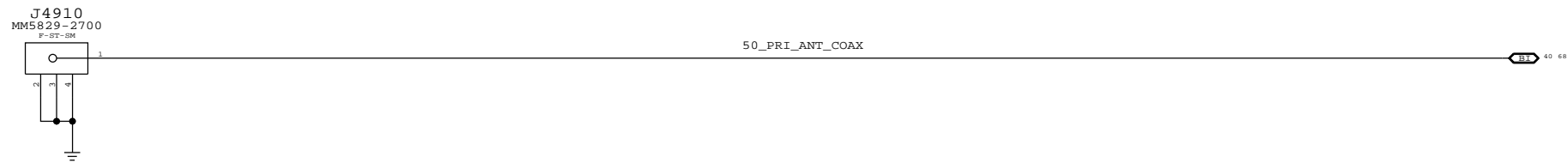


# ANTENNA FEEDS

## DRX\_ANT COAX



## PRI\_ANT COAX



D

C

B

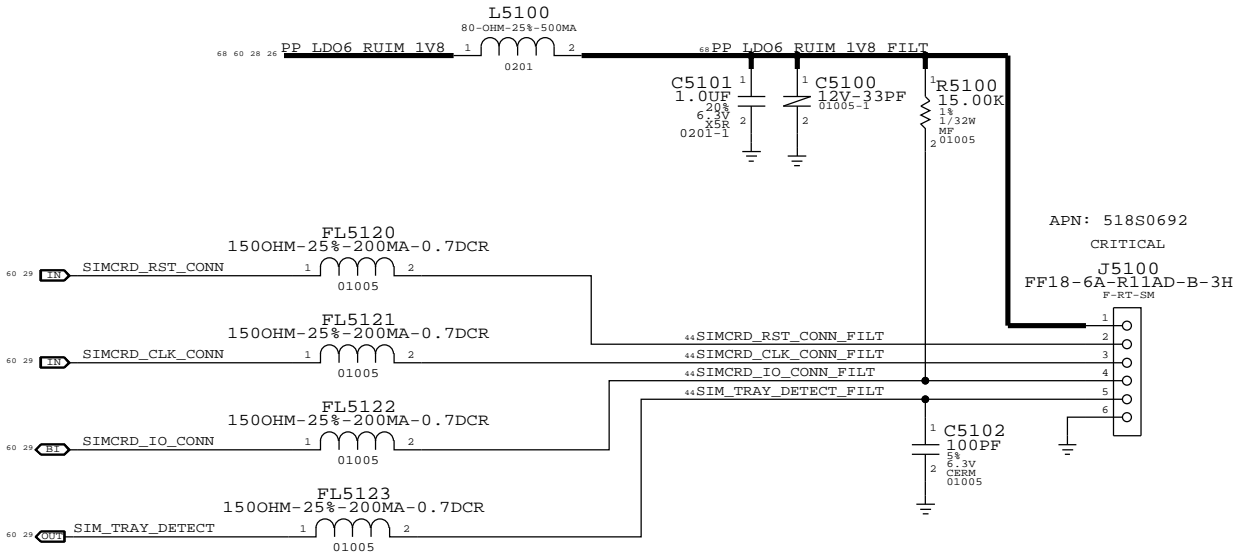
A

D

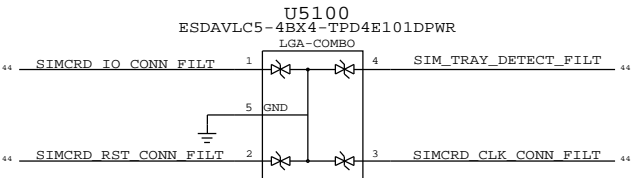
C

B

SIM CARD FLEX CONN

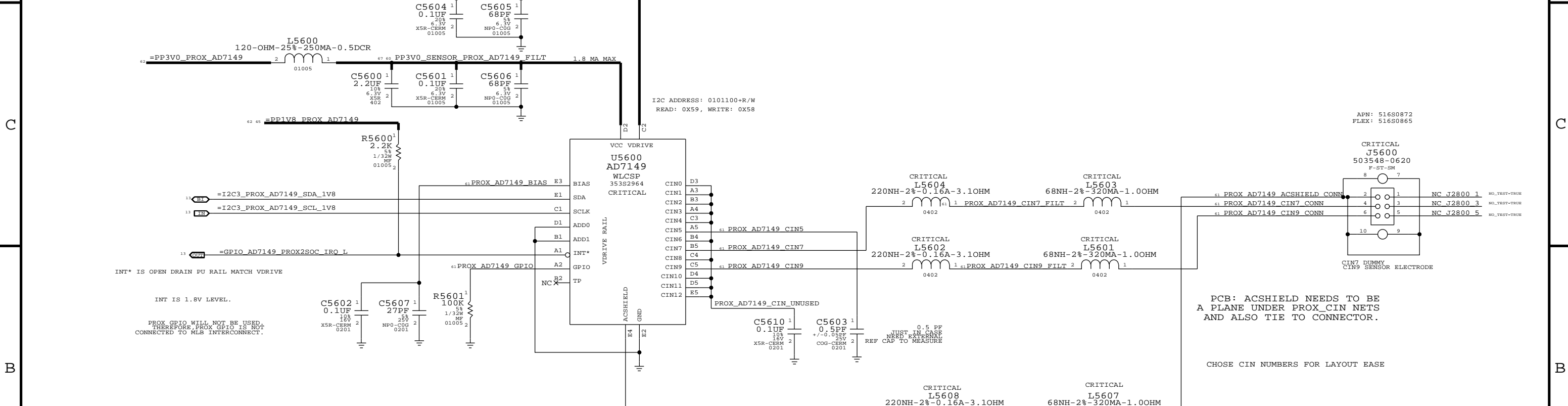


SIM CARD ESD PROTECTION



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0130	377S0159	?	U5100	RDAR: //PROBLEM/12840016

D | PROX SENSOR | D



PCB: ENSURE ACSHIELD PLANE UNDER  
U3200, NO GND PLANE NEAR PROX\_CIN NETS..

# WIFI/BT: MODULE

D

D

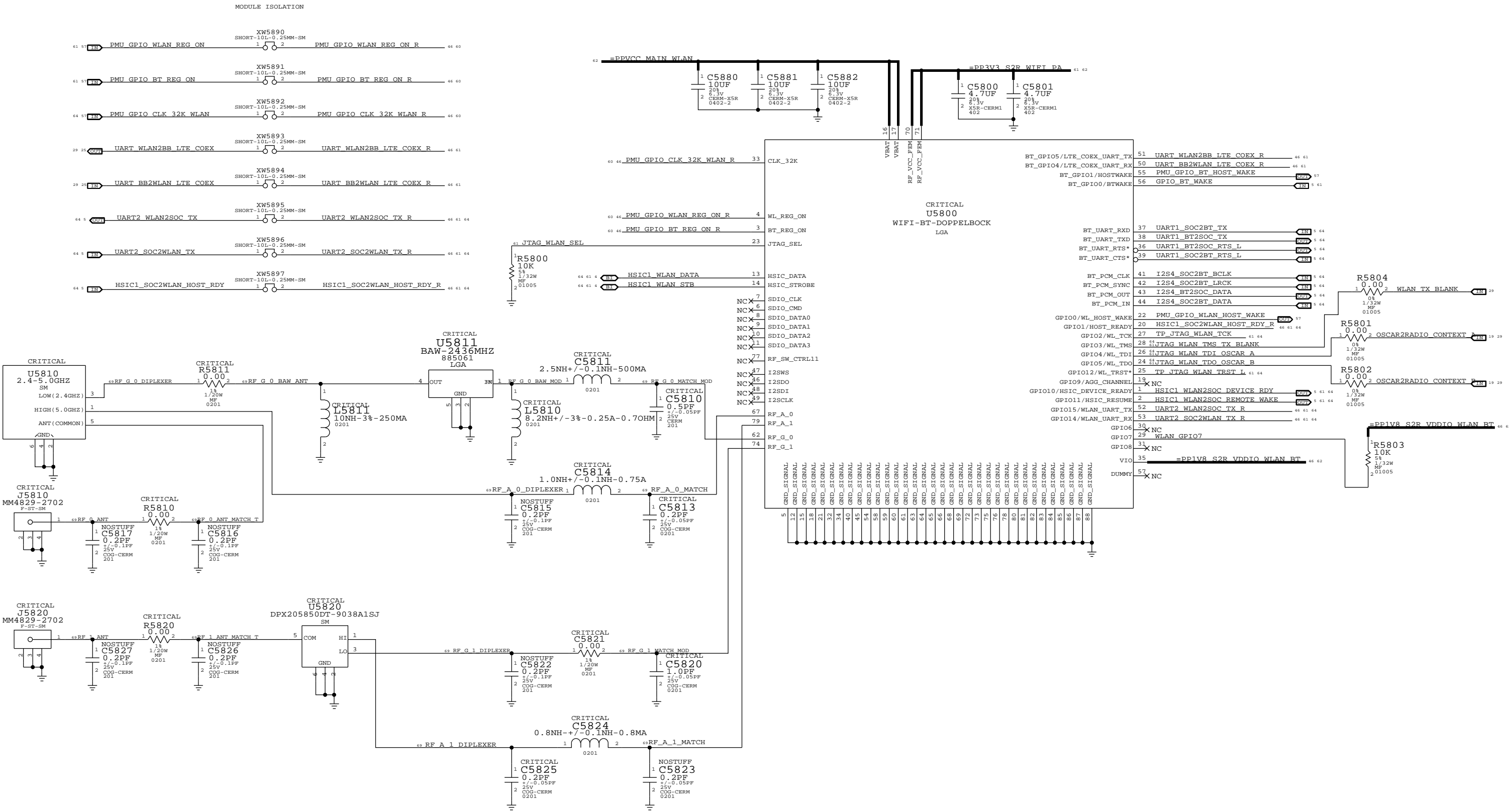
C

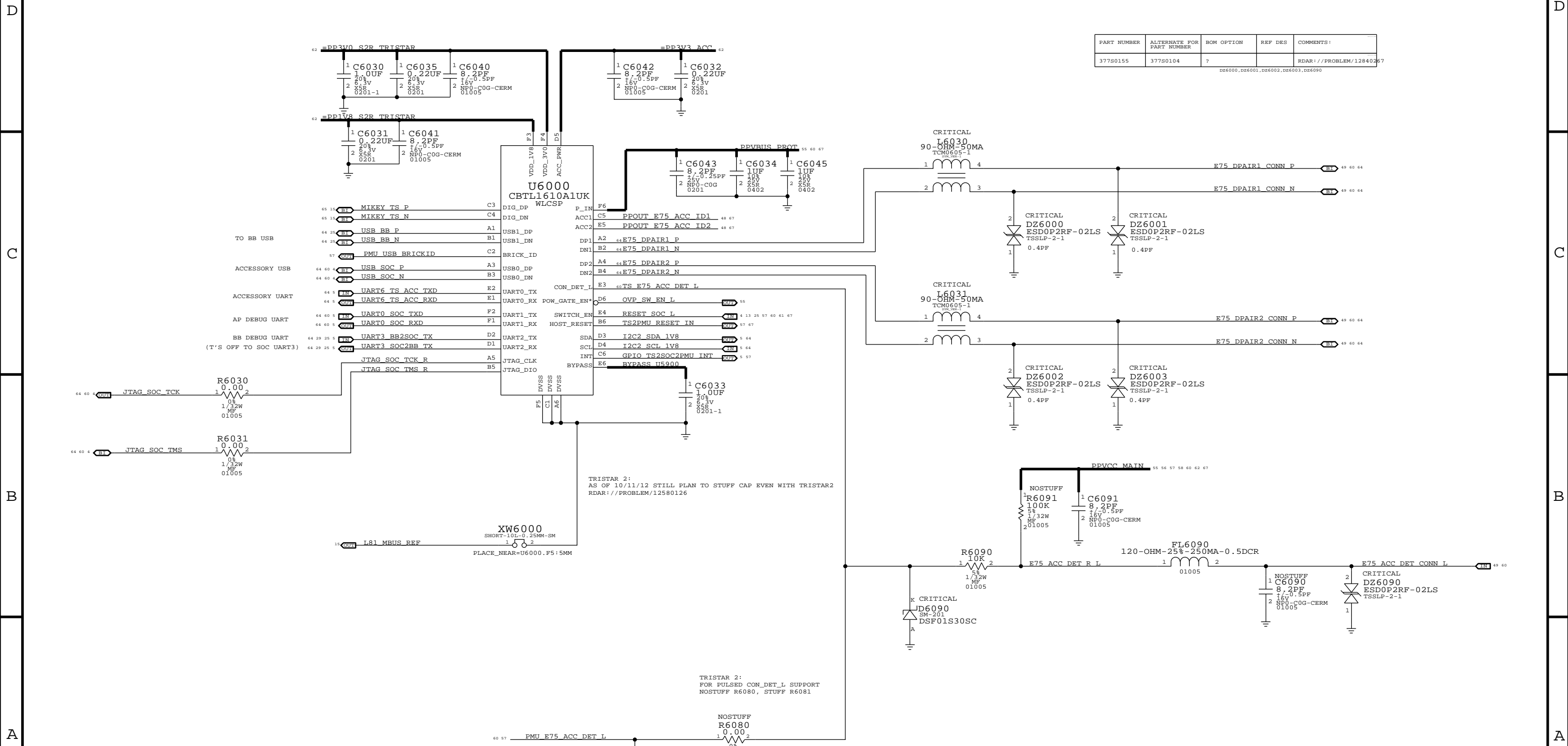
C

B

B

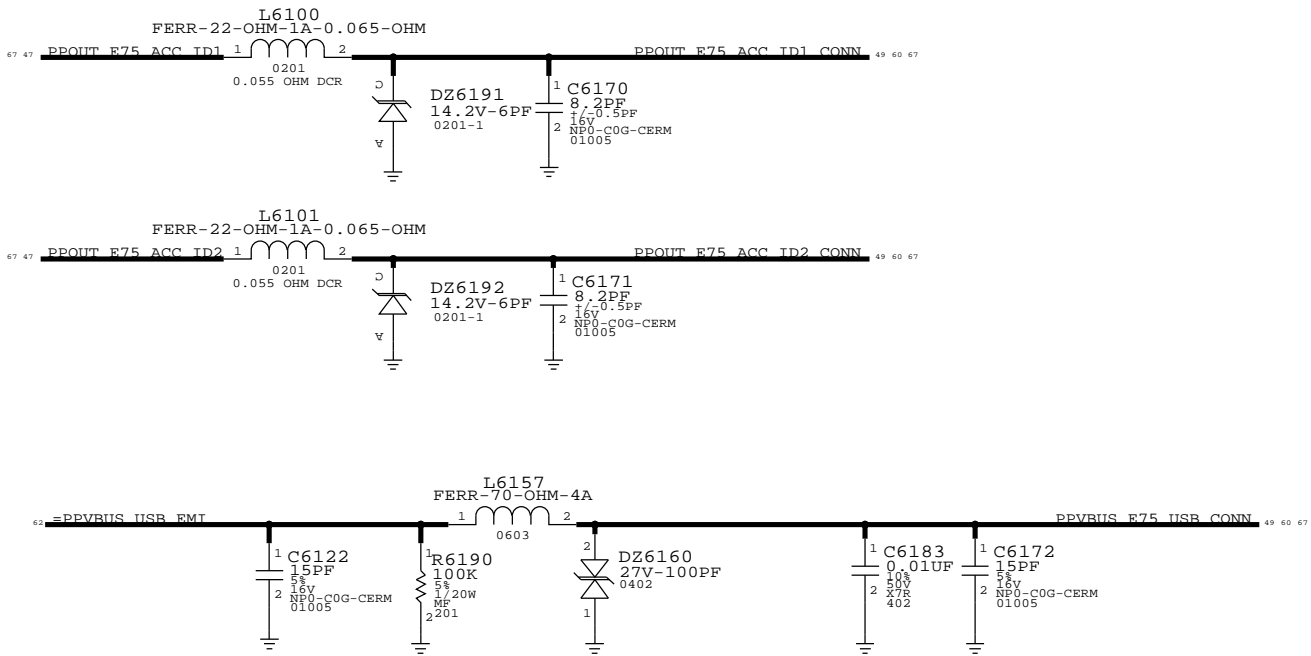
A





DZ6000,DZ6001,DZ6002,DZ6003,DZ6090





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ6160	RDAR:8370432
155S0320	155S0513		L6100,L6101	RDAR:///PROBLEM/9625601
155S0741	155S0397		L6157	RDAR:///PROBLEM/11238851

D

D

C

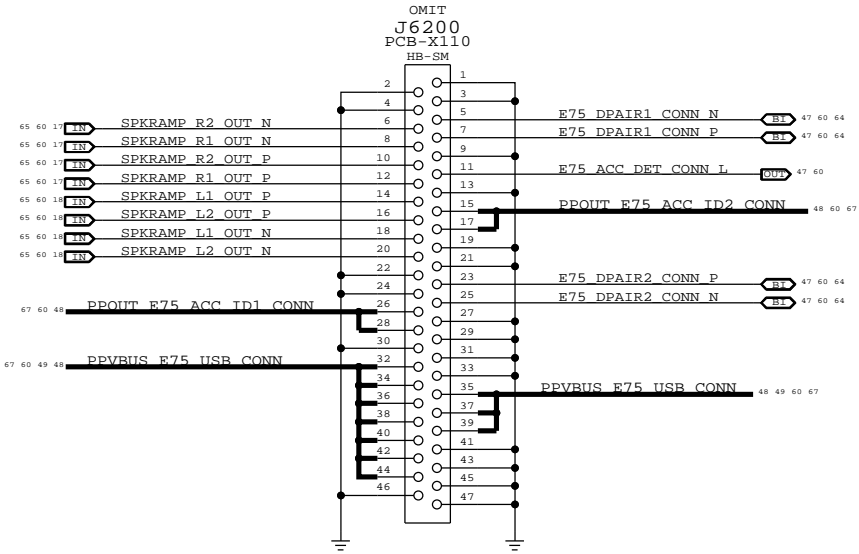
C

B

B

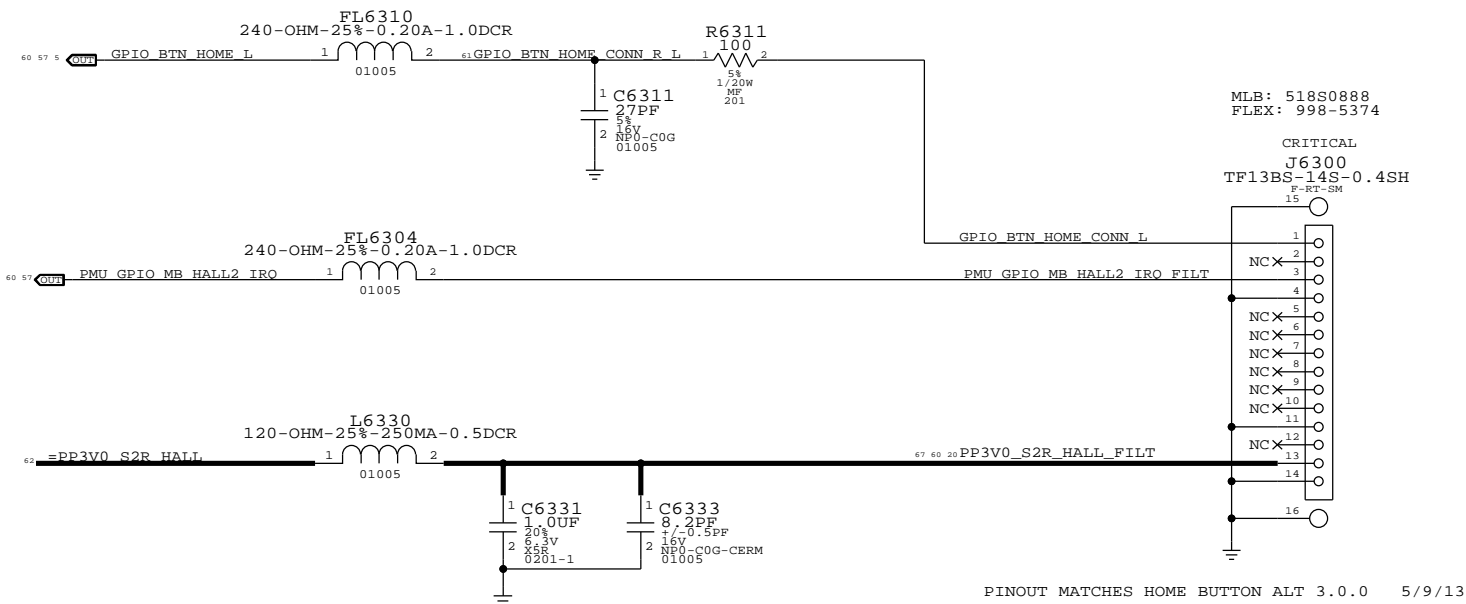
A

IO FLEX HOTBAR PADS  
MLB 998-5877  
FLEX 998-5876

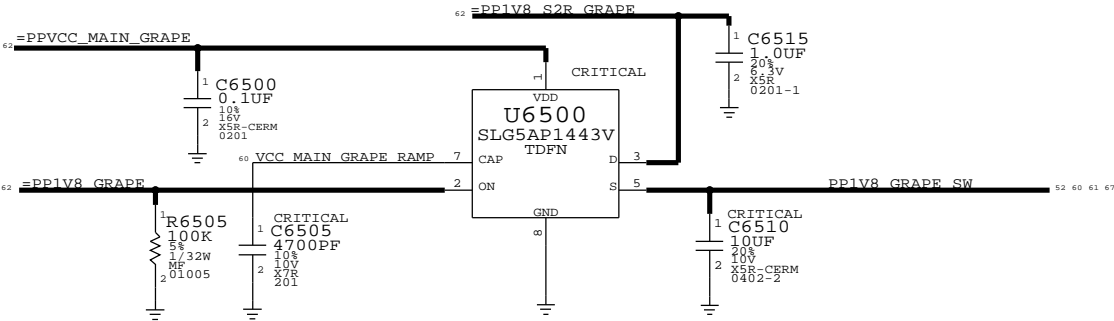


PINOUT MATCHES IO\_FLEX 4.2.0 3/12/13

HOME BUTTON FILTERS

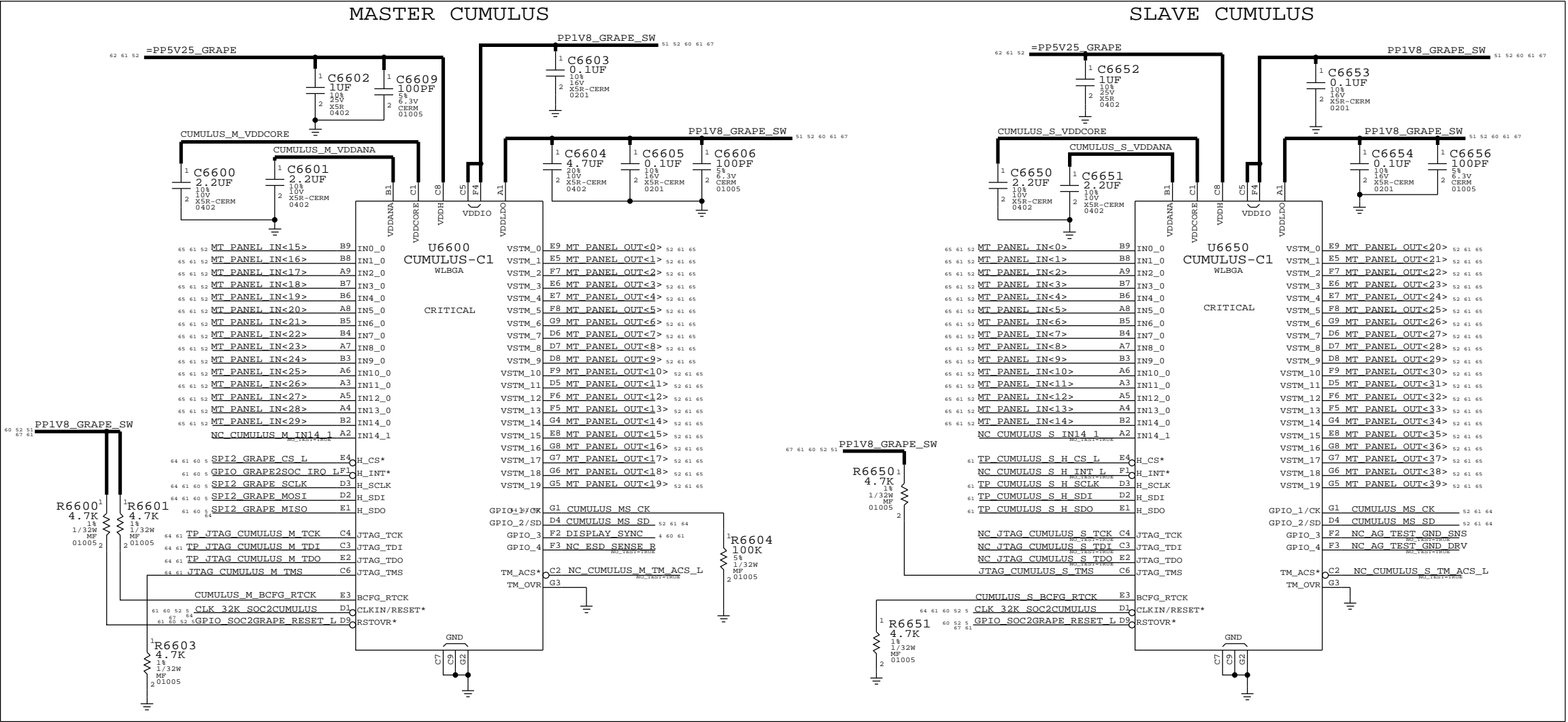


GRAPE CONNECTOR SUPPORT

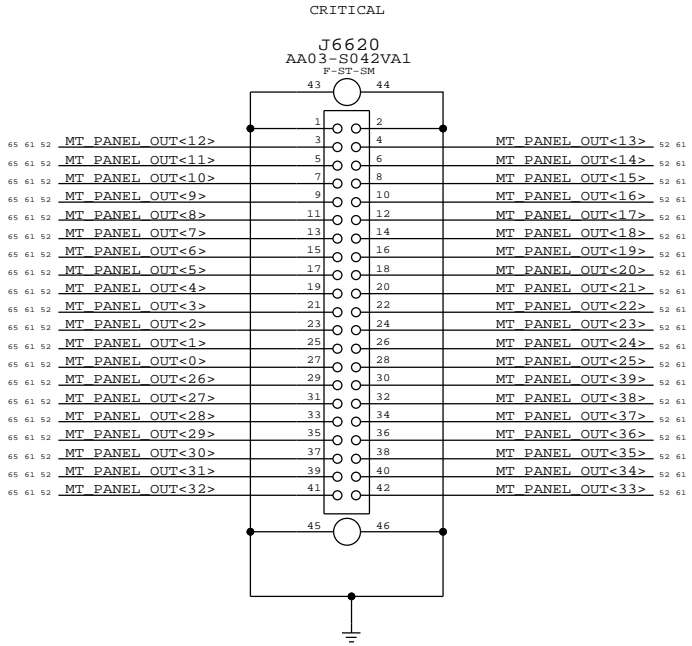


LAYOUT NOTE:  
PUT THERMAL VIAS AROUND U2300 IN CASE OF SHORTED CONDITION

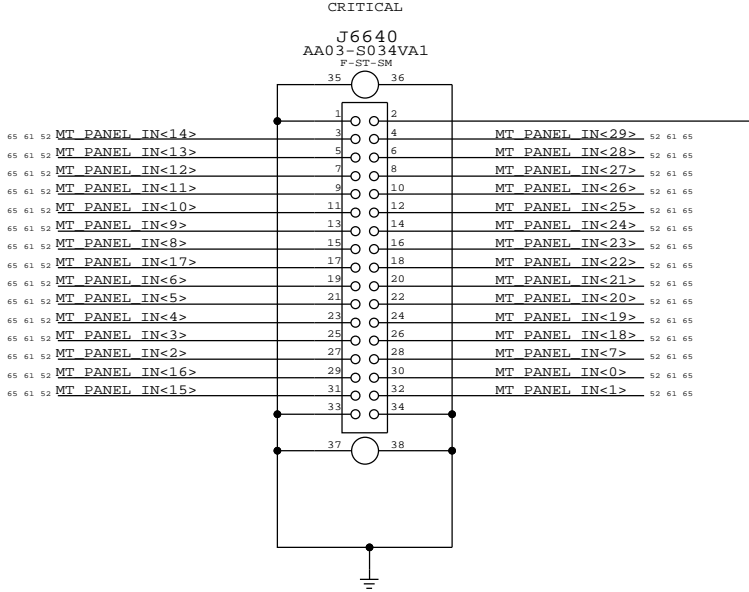
# CUMULUS C1 (CSP) IN MASTER-SLAVE CONFIG



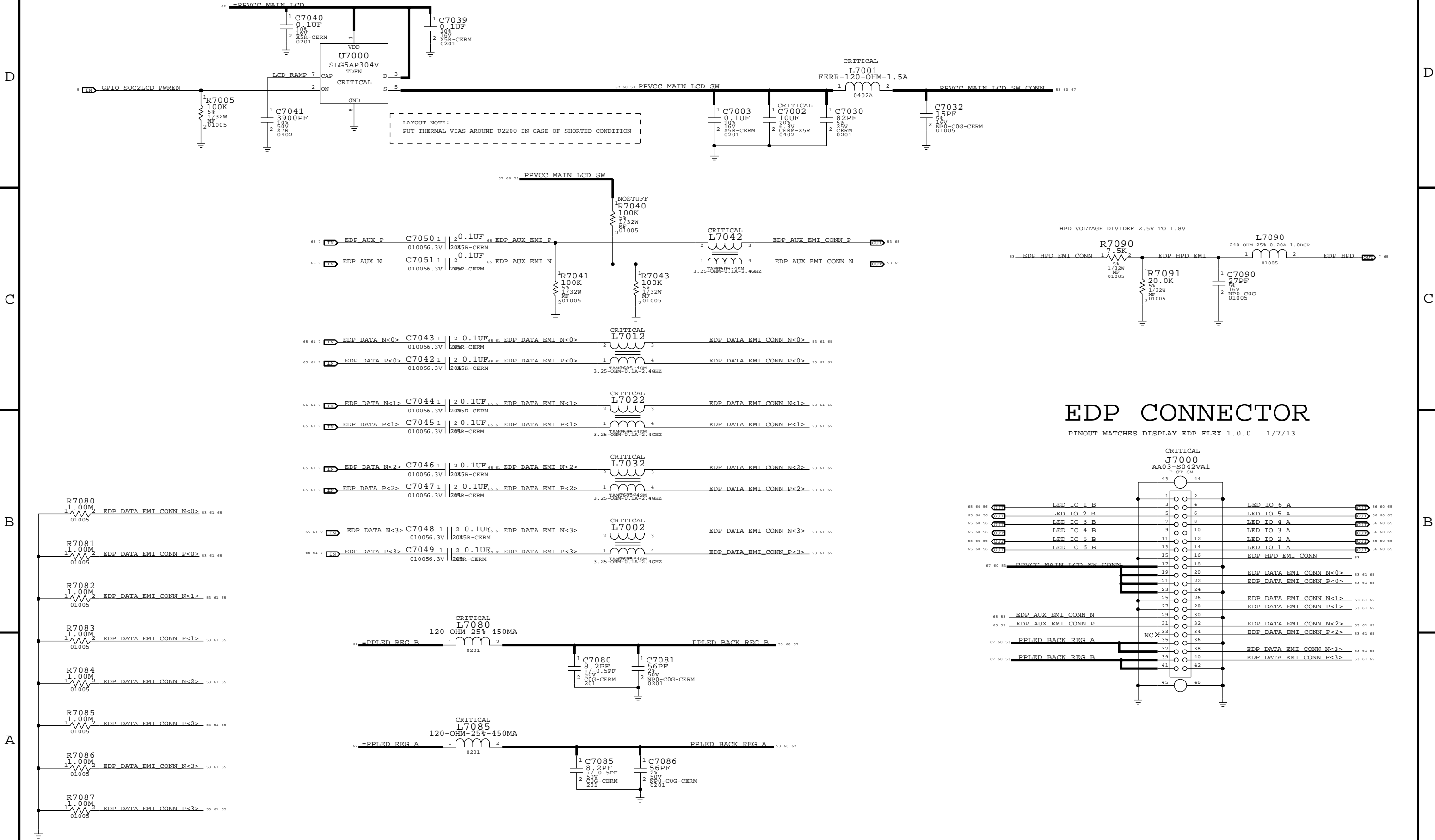
PINOUT MATCHES GRAPE\_FLEX\_DRIVE\_ALT 0.1.0 1/8/1



PINOUT MATCHES GRAPE\_FLEX\_SENSE\_ALT 0.1.0 1/8/1

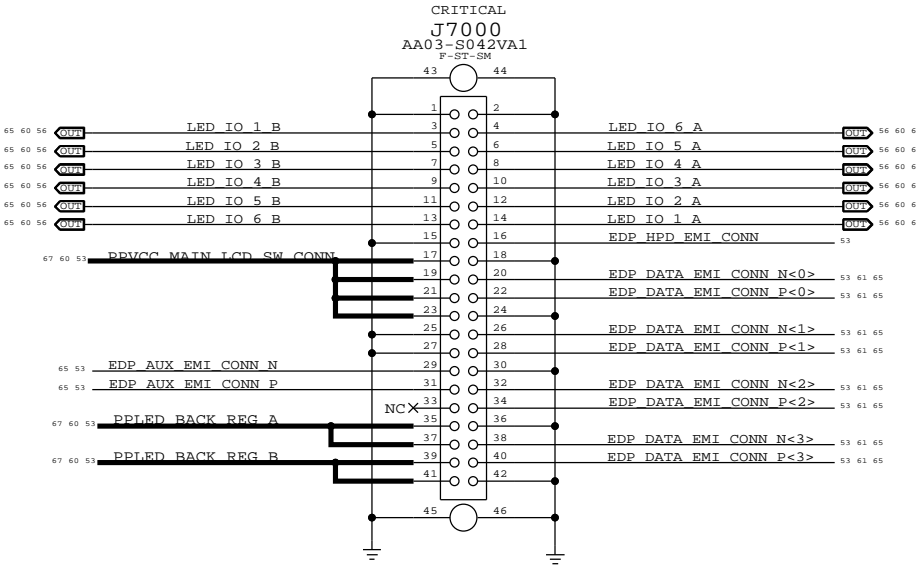


# EDP CONNECTOR SUPPORT



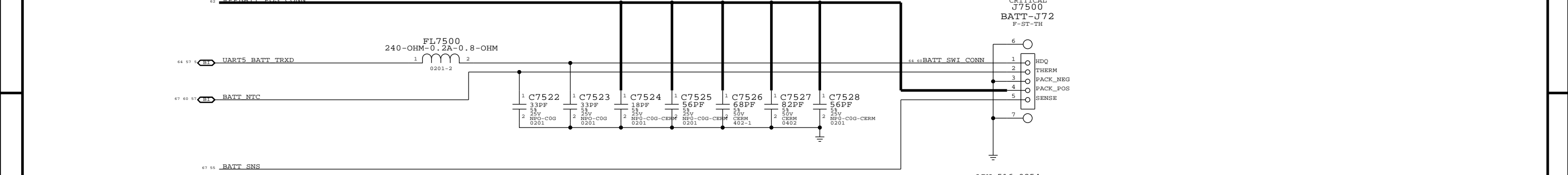
## EDP CONNECTOR

PINOUT MATCHES DISPLAY\_EDP\_FLEX 1.0.0 1/7/13



	PART NUMBER			
155S0644	155S0823	?		RDAR://PROBLEM/11282371

FL7500, L1920



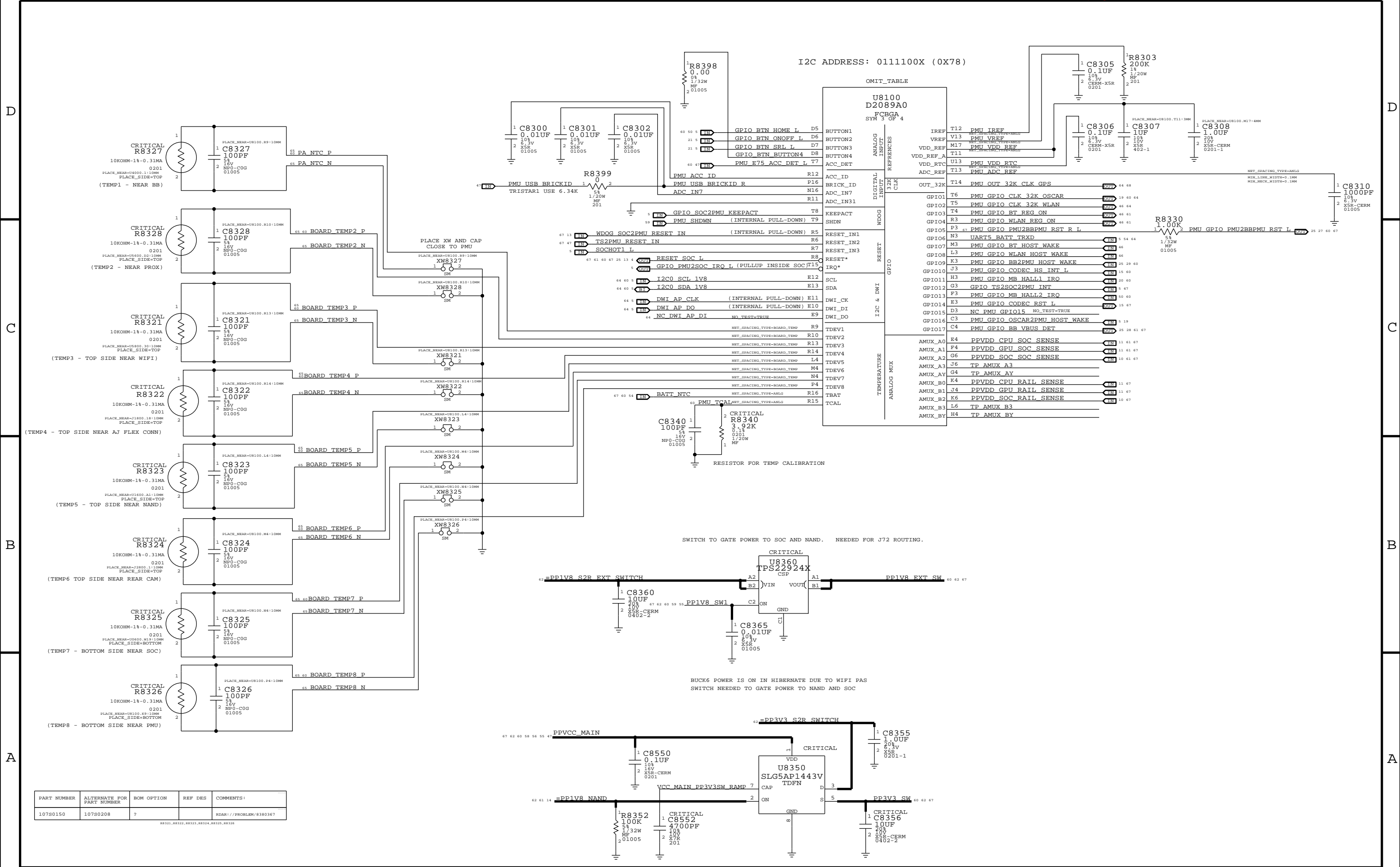
APN: 516-0254

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0339	128S0279	?	C8140,C8141	RDAR://PROBLEM/8967213

C8137 0201 OKAY IF GRAPE HAS EXT FET



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392	?	Y8200	RDAR://PROBLEM/9936684



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	?		RDAR: //PROBLEM/8380367

D

C

B

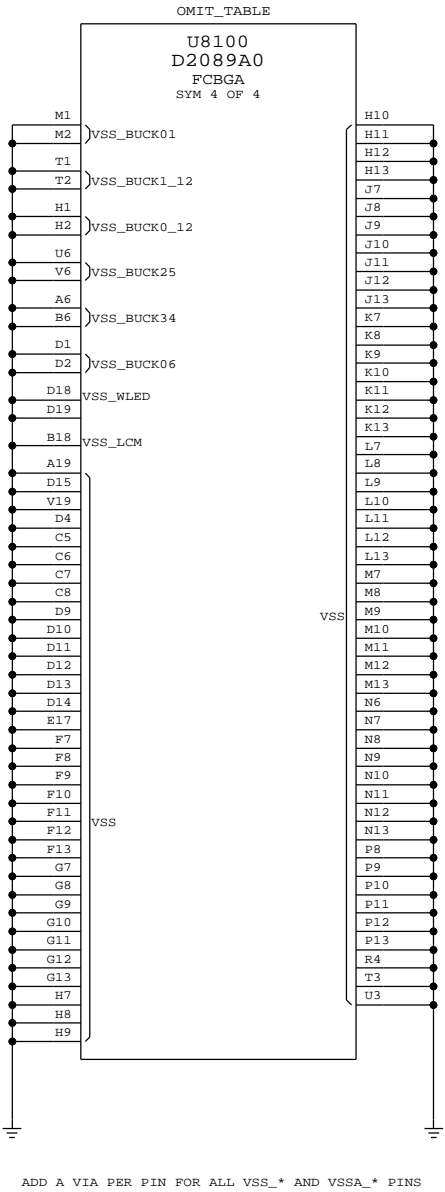
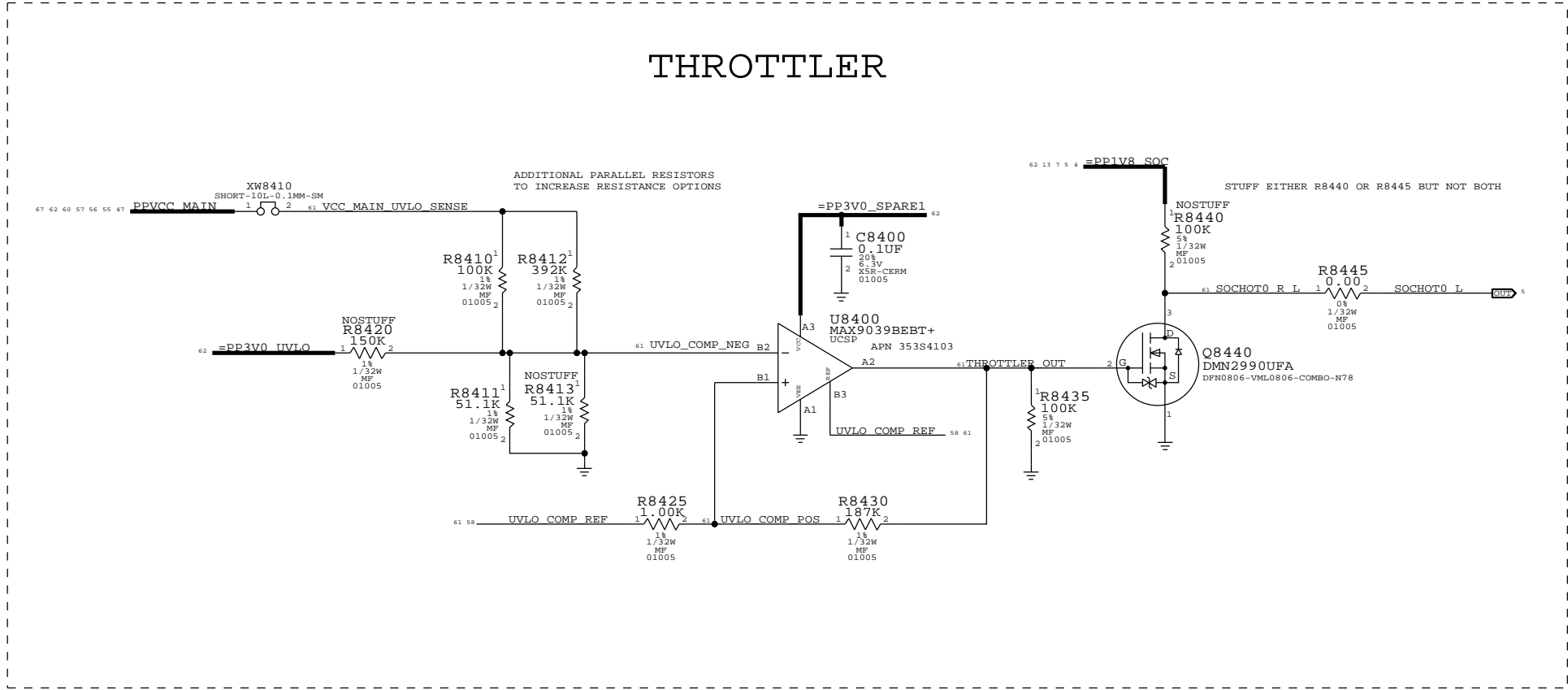
A

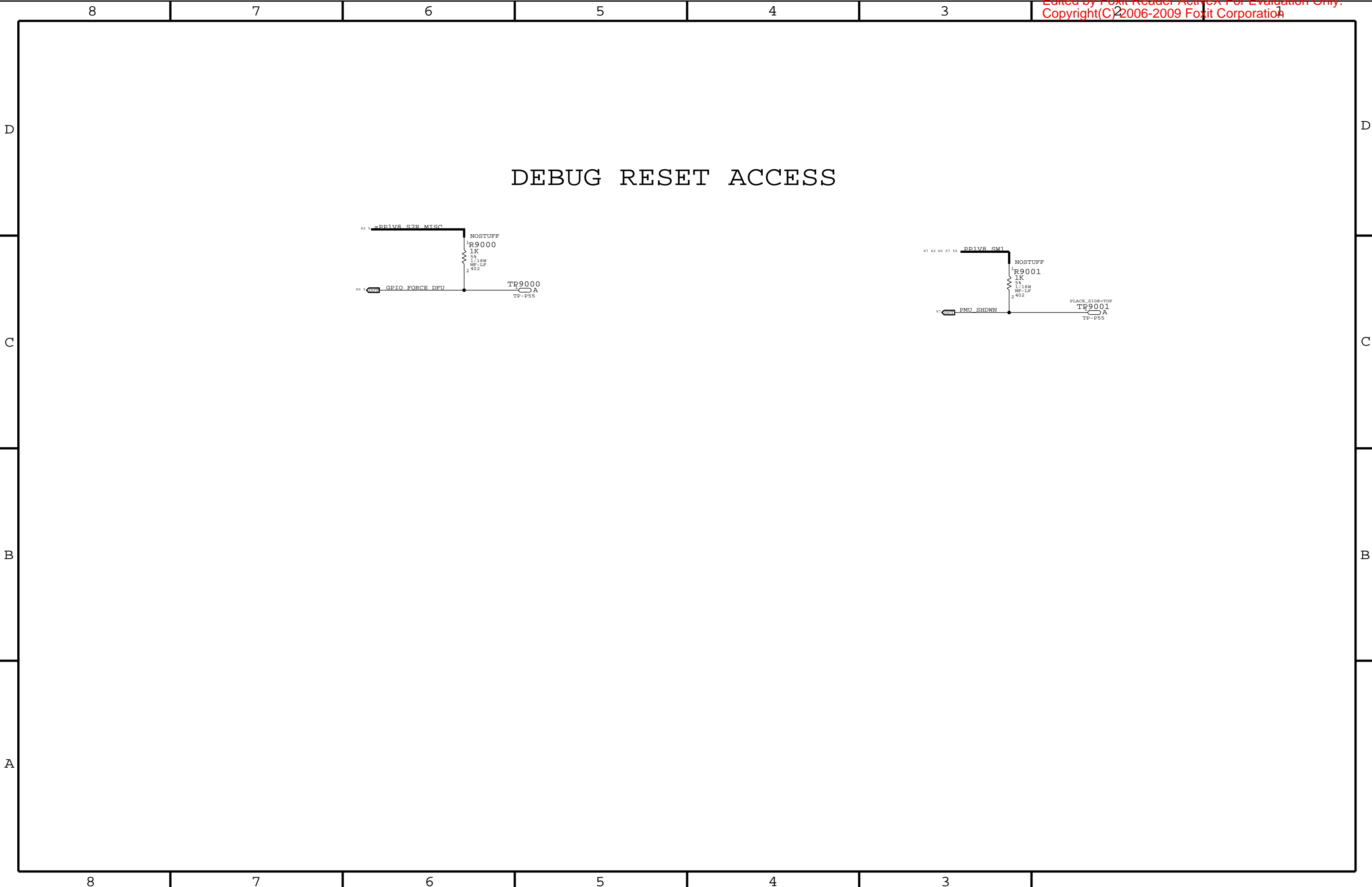
D

C

B

A









EE CHARACTERIZATION TP

FOR FRANK (SEG)

NAND

BOTTOM SIDE	PP9460	1	FMI0 AD<0>	PLACE_NEAR=U0600.A31:2MM	6 14 61 66
	P4MM SM	NO_XNET_CONNECTION=TRUE	NO_XNET_CONNECTION=TRUE		
BOTTOM SIDE	PP9461	1	FMI0 DOS	PLACE_NEAR=U0600.B34:2MM	4 14 61 66
	P4MM SM	NO_XNET_CONNECTION=TRUE	NO_XNET_CONNECTION=TRUE		
			FMI0 AD<0..7>	EE_TEST=TRUE	5 14 61 66
			FMI0 CE0 L	FUNC_TEST=TRUE	4 14 60 66
			FMI0 ALR	FUNC_TEST=TRUE	4 14 66
			FMI0 CLE	FUNC_TEST=TRUE	4 14 66
			FMI0 WE L	FUNC_TEST=TRUE	4 14 66
			FMI0 RE L	FUNC_TEST=TRUE	4 14 66
			FMI0 DOS	FUNC_TEST=TRUE	4 14 61 66
			FMI1 AD<0>	FUNC_TEST=TRUE	4 14 66
			FMI1 CE0 L	FUNC_TEST=TRUE	4 14 66
			FMI1 ALR	FUNC_TEST=TRUE	4 14 66
			FMI1 CLE	FUNC_TEST=TRUE	4 14 66
			FMI1 WE L	FUNC_TEST=TRUE	4 14 66
			FMI1 RE L	FUNC_TEST=TRUE	4 14 66
			FMI1 DOS	FUNC_TEST=TRUE	4 14 66
			PPVREF FMI SOC	FUNC_TEST=TRUE	6 66
			PPVREF FMI NAND	FUNC_TEST=TRUE	14 66
TOP SIDE	PP9440	1	TP FMI TCK NAND	PLACE_SIDE=TOP	14
TOP SIDE	PP9441	1	TP FMI TMS NAND	PLACE_SIDE=TOP	14
TOP SIDE	PP9442	1	=PP1V8 NAND	PLACE_SIDE=TOP	14 57 62
TOP SIDE	PP9443	1	GND	PLACE_SIDE=TOP	
TOP SIDE	PP9450	1	RESET SOC L	EE	4 13 25 47 57 60 67
	P4MM SM				
TOP SIDE	PP9451	1	TP ANALOGMUXOUT		4
	P4MM SM				
TOP SIDE	PP9452	1	SOCHOT0 R L		58
	P4MM SM				
			TP GPIO DFU STATUS	FUNC_TEST=TRUE	5

CAMERA

PP9470	1	MIP11C CAM FRONT CLK P	PLACE_NEAR=U0600.AM35:3MM	7 22 61 65
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9471	1	MIP11C CAM FRONT CLK N	PLACE_NEAR=U0600.AM36:3MM	7 22 61 65
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9472	1	MIP11C CAM FRONT DATA P<0>	PLACE_NEAR=U0600.AM35:3MM	7 22 61 65
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9473	1	MIP11C CAM FRONT DATA N<0>	PLACE_NEAR=U0600.AM36:3MM	7 22 61 65
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9474	1	MIP11C CAM REAR CLK P	PLACE_NEAR=U0600.AR31:3MM	7 23 61 65
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9475	1	MIP11C CAM REAR CLK N	PLACE_NEAR=U0600.AT31:3MM	7 23 61 65
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9476	1	MIP11C CAM REAR DATA P<0>	PLACE_NEAR=U0600.AR33:3MM	7 23 61 65
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9477	1	MIP11C CAM REAR DATA N<0>	PLACE_NEAR=U0600.AT33:3MM	7 23 61 65
P4MM SM	NO_XNET_CONNECTION=TRUE			

HIGH SPEED, NO TEST

		DDR0 CA<0..9>	NO_TEST=TRUE	8 12 61 66
		DDR0 CK P	NO_TEST=TRUE	8 12 61 66
		DDR0 CK N	NO_TEST=TRUE	8 12 61 66
		DDR0 CA<0..9>	NO_TEST=TRUE	8 12 61 66
		DDR0 CKE<0..1>	NO_TEST=TRUE	8 12 61 66
		DDR0 CSN<0..1>	NO_TEST=TRUE	8 12 66
		DDR0 DM<0..3>	NO_TEST=TRUE	8 12 66
		DDR0 DO<0..31>	NO_TEST=TRUE	8 12 61 66
		DDR0 DOS P<0..3>	NO_TEST=TRUE	8 12 61 66
		DDR0 DOS N<0..3>	NO_TEST=TRUE	8 12 61 66
		DDR1 CA<0..9>	NO_TEST=TRUE	8 12 61 66
		DDR1 CK P	NO_TEST=TRUE	8 12 61 66
		DDR1 CK N	NO_TEST=TRUE	8 12 61 66
		DDR1 CA<0..9>	NO_TEST=TRUE	8 12 61 66
		DDR1 CKE<0..1>	NO_TEST=TRUE	8 12 61 66
		DDR1 CSN<0..1>	NO_TEST=TRUE	8 12 66
		DDR1 DM<0..3>	NO_TEST=TRUE	8 12 66
		DDR1 DO<0..31>	NO_TEST=TRUE	8 12 66
		DDR1 DOS P<0..3>	NO_TEST=TRUE	8 12 66
		DDR1 DOS N<0..3>	NO_TEST=TRUE	8 12 66
		MIP11C CAM REAR CLK P	NO_TEST=TRUE	7 23 61 65
		MIP11C CAM REAR CLK N	NO_TEST=TRUE	7 23 61 65
		MIP11C CAM REAR DATA P<0..1>	NO_TEST=TRUE	7 23 61 65
		MIP11C CAM REAR DATA N<0..1>	NO_TEST=TRUE	7 23 61 65
		MIP11C CAM REAR CLK FILT P	NO_TEST=TRUE	23 65
		MIP11C CAM REAR CLK FILT N	NO_TEST=TRUE	23 65
		MIP11C CAM REAR DATA FILT P<0..3>	NO_TEST=TRUE	23 65
		MIP11C CAM REAR DATA FILT N<0..3>	NO_TEST=TRUE	23 65
		MIP11C CAM FRONT CLK P	NO_TEST=TRUE	7 22 61 65
		MIP11C CAM FRONT CLK N	NO_TEST=TRUE	7 22 61 65
		MIP11C CAM FRONT DATA P<0>	NO_TEST=TRUE	7 22 61 65
		MIP11C CAM FRONT DATA N<0>	NO_TEST=TRUE	7 22 61 65
		MIP11C CAM FRONT CLK FILT P	NO_TEST=TRUE	23 65
		MIP11C CAM FRONT CLK FILT N	NO_TEST=TRUE	23 65
		MIP11C CAM FRONT DATA FILT P<0>	NO_TEST=TRUE	23 65
		MIP11C CAM FRONT DATA FILT N<0>	NO_TEST=TRUE	23 65
		EDP DATA P<0..3>	NO_TEST=TRUE	7 53 65
		EDP DATA N<0..3>	NO_TEST=TRUE	7 53 65
		EDP DATA EMI P<0..3>	NO_TEST=TRUE	53 65
		EDP DATA EMI N<0..3>	NO_TEST=TRUE	53 65
		EDP DATA EMI CONN P<0..3>	NO_TEST=TRUE	53 65
		EDP DATA EMI CONN N<0..3>	NO_TEST=TRUE	53 65

DRAM

NEAR DRAM

PP9410	1	DDR0 CK N	PLACE_NEAR=U1400.AF14:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9411	1	DDR0 CK P	PLACE_NEAR=U1400.AF15:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9412	1	DDR0 CKE<0>	PLACE_NEAR=U1400.AF16:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9413	1	DDR0 DOS N<3>	PLACE_NEAR=U1400.AE17:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9414	1	DDR0 CA<0>	PLACE_NEAR=U1400.AE21:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9415	1	DDR0 DO<2>	PLACE_NEAR=U1400.B18:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9416	1	DDR0 DO<3>	PLACE_NEAR=U1400.C8:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9417	1	DDR0 DOS P<3>	PLACE_NEAR=U1400.B8:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9418	1	DDR0 DOS N<0>	PLACE_NEAR=U1400.C15:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9419	1	DDR0 DOS P<0>	PLACE_NEAR=U1400.B15:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			

PP9420	1	DDR1 CK N	PLACE_NEAR=U1400.T26:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9421	1	DDR1 CK P	PLACE_NEAR=U1400.R26:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9422	1	DDR1 CKE<0>	PLACE_NEAR=U1400.P26:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9423	1	DDR1 CKE<1>	PLACE_NEAR=U1400.N25:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9424	1	DDR1 CA<0>	PLACE_NEAR=U1400.J25:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9425	1	DDR1 CA<1>	PLACE_NEAR=U1400.K26:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9426	1	DDR1 CA<2>	PLACE_NEAR=U1400.K25:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9427	1	DDR1 CA<3>	PLACE_NEAR=U1400.L25:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9428	1	DDR1 CSN<0>	PLACE_NEAR=U1400.N35:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			

NEAR SOC

PP9435	1	DDR0 DO<28>	PLACE_NEAR=U0600.D5:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9436	1	DDR0 DOS N<3>	PLACE_NEAR=U0600.A6:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			
PP9437	1	DDR0 DOS P<3>	PLACE_NEAR=U0600.A5:1MM	8 12 61 66
P4MM SM	NO_XNET_CONNECTION=TRUE			

POWER, NO TEST

		PP6V0 LCM HI	NO_TEST=TRUE	56 67
		SW CHGA	NO_TEST=TRUE	56 67
		WLED LX A	NO_TEST=TRUE	56 67
		WLED LX B	NO_TEST=TRUE	56 67
		L81 PVCP	NO_TEST=TRUE	15 65
		L81 NVCP	NO_TEST=TRUE	15 65
		CHARGE PUMP OUTPUTS		
		L81 FLYC	NO_TEST=TRUE	15 65
		L81 FLYN	NO_TEST=TRUE	15 65
		L81 FLYP	NO_TEST=TRUE	15 65
		THROTTLER OUT	NO_TEST=TRUE	58
		UVLO COMP NEG	NO_TEST=TRUE	58
		UVLO COMP POS	NO_TEST=TRUE	58
		UVLO COMP REF	NO_TEST=TRUE	58
		VCC MAIN UVLO SENSE	NO_TEST=TRUE	58

GRAPE

CONVERT TO PROBE POINTS IF NOT ABLE TO PLACE TESTPOINT

		TP JTAG CUMULUS M TCK	52 64
		TP JTAG CUMULUS M TDI	52 64
		TP JTAG CUMULUS M TMS	52 64
		TP JTAG CUMULUS M TDO	52 64
		DISPLAY SYNC	4 52 60
		CUMULUS MS CK	52 64
		CUMULUS MS SD	52 64
		GPIO GRAPE2SOC I/O L	5 52 60
		GPIO SOC2GRAPE RESET L	5 52 60 67
		CLK 32K SOC2CUMULUS	5 52 60 64
		SPI2 GRAPE MOSI	5 52 60 64
		SPI2 GRAPE MISO	5 52 60 64
		SPI2 GRAPE SCLK	5 52 60 64
		SPI2 GRAPE CS L	5 52 60 64
		TP CUMULUS S H CS L	52
		TP CUMULUS S H SCLK	52
		TP CUMULUS S H SDI	52
		TP CUMULUS S H SDO	52
		=PP5V25 GRAPE	52 62
		PP1V8 GRAPE SW	51 52 60 67

AUDIO

		L81 DMIC1 FF SD	FUNC_TEST=TRUE	15
--	--	-----------------	----------------	----

NO TEST DUE TO LAYOUT

		I2C3 TP AT ALS FILTER SIDE		
		I2C3 SCL 1V8	NO_TEST=TRUE	5 13 22 64
		I2C3 SDA 1V8	NO_TEST=TRUE	5 13 22 64
		MAX98304 L1 IN N	NO_TEST=TRUE	18 65
		MAX98304 L1 IN P	NO_TEST=TRUE	18 65
		MAX98304 R1 IN N	NO_TEST=TRUE	17 65
		MAX98304 R1 IN P	NO_TEST=TRUE	17 65
		MAX98304 L2 IN N	NO_TEST=TRUE	18 65
		MAX98304 L2 IN P	NO_TEST=TRUE	18 65
		MAX98304 R2 IN N	NO_TEST=TRUE	17 65
		MAX98304 R2 IN P	NO_TEST=TRUE	17 65
		GPIO BTN HOME CONN R L	NO_TEST=TRUE	50

NO TEST ON PROX

		PROX AD7149 CIN5	NO_TEST=TRUE	45
		PROX AD7149 CIN7	NO_TEST=TRUE	45
		PROX AD7149 CIN9	NO_TEST=TRUE	45
		PROX AD7149 CIN7 FILT	NO_TEST=TRUE	45
		PROX AD7149 CIN9 FILT	NO_TEST=TRUE	45
		PROX AD7149 CIN7 CONN	NO_TEST=TRUE	45
		PROX AD7149 CIN9 CONN	NO_TEST=TRUE	45
		PROX AD7149 ACSHIELD CONN	NO_TEST=TRUE	45
		PROX AD7149 BIAS	NO_TEST=TRUE	45
		ACSHIELD SB	NO_TEST=TRUE	45
		ACSH SB	NO_TEST=TRUE	45
		PROX AD7149 GPIO	NO_TEST=TRUE	45

WIFI

		JTAG WLAN TMS TX BLANK	FUNC_TEST=TRUE	46 64
		TP JTAG WLAN TCK	FUNC_TEST=TRUE	46 64
		JTAG WLAN TDI OSCAR A	FUNC_TEST=TRUE	46 64
		JTAG WLAN TDO OSCAR B	FUNC_TEST=TRUE	46 64
		TP JTAG WLAN TRST L	FUNC_TEST=TRUE	46 64
		JTAG WLAN SEL	FUNC_TEST=TRUE	46 64
		UART2 SOC2WLAN TX R	FUNC_TEST=TRUE	46 64
		UART2 WLAN2SOC TX R	FUNC_TEST=TRUE	46 64
		UART BB2WLAN LTE COEX R	FUNC_TEST=TRUE	46 64
		UART WLAN2BB LTE COEX R	FUNC_TEST=TRUE	46 64
		=PP3V3 S2R WIFI PA	FUNC_TEST=TRUE	46 62
		HSIC1 SOC2WLAN HOST RDY R	FUNC_TEST=TRUE	46 64
		HSIC1 WLAN2SOC DEVICE RDY	FUNC_TEST=TRUE	5 46 64
		HSIC1 WLAN2SOC REMOTE WAKE	FUNC_TEST=TRUE	5 46 64

FOR HSIC CHARACTERIZATION

PP9480	1	HSIC1 WLAN DATA	PLACE_NEAR=U0600.A27:3MM	4 46 61 64
P4MM SM				
PP9481	1	HSIC1 WLAN STB	PLACE_NEAR=U0600.B27:3MM	4 46 61 64
P4MM SM				
PP9482	1	HSIC1 WLAN DATA	PLACE_NEAR=U5800.13:3MM	4 46 61 64
P4MM SM				
PP9483	1	HSIC1 WLAN STB	PLACE_NEAR=U5800.14:3MM	4 46 61 64
P4MM SM				
		PMU GPIO WLAN REG ON	FUNC_TEST=TRUE	46 57
		PMU GPIO BT REG ON	FUNC_TEST=TRUE	46 57
		GPIO BT WAKE	FUNC_TEST=TRUE	5 46

BASEBAND

		BB JTAG TMS	FUNC_TEST=TRUE	5 25 28 64
		BB JTAG TCK	FUNC_TEST=TRUE	5 25 28 64
		BB JTAG TDI	FUNC_TEST=TRUE	5 25 28 64
		BB JTAG TDO	FUNC_TEST=TRUE	5 25 28 64
		BB JTAG TRST L	FUNC_TEST=TRUE	5 25 28 64
		USB BB DEBUG P	FUNC_TEST=TRUE	25 28 64
		USB BB DEBUG N	FUNC_TEST=TRUE	25 28 64
		DEBUG RST L	FUNC_TEST=TRUE	25 28 67
		PMU GPIO BB VBUS DET	FUNC_TEST=TRUE	25 28 57 67

FOR HSIC CHARACTERIZATION

PP9485	1	HSIC2 BB DATA	PLACE_NEAR=U0600.AJ35:3MM	4 25 28 61 64
P4MM SM				
PP9486	1	HSIC2 BB STB	PLACE_NEAR=U0600.AJ36:3MM	4 25 28 61 64
P4MM SM				
PP9487	1	HSIC2 BB DATA	PLACE_NEAR=U3400.C7:3MM	4 25 28 61 64
P4MM SM				
PP9488	1	HSIC2 BB STB	PLACE_NEAR=U3400.B8:3MM	4 25 28 61 64
P4MM SM				

POWER CONNECTIONS

D

D

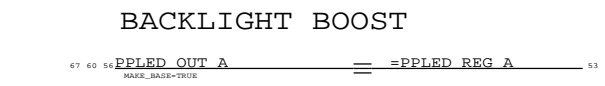
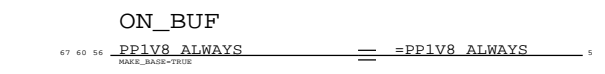
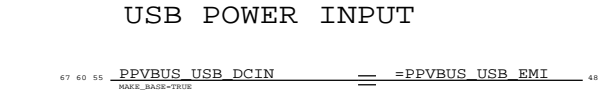
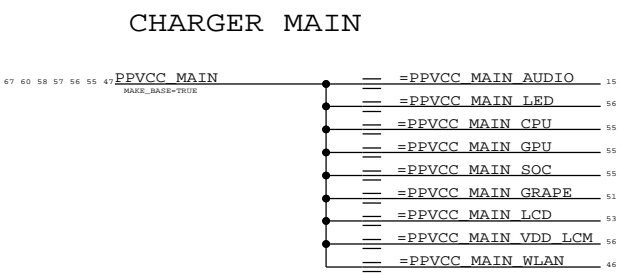
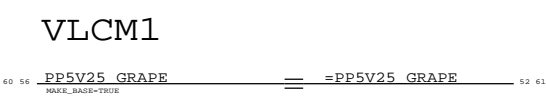
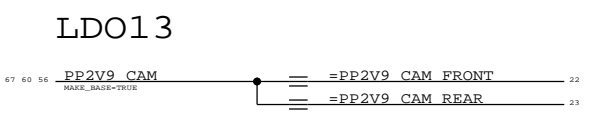
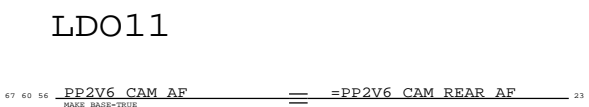
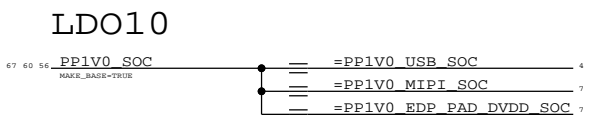
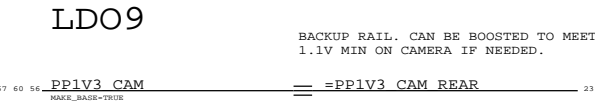
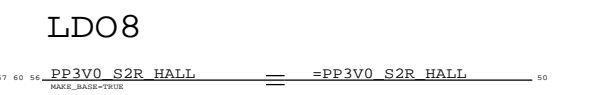
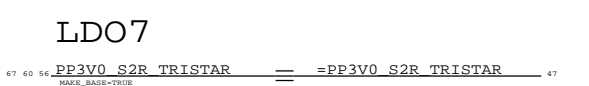
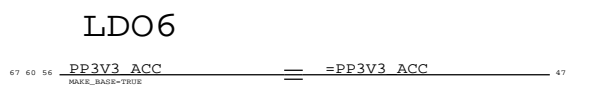
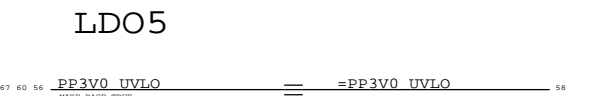
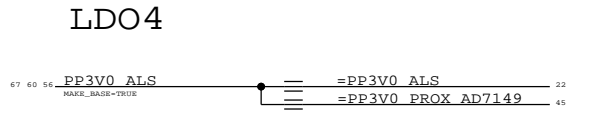
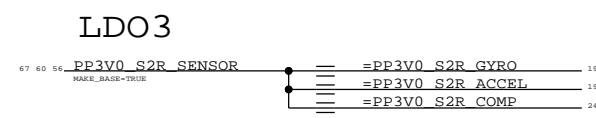
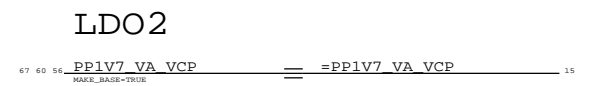
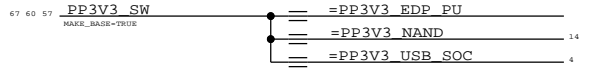
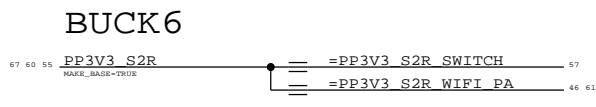
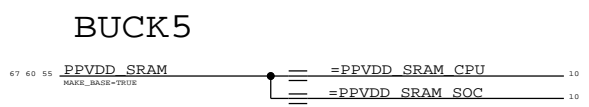
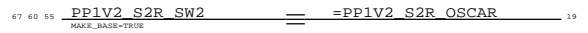
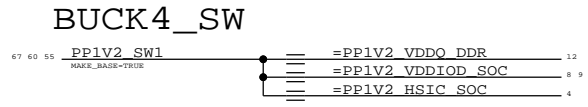
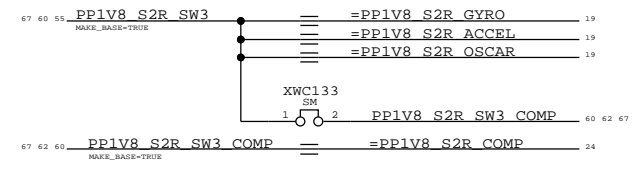
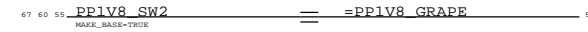
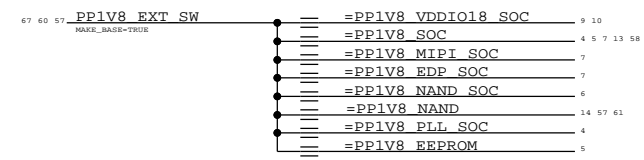
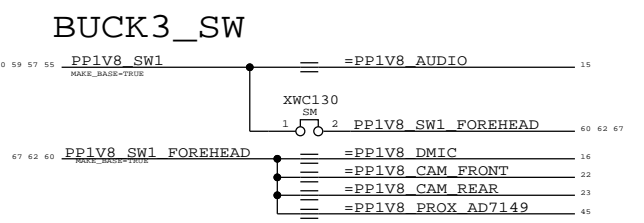
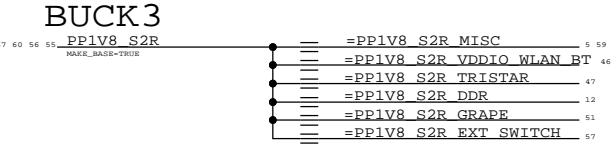
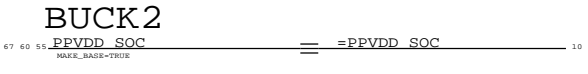
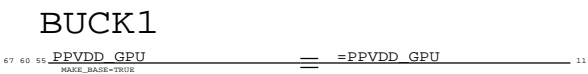
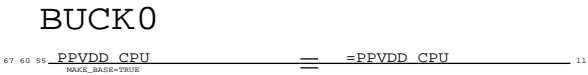
C

C

B

B

A



Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_50S	*	45_OHM_SE	CLK	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
U000		CLK_50S	CLK	CLK 32K SOC2CUMULUS 5 52 60 61
U001		CLK_50S	CLK	CLK 32K SOC2CUMULUS FILT 60
U002		CLK_50S	CLK	CUMULUS MS CK 52 61
U003		CLK_50S	CLK	CUMULUS MS SD 52 61
U004		CLK_50S	CLK	PMU GPIO CLK 32K WLAN 46 57
U005		CLK_50S	CLK	PMU GPIO CLK 32K OSCAR 19 57 60
U006		CLK_50S	CLK	PMU OUT 32K CLK GPS 57 68
U007		CLK_50S	CLK	ISP1 CAM FRONT CLK R 7
U008		CLK_50S	CLK	ISP1 CAM FRONT CLK 7 22
U009		CLK_50S	CLK	ISP1 CAM FRONT CLK F 22 60
U010		CLK_50S	CLK	ISP0 CAM REAR CLK R 7
U011		CLK_50S	CLK	ISP0 CAM REAR CLK 7 23
U012		CLK_50S	CLK	ISP0 CAM REAR CLK F 23 60

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART_50S	*	45_OHM_SE	UART	*	*	3:1_SPACING
			UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
U000		UART_50S	UART	UART0 SOC RXD 5 47 60
U001		UART_50S	UART	UART0 SOC TXD 5 47 60
U002		UART_50S	UART	UART3 SOC2BB RTS L 5 25 29
U003		UART_50S	UART	UART3 BB2SOC RTS L 5 25 29
U004		UART_50S	UART	UART3 SOC2BB TX 5 25 29 47
U005		UART_50S	UART	UART3 BB2SOC TX 5 25 29 47
U006		UART_50S	UART	UART4 OSCAR2SOC RXD 5 19
U007		UART_50S	UART	UART4 SOC2OSCAR TXD 5 19
U008		UART_50S	UART	UART1 SOC2BT RTS L 5 46
U009		UART_50S	UART	UART1 BT2SOC RTS L 5 46
U010		UART_50S	UART	UART1 SOC2BT TX 5 46
U011		UART_50S	UART	UART1 BT2SOC TX 5 46
U012		UART_50S	UART	UART2 SOC2WLAN TX 5 46
U013		UART_50S	UART	UART2 WLAN2SOC TX 5 46
U014		UART_50S	UART	UART2 SOC2WLAN TX R 46 61
U015		UART_50S	UART	UART2 WLAN2SOC TX R 46 61
U016		UART_50S	UART	UART6 TS ACC RXD 5 47
U017		UART_50S	UART	UART6 TS ACC TXD 5 47
U018			UART	UART5 BATT TRXD 5 54 57
U019			UART	BATT SWI CONN 54 60

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S_50S	*	45_OHM_SE	I2S	*	*	3:1_SPACING
			I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
U000		I2S_50S	CLK	I2S0 CODEC ASP MCK R 5 15
U001		I2S_50S	CLK	I2S0 CODEC ASP MCK 5
U002		I2S_50S	I2S	I2S0 CODEC ASP BCLK 5 15
U003		I2S_50S	I2S	I2S0 CODEC ASP LRCK 5 15
U004		I2S_50S	I2S	I2S0 CODEC ASP DIN 5 15
U005		I2S_50S	I2S	I2S0 CODEC ASP DOUT 5 15
U006		I2S_50S	I2S	I2S0 CODEC ASP SDOUT 15
U007		I2S_50S	I2S	NC I2S1 MCK 5
U008		I2S_50S	I2S	I2S1 CODEC XSP BCLK 5 15
U009		I2S_50S	I2S	I2S1 CODEC XSP LRCK 5 15
U010		I2S_50S	I2S	I2S1 CODEC XSP DIN 5 15
U011		I2S_50S	I2S	I2S1 CODEC XSP DOUT 5 15
U012		I2S_50S	I2S	I2S1 CODEC XSP SDOUT 15
U013		I2S_50S	CLK	NC I2S2 MCK R 5
U014		I2S_50S	CLK	NC I2S2 MCK 5
U015		I2S_50S	I2S	NC I2S2 BCLK 5
U016		I2S_50S	I2S	NC I2S2 LRCK 5
U017		I2S_50S	I2S	NC I2S2 DIN 5
U018		I2S_50S	I2S	NC I2S2 DOUT 5
U019		I2S_50S	I2S	NC I2S4 MCK 5
U020		I2S_50S	I2S	I2S4 SOC2BT BCLK 5 46
U021		I2S_50S	I2S	I2S4 SOC2BT LRCK 5 46
U022		I2S_50S	I2S	I2S4 SOC2BT DATA 5 46
U023		I2S_50S	I2S	I2S4 BT2SOC DATA 5 46

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
U000			DWI	DWI AP CLK 5 57
U001			DWI	NC DWI AP DI 57
U002			DWI	DWI AP DO 5 57

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
U000		I2C_50S	I2C	I2C0 SDA 1V8 5 57 60
U001		I2C_50S	I2C	I2C0 SCL 1V8 5 57 60
U002		I2C_50S	I2C	I2C3 CAM ALS SDA 1V8 F 22 60
U003		I2C_50S	I2C	I2C3 CAM ALS SCL 1V8 F 22 60
U004		I2C_50S	I2C	I2C0 HP ALS SDA 1V8 FILT 60
U005		I2C_50S	I2C	I2C0 HP ALS SCL 1V8 FILT 60
U006		I2C_50S	I2C	I2C1 SOC2OSCAR SWDCLK 1V8 5 19
U007		I2C_50S	I2C	I2C1 SOC2OSCAR SWDIO 1V8 5 19
U008		I2C_50S	I2C	I2C2 SDA 1V8 5 47
U009		I2C_50S	I2C	I2C2 SCL 1V8 5 47
U010		I2C_50S	I2C	I2C3 SDA 1V8 5 13 22 61
U011		I2C_50S	I2C	I2C3 SCL 1V8 5 13 22 61
U012		I2C_50S	I2C	DMIC1 FF SD FILT 16 60
U013		I2C_50S	I2C	DMIC1 FF SCLK FILT 16 60
U014		I2C_50S	I2C	DMIC1 FF SD 15 16
U015		I2C_50S	I2C	DMIC1 FF SCLK 15 16
U016		I2C_50S	I2C	SEP I2C0 SCL 5
U017		I2C_50S	I2C	SEP I2C0 SDA 5
U018		I2C_50S	I2C	ISP0 CAM REAR SCL 7 23
U019		I2C_50S	I2C	ISP0 CAM REAR SDA 7 23
U020		I2C_50S	I2C	ISP0 CAM REAR SCL F 23 60
U021		I2C_50S	I2C	ISP0 CAM REAR SDA F 23 60
U022		I2C_50S	I2C	ISP1 CAM FRONT SCL 7 22
U023		I2C_50S	I2C	ISP1 CAM FRONT SDA 7 22
U024		I2C_50S	I2C	ISP1 CAM FRONT SCL F 22 60
U025		I2C_50S	I2C	ISP1 CAM FRONT SDA F 22 60

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
U000		SPI_50S	SPI	SPI3 CODEC MISO 5 15
U001		SPI_50S	SPI	SPI3 CODEC MOSI 5 15
U002		SPI_50S	SPI	SPI3 CODEC SCLK 5 15
U003		SPI_50S	SPI	SPI3 CODEC CS L 5 15
U004		SPI_50S	SPI	SPI2 GRAPE MISO 5 52 60 61 64
U005		SPI_50S	SPI	SPI2 GRAPE MOSI 5 52 60 61 64
U006		SPI_50S	SPI	SPI2 GRAPE SCLK 5 52 60 61 64
U007		SPI_50S	SPI	SPI2 GRAPE CS L 5 52 60 61 64
U008		SPI_50S	SPI	SPI2 GRAPE MISO 5 52 60 61 64
U009		SPI_50S	SPI	SPI2 GRAPE MOSI 5 52 60 61 64
U010		SPI_50S	SPI	SPI2 GRAPE SCLK 5 52 60 61 64
U011		SPI_50S	SPI	SPI2 GRAPE CS L 5 52 60 61 64
U012		SPI_50S	SPI	SPI OSCAR MISO 19 24
U013		SPI_50S	SPI	SPI OSCAR MOSI 19 24
U014		SPI_50S	SPI	SPI OSCAR SCLK 19 24
U015		SPI_50S	SPI	SPI OSCAR MISO GYRO 19
U016		SPI_50S	SPI	SPI OSCAR MISO ACCEL 19
U017		SPI_50S	SPI	SPI OSCAR MISO COMPI 24
U018		SPI_50S	SPI	SPI OSCAR MOSI R 19
U019		SPI_50S	SPI	SPI OSCAR SCLK R 19
U020		SPI_50S	SPI	SPI OSCAR2ACCEL CS L 19
U021		SPI_50S	SPI	SPI OSCAR2GYRO CS L 19
U022		SPI_50S	SPI	SPI OSCAR2COMPASS CS L 19 24

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
U000			JTAG	JTAG SOC TCK 4 47 60
U001			JTAG	JTAG SOC TMS 4 47 60
U002			JTAG	JTAG SOC TDI 4 60
U003			JTAG	TP JTAG SOC TDO 4 60
U004			RST	JTAG SOC TRST L 4 13 60
U005			JTAG	NC JTAG SOC TRTCK 4
U006			JTAG	BB JTAG TMS 5 25 28 61
U007			JTAG	BB JTAG TCK 5 25 28 61
U008			JTAG	BB JTAG TDO 5 25 28 61
U009			JTAG	BB JTAG TDI 5 25 28 61
U010			RST	BB JTAG TRST L 5 25 28 61
U011			JTAG	JTAG WLAN TMS TX BLANK 46 61
U012			JTAG	TP JTAG WLAN TCK 46 61
U013			JTAG	JTAG WLAN TDO OSCAR B 46 61
U014			JTAG	JTAG WLAN TDI OSCAR A 46 61
U015			RST	TP JTAG WLAN TRST L 46 61
U016			JTAG	TP JTAG CUMULUS M TCK 52 61
U017			JTAG	TP JTAG CUMULUS M TDI 52 61
U018			JTAG	JTAG CUMULUS M TMS 52 61
U019			JTAG	TP JTAG CUMULUS M TDO 52 61

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB_90D	*	90_OHM_DIFF	USB	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
U000		USB	USB_90D	USB SOC P 4 47 60
U001		USB	USB_90D	USB SOC N 4 47 60
U002		USB	USB_90D	USB BB P 25 47
U003		USB	USB_90D	USB BB N 25 47
U004		USB	USB_90D	USB BB DEBUG P 25 28 61
U005		USB	USB_90D	USB BB DEBUG N 25 28 61
U006		USB	USB_90D	E75 DPAIR1 CONN P 47 49 60
U007		USB	USB_90D	E75 DPAIR1 CONN N 47 49 60
U008		USB	USB_90D	E75 DPAIR2 CONN P 47 49 60
U009		USB	USB_90D	E75 DPAIR2 CONN N 47 49 60
U010		USB	USB_90D	E75 DPAIR1 P 47
U011		USB	USB_90D	E75 DPAIR1 N 47
U012		USB	USB_90D	E75 DPAIR2 P 47
U013		USB	USB_90D	E75 DPAIR2 N 47

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	4:1_SPACING
HSIC	GND	*	1.5:1_SPACING
HSIC_RDY	*	*	2:1_SPACING
HSIC_RDY	GND	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
U000		HSIC	HSIC	HSIC1 WLAN DATA 4 46 61
U001		HSIC	HSIC	HSIC1 WLAN STB 4 46 61
U002		HSIC	HSIC	HSIC2 BB DATA 4 25 28 61
U003		HSIC	HSIC	HSIC2 BB STB 4 25 28 61
U004		HSIC	HSIC	NC HSIC0 DATA 4
U005		HSIC	HSIC	NC HSIC0 STB 4
U006		HSIC	HSIC_RDY	HSIC1 WLAN2SOC REMOTE WAKE 5 46 61
U007		HSIC	HSIC_RDY	HSIC1 WLAN2SOC DEVICE RDY 5 46 61
U008		HSIC	HSIC_RDY	HSIC1 SOC2WLAN HOST RDY 5 46
U009		HSIC	HSIC_RDY	HSIC1 SOC2WLAN HOST RDY_R 46 61
U010		HSIC	HSIC_RDY	HSIC2 BB2SOC REMOTE WAKE 5 29
U011		HSIC	HSIC_RDY	HSIC2 BB2SOC DEVICE RDY 5 25 29
U012		HSIC	HSIC_RDY	HSIC2 SOC2BB HOST RDY 5 25 29



MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI0C			MIPI0C	*	*	4:1_SPACING
MIPI1C			MIPI1C	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR CLK P	7 23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR CLK N	7 23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR DATA P<0>	7 23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR DATA N<0>	7 23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR DATA P<1>	7 23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR DATA N<1>	7 23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	NC MIPI0C CAM REAR DATA P<2>	7
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	NC MIPI0C CAM REAR DATA N<2>	7
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	NC MIPI0C CAM REAR DATA P<3>	7
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	NC MIPI0C CAM REAR DATA N<3>	7
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR CLK FILT P	23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR CLK FILT N	23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR DATA FILT P<0>	23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR DATA FILT N<0>	23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR DATA FILT P<1>	23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI0C CAM REAR DATA FILT N<1>	23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	NC MIPI0C CAM REAR DATA FILT P<2>	23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	NC MIPI0C CAM REAR DATA FILT N<2>	23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	NC MIPI0C CAM REAR DATA FILT P<3>	23 61
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	NC MIPI0C CAM REAR DATA FILT N<3>	23 61
MIPI1C_PP	MIPI1C_PP	MIPI1C	MIPI1C	MIPI1C CAM FRONT CLK P	7 22 61
MIPI1C_PP	MIPI1C_PP	MIPI1C	MIPI1C	MIPI1C CAM FRONT CLK N	7 22 61
MIPI1C_PP	MIPI1C_PP	MIPI1C	MIPI1C	MIPI1C CAM FRONT DATA P<0>	7 22 61
MIPI1C_PP	MIPI1C_PP	MIPI1C	MIPI1C	MIPI1C CAM FRONT DATA N<0>	7 22 61
MIPI1C_PP	MIPI1C_PP	MIPI1C	MIPI1C	NC MIPI1C CAM FRONT DATA P<1>	7
MIPI1C_PP	MIPI1C_PP	MIPI1C	MIPI1C	NC MIPI1C CAM FRONT DATA N<1>	7
MIPI1C_PP	MIPI1C_PP	MIPI1C	MIPI1C	MIPI1C CAM FRONT CLK FILT P	22 61
MIPI1C_PP	MIPI1C_PP	MIPI1C	MIPI1C	MIPI1C CAM FRONT CLK FILT N	22 61
MIPI1C_PP	MIPI1C_PP	MIPI1C	MIPI1C	MIPI1C CAM FRONT DATA FILT P<0>	22 61
MIPI1C_PP	MIPI1C_PP	MIPI1C	MIPI1C	MIPI1C CAM FRONT DATA FILT N<0>	22 61
MIPI0D_PP	MIPI0D_PP	MIPI0D	MIPI0D	NC MIPI0D DPCLK	7
MIPI0D_PP	MIPI0D_PP	MIPI0D	MIPI0D	NC MIPI0D DNCLK	7
MIPI0D_PP	MIPI0D_PP	MIPI0D	MIPI0D	NC MIPI0D DPDATA0	7
MIPI0D_PP	MIPI0D_PP	MIPI0D	MIPI0D	NC MIPI0D DNDATA0	7
MIPI0D_PP	MIPI0D_PP	MIPI0D	MIPI0D	NC MIPI0D DPDATA1	7
MIPI0D_PP	MIPI0D_PP	MIPI0D	MIPI0D	NC MIPI0D DNDATA1	7
MIPI0D_PP	MIPI0D_PP	MIPI0D	MIPI0D	NC MIPI0D DPDATA2	7
MIPI0D_PP	MIPI0D_PP	MIPI0D	MIPI0D	NC MIPI0D DNDATA2	7
MIPI0D_PP	MIPI0D_PP	MIPI0D	MIPI0D	NC MIPI0D DPDATA3	7
MIPI0D_PP	MIPI0D_PP	MIPI0D	MIPI0D	NC MIPI0D DNDATA3	7
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI CAM0 CLKCON P	
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI CAM0 CLKCON N	
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI CAM0 DOCON P	
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI CAM0 DOCON N	
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI CAM0 DICON P	
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI CAM0 DICON N	
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI CAM0 D2CON P	
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI CAM0 D2CON N	
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI CAM0 D3CON P	
MIPI0C_PP	MIPI0C_PP	MIPI0C	MIPI0C	MIPI CAM0 D3CON N	
MIPI0C_PP	MIPI0C_PP	MIPI1C	MIPI1C	MIPI CAM1 CLKCON P	
MIPI0C_PP	MIPI0C_PP	MIPI1C	MIPI1C	MIPI CAM1 CLKCON N	
MIPI0C_PP	MIPI0C_PP	MIPI1C	MIPI1C	MIPI CAM1 DOCON P	
MIPI0C_PP	MIPI0C_PP	MIPI1C	MIPI1C	MIPI CAM1 DOCON N	
MIPI0C_PP	MIPI0C_PP	MIPI1C	MIPI1C	MIPI CAM1 DICON P	
MIPI0C_PP	MIPI0C_PP	MIPI1C	MIPI1C	MIPI CAM1 DICON N	

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LED	*	LED	LEDA	*	*	2.4:1_SPACING
			LEDB	*	*	2.4:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
LED	LED	LEDA	LEDA	LED IO1 A R	56
LED	LED	LEDB	LEDB	LED IO1 B R	56
LED	LED	LEDA	LEDA	LED IO2 A R	56
LED	LED	LEDR	LEDR	LED IO2 B R	56
LED	LED	LEDA	LEDA	LED IO3 A R	56
LED	LED	LEDB	LEDB	LED IO3 B R	56
LED	LED	LEDA	LEDA	LED IO4 A R	56
LED	LED	LEDR	LEDR	LED IO4 B R	56
LED	LED	LEDA	LEDA	LED IO5 A R	56
LED	LED	LEDB	LEDB	LED IO5 B R	56
LED	LED	LEDA	LEDA	LED IO6 A R	56
LED	LED	LEDB	LEDB	LED IO6 B R	56
LED	LED	LEDA	LEDA	LED IO 1 A	53 56 60
LED	LED	LEDB	LEDB	LED IO 1 B	53 56 60
LED	LED	LEDA	LEDA	LED IO 2 A	53 56 60
LED	LED	LEDB	LEDB	LED IO 2 B	53 56 60
LED	LED	LEDA	LEDA	LED IO 3 A	53 56 60
LED	LED	LEDR	LEDR	LED IO 3 B	53 56 60
LED	LED	LEDA	LEDA	LED IO 4 A	53 56 60
LED	LED	LEDB	LEDB	LED IO 4 B	53 56 60
LED	LED	LEDA	LEDA	LED IO 5 A	53 56 60
LED	LED	LEDB	LEDB	LED IO 5 B	53 56 60
LED	LED	LEDA	LEDA	LED IO 6 A	53 56 60
LED	LED	LEDB	LEDB	LED IO 6 B	53 56 60

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING
AUDIO	AUDIO	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP L1 OUT P	18 49 60	
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP L1 OUT N	18 49 60	
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP L2 OUT P	18 49 60	
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP L2 OUT N	18 49 60	
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP R1 OUT P	17 49 60	
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP R1 OUT N	17 49 60	
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP R2 OUT P	17 49 60	
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP R2 OUT N	17 49 60	
USB_90D	USB	USB	MIKEY TS P	15 47	
USB_90D	USB	USB	MIKEY TS N	15 47	
MAXIMUM_NECK_LENGTH=0.5 MM MIN_NECK_WIDTH=0.06 MM USB_90D	USB	USB	L81 MBUS P	15	
USB_90D	USB	USB	L81 MBUS N	15	
SPKR_DIFF	AUDIO_DIFF	AUDIO	LEFT CH OUT P	15 18 60	
SPKR_DIFF	AUDIO_DIFF	AUDIO	LEFT CH OUT N	15 18 60	
SPKR_DIFF	AUDIO_DIFF	AUDIO	RIGHT CH OUT P	15 17 60	
SPKR_DIFF	AUDIO_DIFF	AUDIO	RIGHT CH OUT N	15 17 60	
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 L1 IN P	18 61	
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 L1 IN N	18 61	
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 R1 IN P	17 61	
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 R1 IN N	17 61	
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 L2 IN P	18 61	
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 L2 IN N	18 61	
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 R2 IN P	17 61	
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 R2 IN N	17 61	
AUDIO_DIFF	AUDIO	AUDIO	SPKR L1 VSNS P		
AUDIO_DIFF	AUDIO	AUDIO	SPKR L1 VSNS N		
AUDIO_DIFF	AUDIO	AUDIO	SPKR R1 VSNS P		
AUDIO_DIFF	AUDIO	AUDIO	SPKR R1 VSNS N		
MAXIMUM_NECK_LENGTH=15 MM PWR_0P5MM	AUDIO	AUDIO	CODEC HP HS3	15	
PWR_0P5MM	AUDIO	AUDIO	CODEC HP HS4	15	
PWR_0P5MM	AUDIO	AUDIO	CONN HP HS3 FILT	15 16 60	
PWR_0P5MM	AUDIO	AUDIO	CONN HP HS4 FILT	15 16 60	
PWR_0P2MM	AUDIO	AUDIO	CODEC HP LEFT	15	
PWR_0P2MM	AUDIO	AUDIO	CODEC HP RIGHT	15	
PWR_0P2MM	AUDIO	AUDIO	CONN HP LEFT FILT	15 16 60	
PWR_0P2MM	AUDIO	AUDIO	CONN HP RIGHT FILT	15 16 60	
PP_PWR	PWR	PWR	L81 NVCP	15 61	
PP_PWR	PWR	PWR	L81 PVCP	15 61	
PP_PWR	PWR	PWR	L81 FLYP	15 61	
PP_PWR	PWR	PWR	L81 FLYN	15 61	
PP_PWR	PWR	PWR	L81 FLYC	15 61	
PP_PWR	PWR	PWR	SPEAKER VO		
PP_PWR	PWR	PWR	L81 FILT	15	
PWR_0P1MM	AUDIO	AUDIO	HP MIC POS	15	
PWR_0P1MM	AUDIO	AUDIO	HP MIC NEG	15	
PWR_0P1MM	AUDIO	AUDIO	L81 AIN2 POS	15	
PWR_0P1MM	AUDIO	AUDIO	L81 AIN2 NEG	15	
PWR_0P1MM	AUDIO	AUDIO	CODEC HP HS3 REF	15	
PWR_0P1MM	AUDIO	AUDIO	CODEC HP HS4 REF	15	
PWR_0P1MM	AUDIO	AUDIO	CONN HP HS3 REF FILT	15 16 60	
PWR_0P1MM	AUDIO	AUDIO	CONN HP HS4 REF FILT	15 16 60	

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
		CRYSTAL	XTAL SOC 24M I	4	
		CRYSTAL	XTAL SOC 24M O	4	
		CRYSTAL	SOC 24M O	4	
		CRYSTAL	PMU XTAL	56	
		CRYSTAL	PMU EXTAL	56	

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF	EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
EDP	EDP	EDP	EDP	EDP AUX P	7 53
EDP	EDP	EDP	EDP	EDP AUX N	7 53
EDP	EDP	EDP	EDP	EDP HPD	7 53
EDP	EDP	EDP	EDP	EDP DATA P<0>	7 53 61
EDP	EDP	EDP	EDP	EDP DATA N<0>	7 53 61
EDP	EDP	EDP	EDP	EDP DATA P<1>	7 53 61
EDP	EDP	EDP	EDP	EDP DATA N<1>	7 53 61
EDP	EDP	EDP	EDP	EDP DATA P<2>	7 53 61
EDP	EDP	EDP	EDP	EDP DATA N<2>	7 53 61
EDP	EDP	EDP	EDP	EDP DATA P<3>	7 53 61
EDP	EDP	EDP	EDP	EDP DATA N<3>	7 53 61
EDP	EDP	EDP	EDP	EDP AUX EMI P	53
EDP	EDP	EDP	EDP	EDP AUX EMI N	53
EDP	EDP	EDP	EDP	EDP DATA EMI P<0>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI N<0>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI P<1>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI N<1>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI P<2>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI N<2>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI P<3>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI N<3>	53 61
EDP	EDP	EDP	EDP	EDP AUX EMI CONN P	53
EDP	EDP	EDP	EDP	EDP AUX EMI CONN N	53
EDP	EDP	EDP	EDP	EDP DATA EMI CONN P<0>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI CONN N<0>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI CONN P<1>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI CONN N<1>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI CONN P<2>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI CONN N<2>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI CONN P<3>	53 61
EDP	EDP	EDP	EDP	EDP DATA EMI CONN N<3>	53 61

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	TEMP_SENSE	BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
BOARD_TEMP	MIN	NECK WIDTH=0.053 MM	BOARD_TEMP	PA NTC P	57 60
BOARD_TEMP	MIN	NECK WIDTH=0.053 MM	BOARD_TEMP	PA NTC N	57
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP2 P	57 60
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP2 N	57
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP3 P	57 60
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP3 N	57
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP4 P	57 60
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP4 N	57
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP5 P	57 60
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP5 N	57
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP6 P	57 60
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP6 N	57
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP7 P	57 60
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP7 N	57
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP8 P	57 60
BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP	BOARD TEMP8 N	57

GRAPE

DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DRAM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DRAM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
8033	DDR_50S	DDR	DDR0_CA<0>	8 12 61
8034	DDR_50S	DDR	DDR0_CA<9...1>	8 12 61
8035	DDR_50S	DDR	DDR0_DM<3...0>	8 12 61
8036	DDR_90D	DDR	DDR0_CK_P	8 12 61
8037	DDR_90D	DDR	DDR0_CK_N	8 12 61
8038	DDR_50S	DDR	DDR0_CKE<1...0>	8 12 61
8039	DDR_50S	DDR	DDR0_CSN<1...0>	8 12 61
8040		DDR	DDR0_CA_ZQ_SOC	8
8041		DDR	DDR0_DO_ZQ_SOC	8
8042		DDR	DDR0_ZQ_DRAM	12
8043	DDR_50S	DDR	DDR0_DQ<1...0>	8 12 61
8044	DDR_50S	DDR	DDR0_DQ<2>	8 12 61
8045	DDR_50S	DDR	DDR0_DQ<7...3>	8 12 61
8046	DDR_90D	DDR	DDR0_DQS_P<0>	8 12 61
8047	DDR_90D	DDR	DDR0_DQS_N<0>	8 12 61
8048	DDR_50S	DDR	DDR0_DQ<15...8>	8 12 61
8049	DDR_90D	DDR	DDR0_DQS_P<1>	8 12 61
8050	DDR_90D	DDR	DDR0_DQS_N<1>	8 12 61
8051	DDR_50S	DDR	DDR0_DQ<23...16>	8 12 61
8052	DDR_90D	DDR	DDR0_DQS_P<2>	8 12 61
8053	DDR_90D	DDR	DDR0_DQS_N<2>	8 12 61
8054	DDR_50S	DDR	DDR0_DQ<27...25>	8 12 61
8055	DDR_50S	DDR	DDR0_DQ<28>	8 12 61
8056	DDR_50S	DDR	DDR0_DQ<31...29>	8 12 61
8057	DDR_90D	DDR	DDR0_DQS_P<3>	8 12 61
8058	DDR_90D	DDR	DDR0_DQS_N<3>	8 12 61
8059				
8060	DDR_50S	DDR	DDR1_CA<3...0>	8 12 61
8061	DDR_50S	DDR	DDR1_CA<9...4>	8 12 61
8062	DDR_50S	DDR	DDR1_DM<3...0>	8 12 61
8063	DDR_90D	DDR	DDR1_CK_P	8 12 61
8064	DDR_90D	DDR	DDR1_CK_N	8 12 61
8065	DDR_50S	DDR	DDR1_CKE<1...0>	8 12 61
8066	DDR_50S	DDR	DDR1_CSN<0>	8 12 61
8067	DDR_50S	DDR	DDR1_CSN<1>	8 12 61
8068				
8069		DDR	DDR1_CA_ZQ_SOC	8
8070		DDR	DDR1_DO_ZQ_SOC	8
8071		DDR	DDR1_ZQ_DRAM	12
8072	DDR_50S	DDR	DDR1_DQ<7...0>	8 12 61
8073	DDR_90D	DDR	DDR1_DQS_P<0>	8 12 61
8074	DDR_90D	DDR	DDR1_DQS_N<0>	8 12 61
8075	DDR_50S	DDR	DDR1_DQ<15...8>	8 12 61
8076	DDR_90D	DDR	DDR1_DQS_P<1>	8 12 61
8077	DDR_90D	DDR	DDR1_DQS_N<1>	8 12 61
8078	DDR_50S	DDR	DDR1_DQ<23...16>	8 12 61
8079	DDR_90D	DDR	DDR1_DQS_P<2>	8 12 61
8080	DDR_90D	DDR	DDR1_DQS_N<2>	8 12 61
8081	DDR_50S	DDR	DDR1_DQ<31...24>	8 12 61
8082	DDR_90D	DDR	DDR1_DQS_P<3>	8 12 61
8083	DDR_90D	DDR	DDR1_DQS_N<3>	8 12 61

VREF (DDR/FMI)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

VOLTAGE	NET_TYPE			
	PHYSICAL	SPACING		
8084	0.6V	PP_PWR	PPVREF_DDR0_CA_SOC	8
8085	0.6V	PP_PWR	PPVREF_DDR0_DO_SOC	8
8086	0.6V	PP_PWR	PPVREF_DDR1_CA_SOC	8
8087	0.6V	PP_PWR	PPVREF_DDR1_DO_SOC	8
8088	0.6V	PP_PWR	PPVREF_DDR0_CA_DRAM	12
8089	0.6V	PP_PWR	PPVREF_DDR0_DO_DRAM	12
8090	0.6V	PP_PWR	PPVREF_DDR1_CA_DRAM	12
8091	0.6V	PP_PWR	PPVREF_DDR1_DO_DRAM	12
8092				
8093	0.9V	PP_PWR	PPVREF_FMI_SOC	6 61
8094	0.9V	PP_PWR	PPVREF_FMI_NAND	14 61

NAND

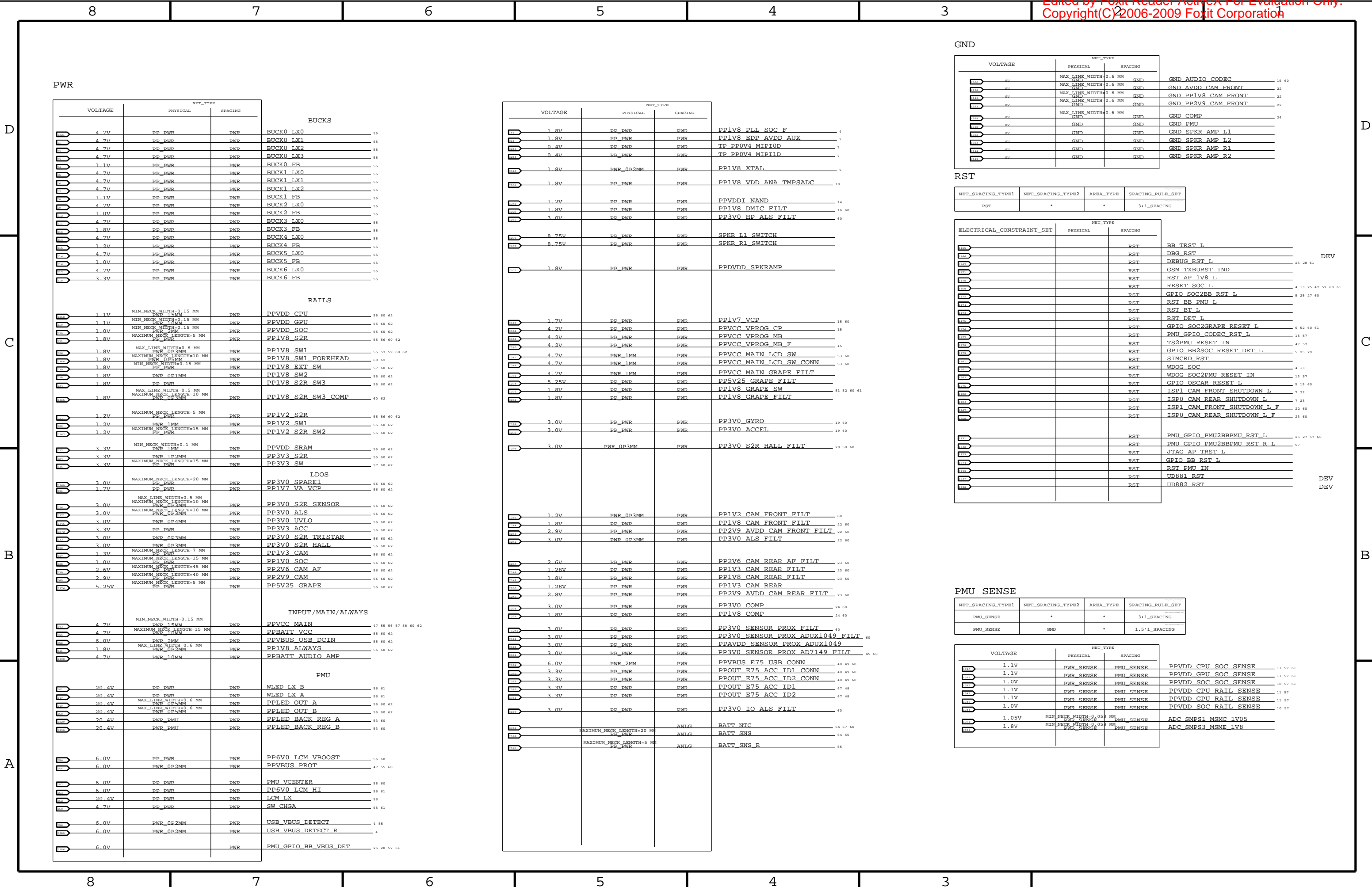
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
8095	FMI0_AD_CTRL_BP	NAND_50S	FMI0_AD<0>	6 14 61
8096	FMI0_AD_CTRL	NAND_50S	FMI0_AD<1>	6 14 61
8097	FMI0_AD_CTRL	NAND_50S	FMI0_AD<2>	6 14 61
8098	FMI0_AD_CTRL	NAND_50S	FMI0_AD<3>	6 14 61
8099	FMI0_AD_CTRL	NAND_50S	FMI0_AD<4>	6 14 61
8100	FMI0_AD_CTRL	NAND_50S	FMI0_AD<5>	6 14 61
8101	FMI0_AD_CTRL	NAND_50S	FMI0_AD<6>	6 14 61
8102	FMI0_AD_CTRL	NAND_50S	FMI0_AD<7>	6 14 61
8103	FMI0_AD_CTRL	NAND_50S	FMI0_ALE	6 14 61
8104	FMI0_CE	NAND_50S	FMI0_CE0_L	6 14 60 61
8105	FMI0_AD_CTRL	NAND_50S	FMI0_CLE	6 14 61
8106		NAND_50S	FMI0_DQS	6 14 61
8107	FMI0_AD_CTRL	NAND_50S	FMI0_RE_L	6 14 61
8108	FMI0_AD_CTRL	NAND_50S	FMI0_WE_L	6 14 61
8109				
8110	FMI1_AD_CTRL	NAND_50S	FMI1_AD<0>	6 14 61
8111	FMI1_AD_CTRL	NAND_50S	FMI1_AD<1>	6 14
8112	FMI1_AD_CTRL	NAND_50S	FMI1_AD<2>	6 14
8113	FMI1_AD_CTRL	NAND_50S	FMI1_AD<3>	6 14
8114	FMI1_AD_CTRL	NAND_50S	FMI1_AD<4>	6 14
8115	FMI1_AD_CTRL	NAND_50S	FMI1_AD<5>	6 14
8116	FMI1_AD_CTRL	NAND_50S	FMI1_AD<6>	6 14
8117	FMI1_AD_CTRL	NAND_50S	FMI1_AD<7>	6 14
8118	FMI1_AD_CTRL	NAND_50S	FMI1_ALE	6 14 61
8119	FMI1_CE	NAND_50S	FMI1_CE0_L	6 14 61
8120	FMI1_AD_CTRL	NAND_50S	FMI1_CLE	6 14 61
8121	FMI1_AD_CTRL	NAND_50S	FMI1_DQS	6 14 61
8122	FMI1_AD_CTRL	NAND_50S	FMI1_RE_L	6 14 61
8123	FMI1_AD_CTRL	NAND_50S	FMI1_WE_L	6 14 61

NAND DEV

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
8124	NAND_50S	NAND	FMI0_AD_BUF<0>	
8125	NAND_50S	NAND	FMI0_AD_BUF<1>	
8126	NAND_50S	NAND	FMI0_AD_BUF<2>	
8127	NAND_50S	NAND	FMI0_AD_BUF<3>	
8128	NAND_50S	NAND	FMI0_AD_BUF<4>	
8129	NAND_50S	NAND	FMI0_AD_BUF<5>	
8130	NAND_50S	NAND	FMI0_AD_BUF<6>	
8131	NAND_50S	NAND	FMI0_AD_BUF<7>	
8132	NAND_50S	NAND	FMI0_ALE_BUF	
8133	NAND_50S	NAND	FMI0_CE0_BUF_L	
8134	NAND_50S	NAND	FMI0_CLE_BUF	
8135	NAND_50S	NAND	FMI0_DQS_BUF	
8136	NAND_50S	NAND	FMI0_DQSN_BUF	
8137	NAND_50S	NAND	FMI0_REP_BUF	
8138	NAND_50S	NAND	FMI0_RE_BUF_L	
8139	NAND_50S	NAND	FMI0_WE_BUF_L	
8140				
8141	NAND_50S	NAND	FMI1_AD_BUF<0>	
8142	NAND_50S	NAND	FMI1_AD_BUF<1>	
8143	NAND_50S	NAND	FMI1_AD_BUF<2>	
8144	NAND_50S	NAND	FMI1_AD_BUF<3>	
8145	NAND_50S	NAND	FMI1_AD_BUF<4>	
8146	NAND_50S	NAND	FMI1_AD_BUF<5>	
8147	NAND_50S	NAND	FMI1_AD_BUF<6>	
8148	NAND_50S	NAND	FMI1_AD_BUF<7>	
8149	NAND_50S	NAND	FMI1_ALE_BUF	
8150	NAND_50S	NAND	FMI1_CE0_BUF_L	
8151	NAND_50S	NAND	FMI1_CLE_BUF	
8152	NAND_50S	NAND	FMI1_DQS_BUF	
8153	NAND_50S	NAND	FMI1_DQSN_BUF	
8154	NAND_50S	NAND	FMI1_REP_BUF	
8155	NAND_50S	NAND	FMI1_RE_BUF_L	
8156	NAND_50S	NAND	FMI1_WE_BUF_L	



PWR

NET_TYPE			BUCKS		
VOLTAGE	PHYSICAL	SPACING			
4.7V	PP_PWR	PWR	BUCK0 LX0	55	
4.7V	PP_PWR	PWR	BUCK0 LX1	55	
4.7V	PP_PWR	PWR	BUCK0 LX2	55	
4.7V	PP_PWR	PWR	BUCK0 LX3	55	
1.1V	PP_PWR	PWR	BUCK0 FB	55	
4.7V	PP_PWR	PWR	BUCK1 LX0	55	
4.7V	PP_PWR	PWR	BUCK1 LX1	55	
4.7V	PP_PWR	PWR	BUCK1 LX2	55	
1.1V	PP_PWR	PWR	BUCK1 FB	55	
4.7V	PP_PWR	PWR	BUCK2 LX0	55	
1.0V	PP_PWR	PWR	BUCK2 FB	55	
4.7V	PP_PWR	PWR	BUCK3 LX0	55	
1.8V	PP_PWR	PWR	BUCK3 FB	55	
4.7V	PP_PWR	PWR	BUCK4 LX0	55	
1.2V	PP_PWR	PWR	BUCK4 FB	55	
4.7V	PP_PWR	PWR	BUCK5 LX0	55	
1.0V	PP_PWR	PWR	BUCK5 FB	55	
4.7V	PP_PWR	PWR	BUCK6 LX0	55	
3.3V	PP_PWR	PWR	BUCK6 FB	55	
			RAILS		
1.1V	MIN_NECK_WIDTH=0.15 MM PWR_15MM	PWR	PPVDD CPU	55 60 62	
1.1V	MIN_NECK_WIDTH=0.15 MM PWR_15MM	PWR	PPVDD GPU	55 60 62	
1.0V	MIN_NECK_WIDTH=0.15 MM PWR_15MM	PWR	PPVDD SOC	55 60 62	
1.8V	MAXIMUM_NECK_LENGTH=5 MM PP_PWR	PWR	PP1V8 S2R	55 56 60 62	
1.8V	MAX_LINE_WIDTH=0.6 MM PWR_0P3MM	PWR	PP1V8 SW1	55 57 59 60 62	
1.8V	MAXIMUM_NECK_LENGTH=10 MM PWR_0P3MM	PWR	PP1V8 SW1 FOREHEAD	60 62	
1.8V	MIN_NECK_WIDTH=0.15 MM PP_PWR	PWR	PP1V8 EXT SW	57 60 62	
1.8V	PWR_0P1MM	PWR	PP1V8 SW2	55 60 62	
1.8V	PP_PWR	PWR	PP1V8 S2R SW3	55 60 62	
1.8V	MAX_LINE_WIDTH=0.5 MM MAXIMUM_NECK_LENGTH=10 MM PWR_0P3MM	PWR	PP1V8 S2R SW3 COMP	60 62	
1.2V	MAXIMUM_NECK_LENGTH=5 MM PP_PWR	PWR	PP1V2 S2R	55 56 60 62	
1.2V	PWR_1MM	PWR	PP1V2 SW1	55 60 62	
1.2V	MAXIMUM_NECK_LENGTH=15 MM PP_PWR	PWR	PP1V2 S2R SW2	55 60 62	
3.3V	MIN_NECK_WIDTH=0.1 MM PWR_1MM	PWR	PPVDD SRAM	55 60 62	
3.3V	PWR_1P2MM	PWR	PP3V3 S2R	55 60 62	
3.3V	MAXIMUM_NECK_LENGTH=15 MM PP_PWR	PWR	PP3V3 SW	57 60 62	
			LDOS		
3.0V	PP_PWR	PWR	PP3V0 SPARE1	56 60 62	
1.7V	PP_PWR	PWR	PP1V7 VA VCP	56 60 62	
3.0V	MAX_LINE_WIDTH=0.5 MM MAXIMUM_NECK_LENGTH=10 MM PWR_0P3MM	PWR	PP3V0 S2R SENSOR	56 60 62	
3.0V	MAXIMUM_NECK_LENGTH=10 MM PWR_0P3MM	PWR	PP3V0 ALS	56 60 62	
3.0V	PWR_0P4MM	PWR	PP3V0 UVLO	56 60 62	
3.3V	PP_PWR	PWR	PP3V3 ACC	56 60 62	
3.0V	PWR_0P3MM	PWR	PP3V0 S2R TRISTAR	56 60 62	
3.0V	PWR_0P3MM	PWR	PP3V0 S2R HALL	56 60 62	
1.3V	MAXIMUM_NECK_LENGTH=7 MM PP_PWR	PWR	PP1V3 CAM	56 60 62	
1.0V	MAXIMUM_NECK_LENGTH=15 MM PP_PWR	PWR	PP1V0 SOC	56 60 62	
2.6V	MAXIMUM_NECK_LENGTH=45 MM PP_PWR	PWR	PP2V6 CAM AF	56 60 62	
2.9V	MAXIMUM_NECK_LENGTH=40 MM PP_PWR	PWR	PP2V9 CAM	56 60 62	
5.25V	MAXIMUM_NECK_LENGTH=5 MM PP_PWR	PWR	PP5V25 GRAPE	56 60 62	
			INPUT/MAIN/ALWAYS		
4.7V	MIN_NECK_WIDTH=0.15 MM PWR_15MM	PWR	PPVCC MAIN	47 55 56 57 58 60 62	
4.7V	MAXIMUM_NECK_LENGTH=15 MM PWR_10MM	PWR	PPBATT VCC	55 60 62	
6.0V	PWR_2MM	PWR	PPVBUS USB DCIN	55 60 62	
1.8V	MAX_LINE_WIDTH=0.6 MM PWR_0P2MM	PWR	PP1V8 ALWAYS	56 60 62	
4.7V	PWR_10MM	PWR	PPBATT AUDIO AMP		
			PMU		
20.4V	PP_PWR	PWR	WLDD LX B	56 61	
20.4V	PP_PWR	PWR	WLDD LX A	56 61	
20.4V	MAX_LINE_WIDTH=0.6 MM PWR_0P3MM	PWR	PPLED OUT A	56 60 62	
20.4V	MAX_LINE_WIDTH=0.6 MM PWR_0P5MM	PWR	PPLED OUT B	56 60 62	
20.4V	PWR_PMU	PWR	PPLED BACK REG A	53 60	
20.4V	PWR_PMU	PWR	PPLED BACK REG B	53 60	
6.0V	PP_PWR	PWR	PP6V0 LCM VBOOST	56 60	
6.0V	PWR_0P2MM	PWR	PPVBUS PROT	47 55 60	
6.0V	PP_PWR	PWR	PMU VCENTER	55 60	
6.0V	PP_PWR	PWR	PP6V0 LCM HI	56 61	
20.4V	PP_PWR	PWR	LCM LX	56	
4.7V	PP_PWR	PWR	SW CHGA	55 61	
6.0V	PWR_0P2MM	PWR	USB VBUS DETECT	4 55	
6.0V	PWR_0P2MM	PWR	USB VBUS DETECT R	4	
6.0V		PWR	PMU GPIO_BB_VBUS_DET	25 28 57 61	

NET_TYPE			BUCKS		
VOLTAGE	PHYSICAL	SPACING			
1.8V	PP_PWR	PWR	PP1V8 PLL SOC F	4	
1.8V	PP_PWR	PWR	PP1V8 EDP AVDD AUX	7	
0.4V	PP_PWR	PWR	TP PP0V4 MIPI0D	7	
0.4V	PP_PWR	PWR	TP PP0V4 MIPI1D	7	
1.8V	PWR_0P2MM	PWR	PP1V8 XTAL	9	
1.8V	PP_PWR	PWR	PP1V8 VDD ANA TMPSADC	10	
1.2V	PP_PWR	PWR	PPVDDI NAND	14	
1.8V	PP_PWR	PWR	PP1V8 DMIC FILT	16 60	
3.0V	PP_PWR	PWR	PP3V0 HP ALS FILT	60	
8.75V	PP_PWR	PWR	SPKR L1 SWITCH		
8.75V	PP_PWR	PWR	SPKR R1 SWITCH		
1.8V	PP_PWR	PWR	PPDVDD SPKRAMP		
1.7V	PP_PWR	PWR	PP1V7 VCP	15 60	
4.2V	PP_PWR	PWR	PPVCC VPROG_CP	16	
4.2V	PP_PWR	PWR	PPVCC VPROG_MB		
4.2V	PP_PWR	PWR	PPVCC VPROG_MB_F	15	
4.7V	PWR_1MM	PWR	PPVCC MAIN LCD SW	53 60	
4.7V	PWR_1MM	PWR	PPVCC MAIN LCD SW CONN	53 60	
4.7V	PWR_1MM	PWR	PPVCC MAIN GRAPE FILT		
5.25V	PP_PWR	PWR	PP5V25 GRAPE FILT		
1.8V	PP_PWR	PWR	PP1V8 GRAPE SW	61 62 60 61	
1.8V	PP_PWR	PWR	PP1V8 GRAPE FILT		
3.0V	PP_PWR	PWR	PP3V0 GYRO	19 60	
3.0V	PP_PWR	PWR	PP3V0 ACCEL	19 60	
3.0V	PWR_0P3MM	PWR	PP3V0 S2R HALL FILT	20 50 60	
1.2V	PWR_0P3MM	PWR	PP1V2 CAM FRONT FILT	60	
1.8V	PP_PWR	PWR	PP1V8 CAM FRONT FILT	22 60	
2.9V	PP_PWR	PWR	PP2V9 AVDD CAM FRONT FILT	22 60	
3.0V	PWR_0P3MM	PWR	PP3V0 ALS FILT	22 60	
2.6V	PP_PWR	PWR	PP2V6 CAM REAR AF FILT	23 60	
1.28V	PP_PWR	PWR	PP1V3 CAM REAR FILT	23 60	
1.8V	PP_PWR	PWR	PP1V8 CAM REAR FILT	23 60	
1.28V	PP_PWR	PWR	PP1V3 CAM REAR		
2.8V	PP_PWR	PWR	PP2V9 AVDD CAM REAR FILT	23 60	
3.0V	PP_PWR	PWR	PP3V0 COMP	24 60	
1.8V	PP_PWR	PWR	PP1V8 COMP	24 60	
3.0V	PP_PWR	PWR	PP3V0 SENSOR PROX FILT	60	
3.0V	PP_PWR	PWR	PP3V0 SENSOR PROX ADUX1049 FILT	60	
3.0V	PP_PWR	PWR	PPAVDD SENSOR PROX ADUX1049		
3.0V	PP_PWR	PWR	PP3V0 SENSOR PROX AD7149 FILT	45 60	
6.0V	PWR_2MM	PWR	PPVBUS E75 USB CONN	48 49 60	
3.3V	PP_PWR	PWR	PPOUT E75 ACC ID1 CONN	48 49 60	
3.3V	PP_PWR	PWR	PPOUT E75 ACC ID2 CONN	48 49 60	
3.3V	PP_PWR	PWR	PPOUT E75 ACC ID1	47 48	
3.3V	PP_PWR	PWR	PPOUT E75 ACC ID2	47 48	
3.0V	PP_PWR	PWR	PP3V0 IO ALS FILT	60	
			BATT NTC		
			MAXIMUM_NECK_LENGTH=20 MM PP_PWR	ANLG	54 57 60
			BATT SNS		
			MAXIMUM_NECK_LENGTH=5 MM PP_PWR	ANLG	54 55
			BATT SNS_R		
			MAXIMUM_NECK_LENGTH=5 MM PP_PWR	ANLG	55

GND

NET_TYPE			GND		
VOLTAGE	PHYSICAL	SPACING			
0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_AUDIO_CODEC	15 60	
0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_AVDD_CAM_FRONT	22	
0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_PP1V8_CAM_FRONT	22	
0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_PP2V9_CAM_FRONT	22	
0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_COMP	24	
0V	GND	GND	GND_PMU		
0V	GND	GND	GND_SPKR_AMP_L1		
0V	GND	GND	GND_SPKR_AMP_L2		
0V	GND	GND	GND_SPKR_AMP_R1		
0V	GND	GND	GND_SPKR_AMP_R2		

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	3:1_SPACING

NET_TYPE			RST		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING			
		RST	BB TRST L		
		RST	DBG RST		
		RST	DEBUG RST L	25 28 61	DEV
		RST	GSM TXBURST IND		
		RST	RST AP 1V8 L		
		RST	RESET SOC L	4 13 25 47 57 60 61	
		RST	GPIO_SOC2BB RST L	5 25 27 60	
		RST	RST BB PMU L		
		RST	RST BT L		
		RST	RST DET L		
		RST	GPIO_SOC2GRAPE RESET L	5 52 60 61	
		RST	PMU GPIO CODEC RST L	15 57	
		RST	TS2PMU RESET IN	47 57	
		RST	GPIO_BB2SOC RESET DET L	6 25 29	
		RST	SIMCRD RST		
		RST	WDOG SOC	4 13	
		RST	WDOG_SOC2PMU RESET IN	13 57	
		RST	GPIO_OSCAR RESET L	5 19 60	
		RST	ISP1_CAM_FRONT_SHUTDOWN L	7 22	
		RST	ISP0_CAM_REAR_SHUTDOWN L	7 23	
		RST	ISP1_CAM_FRONT_SHUTDOWN L F	22 60	
		RST	ISP0_CAM_REAR_SHUTDOWN L F	23 60	
		RST	PMU_GPIO_PMU2BBPMU_RST_L	25 27 57 60	
		RST	PMU_GPIO_PMU2BBPMU_RST_R_L	57	
		RST	JTAG AP TRST L		
		RST	GPIO_BB_RST L		
		RST	RST PMU IN		
		RST	UD881 RST		DEV
		RST	UD882 RST		DEV

PMU SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PMU_SENSE	*	*	3:1_SPACING
PMU_SENSE	GND	*	1.5:1_SPACING

NET_TYPE			PMU_SENSE		
VOLTAGE	PHYSICAL	SPACING			
1.1V	PWR_SENSE	PMU_SENSE	PPVDD CPU SOC SENSE	11 57 61	
1.1V	PWR_SENSE	PMU_SENSE	PPVDD GPU SOC SENSE	11 57 61	
1.0V	PWR_SENSE	PMU_SENSE	PPVDD SOC SOC SENSE	10 57 61	
1.1V	PWR_SENSE	PMU_SENSE	PPVDD CPU RAIL SENSE	11 57	
1.1V	PWR_SENSE	PMU_SENSE	PPVDD GPU RAIL SENSE	11 57	
1.0V	PWR_SENSE	PMU_SENSE	PPVDD SOC RAIL SENSE	10 57	
1.05V	MIN_NECK_WIDTH=0.058 MM PWR_SENSE	PMU_SENSE	ADC_SMPS1 MSMC 1V05		
1.8V	MIN_NECK_WIDTH=0.058 MM PWR_SENSE	PMU_SENSE	ADC_SMPS3 MSME 1V8		



RF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RF_50S	*	50_OHM_RF	100_RF	*	*	100_RF_CLEAR_SPACING
			50_RF	*	*	50_RF_SPACING
			50_RF_CLEAR	*	*	50_RF_CLEAR_SPACING
RF_100D	*	100_OHM_RF	RF_60	*	*	1.2:1_SPACING

NET_TYPE			PP BATT VCC 2G FEM	40
VOLTAGE	PHYSICAL	SPACING		
4.7V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP PA	34
3.8V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP PA	34
1.8V	MIN_NECK_WIDTH=0.06 MM	DWR_RF	PP LVS1	26
1.3V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP RF1 1V3 DRX FE	31
4.7V UNDEFINED	MAX_LINE_WIDTH=1 MM	DWR_RF	PP VREG	26
2.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP RF2 2V05 DRX BB	31
4.7V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP BATT VCC PA DCDC	26
1.8V	MIN_NECK_WIDTH=0.06 MM	DWR_RF	PP LDO1	26
1.8V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP LDO2 XO HS 1V8	26
1.8V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP LDO3 AMUX 1V8	26
3.3V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP LDO4 VDDA 3V3	26
2.5V	MIN_NECK_WIDTH=0.06 MM	DWR_RF	PP LDO5 GPS LNA 2V5	26
1.8V	MAXIMUM_NECK_LENGTH=5 MM	DWR_RF	PP LDO6 RUIIM 1V8	26
1.8V	MIN_NECK_WIDTH=0.15 MM	DWR_RF	PP LDO6 RUIIM 1V8 FILT	44
1.8V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP LDO7 DAC 1V8	26
1.2V	MAXIMUM_NECK_LENGTH=9 MM	DWR_RF	PP LDO8 VDDPX 1V2	26
1.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP LDO9 PLL 1V05	26
1.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP LDO10 ADSP 1V05	26
1.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP LDO11 MDSP FW 1V05	26
1.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP LDO12 MDSP SW 1V05	26
2.95V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP LDO13 VDDPX 2V95	26
2.65V	MAXIMUM_NECK_LENGTH=4 MM	DWR_RF	PP LDO14 2V65	26
1.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP VSW S1	36
1.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP SMPS1 MSMC 1V05	26
1.3V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP VSW S2	26
1.3V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP SMPS2 RF1 1V3	26
1.8V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP VSW S3	26
1.8V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP RF1 1V8 DIG	31
1.8V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP SMPS3 MSME 1V8 FILT	31
2.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP VSW S4	26
2.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP SMPS4 RF2 2V05	26
1.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP VSW S5	26
1.05V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP SMPS5 DSP 1V05	26
4.7V	MAX_LINE_WIDTH=1 MM	DWR_RF	PP BATT VCC PA DCDC IN2	26

NET_TYPE			50 HSIC CAL	28
PHYSICAL	SPACING			
45_OHM_SF	RF_60		50 XCVR B13 B17 B20 TX	30
RF_50S	50_RF_CLEAR		50 XCVR 2G LB TX	30
RF_50S	50_RF_CLEAR		50 XCVR B8 TX	30
RF_50S	50_RF_CLEAR		50 XCVR B5 B18 TX	30
RF_50S	50_RF_CLEAR		50 XCVR B2 B25 TX	30
RF_50S	50_RF_CLEAR		50 XCVR 2G HB TX	30
RF_50S	50_RF_CLEAR		50 XCVR B3 B4 TX	30
RF_50S	50_RF_CLEAR		50 XCVR B1 TX	30
RF_50S	50_RF_CLEAR		50 PDET IN	30
RF_50S	50_RF_CLEAR		50 PDET PAD OUT	30
RF_50S	50_RF_CLEAR		50 PDET PAD IN	30
RF_50S	50_RF_CLEAR		50 B1 TX SAW IN	32
RF_50S	50_RF_CLEAR		50 B3 B4 TX SAW IN	32
RF_50S	50_RF_CLEAR		50 B2 B25 TX SAW IN	32
RF_50S	50_RF_CLEAR		50 B1 TX SAW OUT	33
RF_50S	50_RF_CLEAR		50 B2 TX SAW OUT	33
RF_50S	50_RF_CLEAR		50 B3 TX SAW OUT	33
RF_50S	50_RF_CLEAR		50 B4 TX SAW OUT	33
RF_50S	50_RF_CLEAR		50 B5 TX SAW OUT	33
RF_50S	50_RF_CLEAR		50 B8 TX SAW OUT	33
RF_50S	50_RF_CLEAR		50 B13 TX SAW OUT	33
RF_50S	50_RF_CLEAR		50 B17 TX SAW OUT	33
RF_50S	50_RF_CLEAR		50 B20 TX SAW OUT	33
RF_50S	50_RF_CLEAR		50 PCS RX	39
RF_50S	50_RF_CLEAR		50 PCS RX MATCH	39
RF_50S	50_RF_CLEAR		50 DCS RX	39
RF_50S	50_RF_CLEAR		50 DCS RX MATCH	39

NET_TYPE			50 B1 TX PAD IN	34
PHYSICAL	SPACING			
RF_50S	50_RF_CLEAR		50 B4 TX PAD IN	34
RF_50S	50_RF_CLEAR		50 B1 B4 DPLX ANT	34
RF_50S	50_RF_CLEAR		50 B1 B4 ANT	34
RF_50S	50_RF_CLEAR		50 B1 B4 ANT PHASESHIFT	34
RF_50S	50_RF_CLEAR		50 B2 TX PAD IN	35
RF_50S	50_RF_CLEAR		50 B3 TX PAD IN	35
RF_50S	50_RF_CLEAR		50 B2 DUPLX RX	32
RF_50S	50_RF_CLEAR		50 B3 DUPLX RX	32
RF_50S	50_RF_CLEAR		50 B2 DPLX ANT	35
RF_50S	50_RF_CLEAR		50 B3 DPLX ANT	35
RF_50S	50_RF_CLEAR		50 B2 ANT	35
RF_50S	50_RF_CLEAR		50 B3 ANT	35
RF_50S	50_RF_CLEAR		50 B2 RX BALUN	32
RF_50S	50_RF_CLEAR		50 B3 RX BALUN	32
RF_50S	50_RF_CLEAR		50 B2 ANT PHASESHIFT	35
RF_50S	50_RF_CLEAR		50 B3 ANT PHASESHIFT	35
RF_50S	50_RF_CLEAR		50 B20 TX PAD IN	36
RF_50S	50_RF_CLEAR		50 B20 DPLX ANT	36
RF_50S	50_RF_CLEAR		50 B20 ANT	36
RF_50S	50_RF_CLEAR		50 B20 ANT PHASESHIFT	36
RF_50S	50_RF_CLEAR		50 B5 TX PAD IN	37
RF_50S	50_RF_CLEAR		50 B8 TX PAD IN	37
RF_50S	50_RF_CLEAR		50 B5 DPLX ANT	37
RF_50S	50_RF_CLEAR		50 B8 DPLX ANT	37
RF_50S	50_RF_CLEAR		50 B5 ANT	37
RF_50S	50_RF_CLEAR		50 B8 ANT	37
RF_50S	50_RF_CLEAR		50 B5 ANT PHASESHIFT	37
RF_50S	50_RF_CLEAR		50 B8 ANT PHASESHIFT	37
RF_50S	50_RF_CLEAR		50 B7 ANT	36
RF_50S	50_RF_CLEAR		50 B7 BALUN IN RX	36
RF_50S	50_RF_CLEAR		50 B7 DPLX ANT	36
RF_50S	50_RF_CLEAR		50 B7 DUPLX RX	32
RF_50S	50_RF_CLEAR		50 B7 TX PAD IN	36
RF_50S	50_RF_CLEAR		50 B7 TX SAW IN	36
RF_50S	50_RF_CLEAR		50 B7 TX SAW OUT	36
RF_50S	50_RF_CLEAR		50 XCVR B7 TX	30
RF_50S	50_RF_CLEAR		50 B13 TX PAD IN	38
RF_50S	50_RF_CLEAR		50 B17 TX PAD IN	38
RF_50S	50_RF_CLEAR		50 B13 DPLX ANT	38
RF_50S	50_RF_CLEAR		50 B17 DPLX ANT	38
RF_50S	50_RF_CLEAR		50 B13 LFF IN	38
RF_50S	50_RF_CLEAR		50 B13 ANT	38
RF_50S	50_RF_CLEAR		50 B17 ANT	38
RF_50S	50_RF_CLEAR		50 B13 ANT PHASESHIFT	38
RF_50S	50_RF_CLEAR		50 B17 ANT PHASESHIFT	38
RF_50S	50_RF_CLEAR		50 XCVR 2G LB TX MATCH	40
RF_50S	50_RF_CLEAR		50 XCVR 2G HB TX MATCH	40
RF_50S	50_RF_CLEAR		50 2G LB PA IN	40
RF_50S	50_RF_CLEAR		50 2G HB PA IN	40
RF_50S	50_RF_CLEAR		50 PRI ANT ASM	40
RF_50S	50_RF_CLEAR		50 DRX ANT TEST	41
RF_50S	50_RF_CLEAR		50 DRX ANT PHASESHIFT	41
RF_50S	50_RF_CLEAR		50 DRX ANT FEED	41
RF_50S	50_RF_CLEAR		50 COUPLER TERM	41
RF_50S	50_RF_CLEAR		50 DIVERSITY SWITCH MATCH	41
RF_50S	50_RF_CLEAR		50 GPS LNA OUT	41
RF_50S	50_RF_CLEAR		50 GPS ANT COAX	42
RF_50S	50_RF_CLEAR		50 GPS ANT MATCH	42
RF_50S	50_RF_CLEAR		50 GPS ANT TEST	42
RF_50S	50_RF_CLEAR		50 PRI ANT COAX	40
RF_50S	50_RF_CLEAR		50 ANT2 TERM	40
RF_50S	50_RF_CLEAR		50 DRX ANT TERM	40
RF_60	2G FEM S0		2G FEM S1	29
RF_60	2G FEM S1		2G FEM S2	29
RF_60	2G FEM S2		2G FEM S3	29
RF_60	2G FEM S3		2G FEM S4	29
RF_60	2G FEM S4		2G FEM S5	29
RF_60	2G FEM S5		2G FEM S6	29
RF_60	BB PDM		BB PDM	39
RF_60	BB PDM FILT		DCDC ADJ	39
RF_60	DCDC ADJ		PA R1	29

NET_TYPE			WTR GP DATA0	29
PHYSICAL	SPACING			
RF_60	RF_60		WTR GP DATA1	29
RF_60	RF_60		BB ERROR FLAG	29
RF_60	RF_60		PA ON B1 B4	29
RF_60	RF_60		PA ON B2 B3	29
RF_60	RF_60		PA ON B5 B8	29
RF_60	RF_60		PA ON B7 B20	29
RF_60	RF_60		PA ON B13 B17	29
RF_60	RF_60		PA BS	29
RF_60	RF_60		LAT SW1 CTL	29
RF_60	RF_60		PS HOLD	29
RF_60	RF_60		WTR RF ON	29
RF_60	RF_60		WTR RX ON	29
RF_60	RF_60		DCDC MODE	29
RF_60	RF_60		DCDC ENABLE	29
RF_60	RF_60		DRX ASM V1	29
RF_60	RF_60		DRX ASM V2	29
RF_60	RF_60		DRX ASM V3	29
RF_60	RF_60		DRX ASM V4	29
RF_60	RF_60		19P2M CLK EN	29
RF_60	RF_60		PMIC RESOUT L	29
RF_60	RF_60		PMIC SSB1	29

NET_TYPE			TX BB O P	29
PHYSICAL	SPACING			
RF_DIFF	RF_DIFF	RF_60	TX BB O N	29
RF_DIFF	RF_DIFF	RF_60	DRX BB O P	29
RF_DIFF	RF_DIFF	RF_60	DRX BB O N	29
RF_DIFF	RF_DIFF	RF_60	GPS BB O P	29
RF_DIFF	RF_DIFF	RF_60	GPS BB O N	29
RF_DIFF	RF_DIFF	RF_60	PRX BB O P	29
RF_DIFF	RF_DIFF	RF_60	PRX BB O N	29
RF_DIFF	RF_DIFF	RF_60	DRX BB I P	29
RF_DIFF	RF_DIFF	RF_60	DRX BB I N	29
RF_DIFF	RF_DIFF	RF_60	GPS BB I P	29
RF_DIFF	RF_DIFF	RF_60	GPS BB I N	29
RF_DIFF	RF_DIFF	RF_60	PRX BB I P	29
RF_DIFF	RF_DIFF	RF_60	PRX BB I N	29
RF_DIFF	RF_DIFF	RF_60	TX BB I P	29
RF_DIFF	RF_DIFF	RF_60	TX BB I N	29
RF_DIFF	RF_100D	100_RF	100 XCVR B13 B17 B20 PRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B13 B17 B20 PRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR B8 PRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B8 PRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR B5 B18 PRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B5 B18 PRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR B2 B25 PRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B2 B25 PRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR B3 PRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B3 PRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR DCS PCS PRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR DCS PCS PRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR B1 B4 PRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B1 B4 PRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR B8 B20 DRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B8 B20 DRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR B5 B18 B13 B17 DRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B5 B18 B13 B17 DRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR B2 B25 B3 DRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B2 B25 B3 DRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR B1 B4 DRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B1 B4 DRX N	30
RF_DIFF	RF_100D	100_RF	100 XCVR GPS RX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR GPS RX N	30
RF_DIFF	RF_100D	100_RF	100 B13 DUPLX RX P	30
RF_DIFF	RF_100D	100_RF	100 B13 DUPLX RX N	30
RF_DIFF	RF_100D	100_RF	100 B17 DUPLX RX P	30
RF_DIFF	RF_100D	100_RF	100 B17 DUPLX RX N	30
RF_DIFF	RF_100D	100_RF	100 B20 DUPLX RX P	30
RF_DIFF	RF_100D	100_RF	100 B20 DUPLX RX N	30
RF_DIFF	RF_100D	100_RF	100 DCS PCS RX FILTER P	30
RF_DIFF	RF_100D	100_RF	100 DCS PCS RX FILTER N	30
RF_DIFF	RF_100D	100_RF	100 B1 B4 DUPLX RX P	30
RF_DIFF	RF_100D	100_RF	100 B1 B4 DUPLX RX N	30
RF_DIFF	RF_100D	100_RF	100 B8 DUPLX RX P	30
RF_DIFF	RF_100D	100_RF	100 B8 DUPLX RX N	30
RF_DIFF	RF_100D	100_RF	100 B5 B18 DUPLX RX P	30
RF_DIFF	RF_100D	100_RF	100 B5 B18 DUPLX RX N	30
RF_DIFF	RF_100D	100_RF	100 B7 PRX BALUN OUT P	30
RF_DIFF	RF_100D	100_RF	100 B7 PRX BALUN OUT N	30
RF_DIFF	RF_100D	100_RF	100 B7 PRX MATCH P	30
RF_DIFF	RF_100D	100_RF	100 B7 PRX MATCH N	30
RF_DIFF	RF_100D	100_RF	100 XCVR B7 PRX P	30
RF_DIFF	RF_100D	100_RF	100 XCVR B7 PRX N	30
RF_CLK			SLEEP_CLK 32K	25
RF_CLK			19P2M_WTR	27
RF_CLK			19P2M_MDM	27

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
50_RF_SPACING	TOP,BOTTOM	0.178 MM	?	GND	50_RF	*	50_RF_CLEAR_SPACING
50_RF_SPACING	ISL3	0.130 MM	?	GND	50_RF_CLEAR	*	50_RF_CLEAR_SPACING
50_RF_SPACING	*	0.092 MM	?	GND	100_RF	*	100_RF_CLEAR_SPACING
50_RF_CLEAR_SPACING	TOP,BOTTOM	0.178 MM	?	GND	RF_60	*	1.2:1_SPACING
50_RF_CLEAR_SPACING	ISL3	0.130 MM	?	GND	PWR_RF	*	1.2:1_SPACING
50_RF_CLEAR_SPACING	*	0.138 MM	?	PWR_RF	PWR_RF	*	1.2:1_SPACING
100_RF_CLEAR_SPACING	TOP,BOTTOM	0.143 MM	?	RF_CLK	*	*	3:1_SPACING
100_RF_CLEAR_SPACING	*	0.118 MM	?	RF_CLK	GND	*	1.2:1_SPACING

NC PMU\_OUT 32K CLK GPS PMU\_OUT 32K CLK GPS

