

Preliminary Work for Exp. #3

1) I write a subroutine which sends a GPIO port the necessary signals to demonstrate the Full Step Mode in both directions (clockwise or counterclockwise).

```

1  GPIO_PORTB_ICR      EQU      0X4000541C
2  GPIO_PORTB_RIS      EQU      0X40005414
3  PB_OUT              EQU      0X400053C0
4
5                      AREA isr,   CODE,   READONLY,   ALIGN=2
6                      THUMB
7                      EXPORT  My_ST_ISR
8
9  My_ST_ISR           PROC
10                     CMP      R5,#0
11                     BNE      CCW
12  CW                 LDR      R1,=PB_OUT
13                     LDR      R0,[R1]
14                     LSL      R0,#1
15                     CMP      R0,#0X100
16                     MOVEQ    R0,#0X10
17                     STR      R0,[R1]
18                     B        last
19  CCW                LDR      R1,=PB_OUT
20                     LDR      R0,[R1]
21                     LSR      R0,#1
22                     CMP      R0,#0X08
23                     MOVEQ    R0,#0X80
24                     STR      R0,[R1]
25  last              BX      LR
26                     ALIGN
27                     ENDP
28                     END
29

```

Figure 1. ISR OF THE Q1

2) I design a system that has two inputs from push buttons and provides a step to the stepper motor upon input. One button is to provide a step for clockwise rotation and the other is for counterclockwise rotation. I use 4 buttons of the 4x4 Keypad Module introduced in Experiment-2. ,

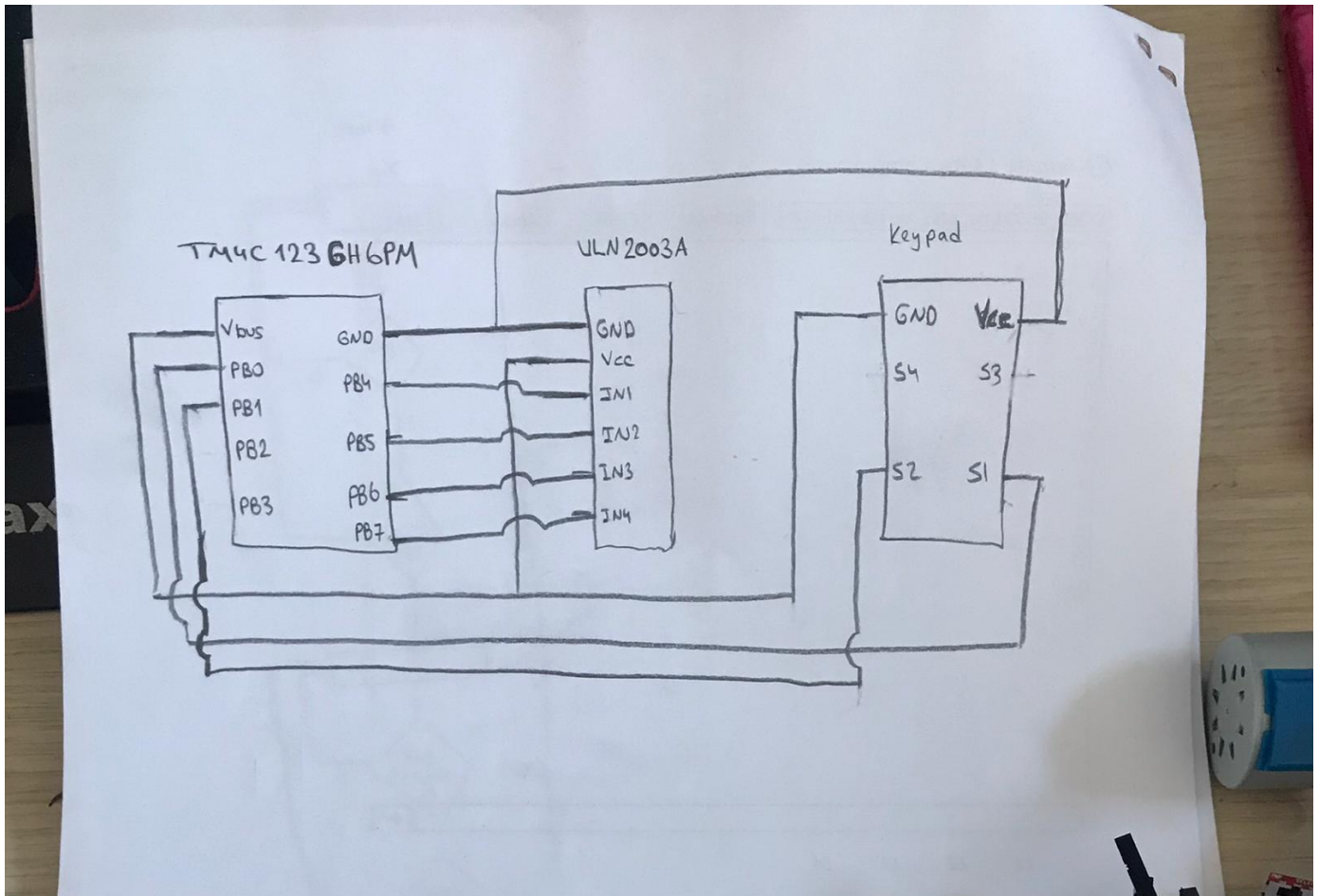


Figure 2. Drawing the connections between TM4C123G, ULN2003A's board, 4x4 Keypad Module.

3) According to my hardware design in step-2, I write a program that, in an infinite loop, gives a step upon the release of one button and gives a step in the opposite direction upon the release of the other button. I assume that the other button is never pushed until the pressed button is released. The response of the motor should be after the button release. I am aware of bouncing inherent in the buttons.

```

1  PB_OUT          EQU      0X400053C0
2  PB_INP          EQU      0X4000503C
3
4
5
6      AREA main,   CODE,   READONLY,   ALIGN=2
7      THUMB
8      IMPORT      PORTB_Init
9      IMPORT      DELAY100
10     EXPORT      __main
11
12
13 __main          PROC
14                 ;BL      InitSysTick
15                 BL      PORTB_Init
16                 MOV      R5,#2
17
18
19 LOOP            LDR      R0,=PB_INP
20                 LDRB     R1,[R0]
21                 BL      DELAY100
22                 LDRB     R2,[R0]
23                 CMP      R1,R2
24                 BNE      LOOP
25                 CMP      R1,#0X00
26                 BEQ      LOOP
27                 CPY      R4,R1
28 RELEASE        LDRB     R1,[R0]
29                 BL      DELAY100
30                 LDRB     R2,[R0]
31                 CMP      R1,R2
32                 BNE      RELEASE
33                 CMP      R1,#0X00
34                 BNE      RELEASE
35                 CPYEQ    R5,R4
36
37                 CMP      R5,#1
38                 BNE      CCW
39
40                 BNE      CCW
41
42 CW              LDR      R1,=PB_OUT
43                 LDR      R0,[R1]
44                 LSL      R0,#1
45                 CMP      R0,#0X100
46                 MOVEQ    R0,#0X10
47                 STR      R0,[R1]
48                 B        last
49
50 CCW             LDR      R1,=PB_OUT
51                 LDR      R0,[R1]
52                 LSR      R0,#1
53                 CMP      R0,#0X08
54                 MOVEQ    R0,#0X80
55                 STR      R0,[R1]
56
57 last           B        LOOP
58
59                 ENDP
60                 END

```

Figure 3. MAIN OF THE Q3

```

1  PB_OUT          EQU      0X400053C0
2
3      AREA isr,    CODE,    READONLY,    ALIGN=2
4      THUMB
5      EXPORT      My_ST_ISR
6
7  My_ST_ISR       PROC
8
9              CMP      R5,#1
10             BNE      CCW
11
12  CW              LDR      R1,=PB_OUT
13                 LDR      R0,[R1]
14                 LSL      R0,#1
15                 CMP      R0,#0X100
16                 MOVEQ     R0,#0X10
17                 STR      R0,[R1]
18                 B        last
19
20  CCW             LDR      R1,=PB_OUT
21                 LDR      R0,[R1]
22                 LSR      R0,#1
23                 CMP      R0,#0X08
24                 MOVEQ     R0,#0X80
25                 STR      R0,[R1]
26
27
28  last            BX      LR
29                 ALIGN
30                 ENDP
31                 END

```

Figure 4. ISR OF THE Q3

4) At this stage, I design a system that has 4 inputs from push buttons to control a stepper motor. One button is for speeding up, one is for slowing down, the other two are for directions. I use 4 buttons of the 4x4 Keypad Module introduced in Experiment-2.

The necessary connections between TM4C123G, ULN2003A's board, 4x4 Keypad Module and stepper motor is like part2. However, in this part I connect PB4 to S4, PB2 to S3. So, I use 3rd button for speed up, and 4th button for speed down.

5) According to my hardware design in part-4, write a program that, in an infinite loop, drives a stepper motor speed and direction of which can be controlled by external push buttons. I assume that the no button is ever pushed until a pressed button is released. The controls should be applied upon releasing the corresponding button. I am aware of bouncing inherent in the buttons.

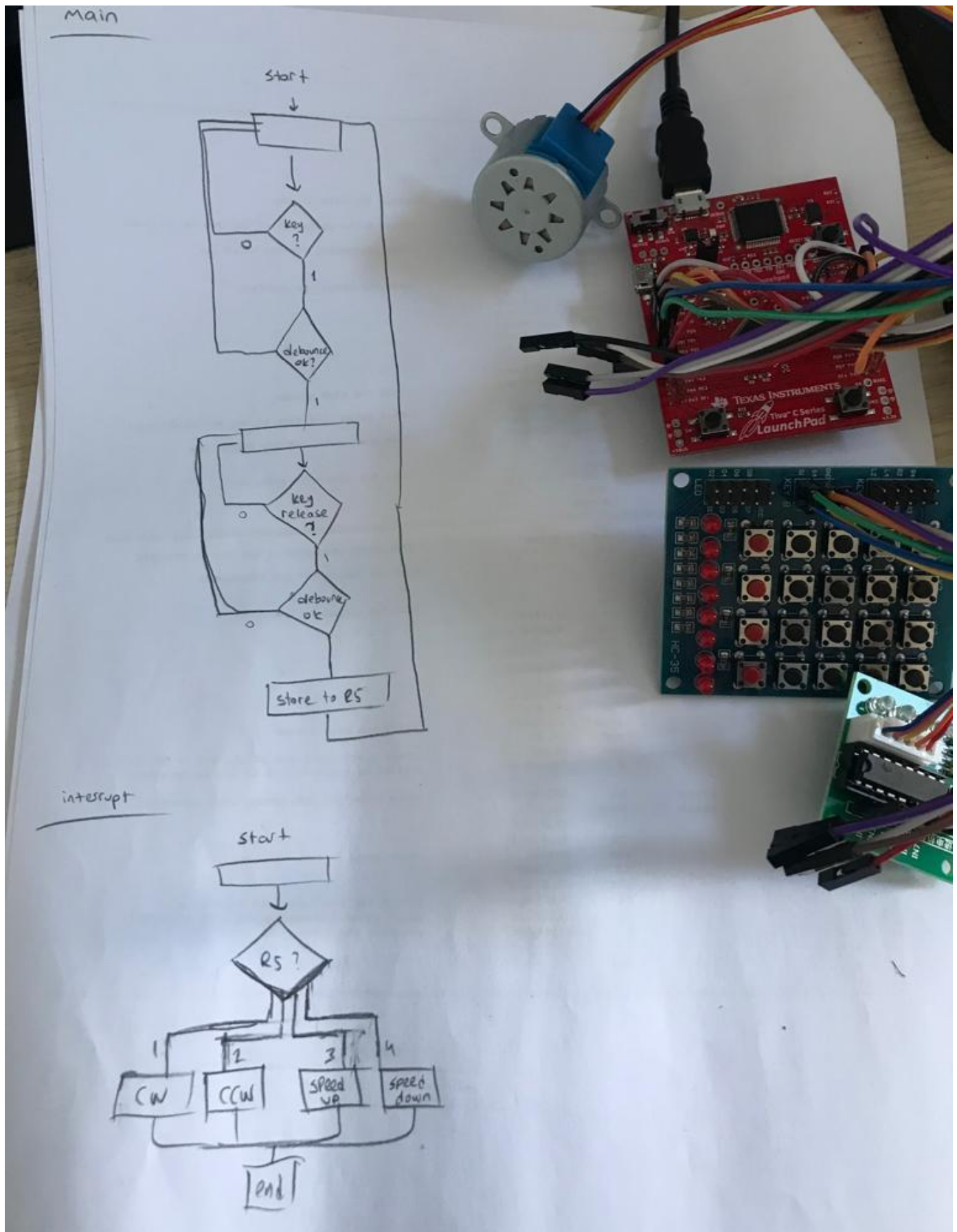


Figure5. Flowchart of my algorithm

```

1  PB_INP      EQU      0X4000503C
2              AREA main, CODE, READONLY, ALIGN=2
3              THUMB
4              IMPORT    PORTB_Init
5              IMPORT    DELAY100
6              IMPORT    InitSysTick
7              EXPORT    __main
8
9
10 __main      PROC
11             BL        InitSysTick
12             BL        PORTB_Init
13             MOV       R5, #1
14
15 LOOP        LDR        R0, =PB_INP
16             LDRB      R1, [R0]
17             BL        DELAY100
18             LDRB      R2, [R0]
19             CMP       R1, R2
20             BNE       LOOP
21             CMP       R1, #0X00
22             BEQ       LOOP
23             CPY       R4, R1
24 RELEASE     LDRB      R1, [R0]
25             BL        DELAY100
26             LDRB      R2, [R0]
27             CMP       R1, R2
28             BNE       RELEASE
29             CMP       R1, #0X00
30             BNE       RELEASE
31             CPYEQ     R5, R4
32             B         LOOP
33             ENDP
34             END

```

Figure 6. MAIN OF THE Q5

```

1              AREA subroutine, READONLY, CODE
2              THUMB
3              EXPORT    DELAY100
4
5 DELAY100
6             PUSH     {R0}
7             MOV32    R0, #600000
8 LOOP        SUBS     R0, #1
9             BNE      LOOP
10            POP      {R0}
11            BX       LR
12            ALIGN
13            END

```

Figure 7. DELAY100


```

1  GPIO_PORTB_ICR      EQU      0X4000541C
2  GPIO_PORTB_RIS      EQU      0X40005414
3  PB_OUT              EQU      0X400053C0
4  NVIC_ST_RELOAD      EQU      0XE000E014
5  NVIC_ST_CURRENT     EQU      0XE000E018
6  RELOAD_VALUE        EQU      0X20000400
7
8
9
10         AREA isr,    CODE,    READONLY,    ALIGN=2
11         THUMB
12         EXPORT      My_ST_ISR
13 My_ST_ISR      PROC
14             CMP      R5,#0X01
15             BEQ      CW
16             CMP      R5,#0X02
17             BEQ      CCW
18             CMP      R5,#0X04
19             BEQ      FAST
20             CMP      R5,#0X08
21             BEQ      SLOW
22
23 FAST          LDR      R1,=RELOAD_VALUE
24             LDR      R0,[R1]
25             CMP      R0,#0X3000
26             CPYEQ    R5,R6
27             BEQ      EXIT
28             SUB      R0,#0X3000
29             STR      R0,[R1]
30             LDR      R1,=NVIC_ST_RELOAD
31             STR      R0,[R1]
32             ;LDR      R1,=NVIC_ST_CURRENT
33             ;STR      R0,[R1]
34             CPY      R5,R6
35
36 SLOW          CPY      R5,R6
37             B        last
38             LDR      R1,=RELOAD_VALUE
39             LDR      R0,[R1]
40             ADD      R0,#0X3000
41             STR      R0,[R1]
42             LDR      R1,=NVIC_ST_RELOAD
43             STR      R0,[R1]
44             ;LDR      R1,=NVIC_ST_CURRENT
45             ;STR      R0,[R1]
46             CPY      R5,R6
47             B        last
48 CW           LDR      R1,=PB_OUT
49             LDR      R0,[R1]
50             LSL      R0,#1
51             CMP      R0,#0X100
52             MOVEQ    R0,#0X10
53             STR      R0,[R1]
54             CPY      R6,R5
55             B        last
56 CCW          LDR      R1,=PB_OUT
57             LDR      R0,[R1]
58             LSR      R0,#1
59             CMP      R0,#0X08
60             MOVEQ    R0,#0X80
61             STR      R0,[R1]
62             CPY      R6,R5
63             B        last
64 last         BX      LR
65             ALIGN
66             ENDP
67             END

```

Figure 8. ISR OF THE Q5

```

1  GPIO_PORTB_DIR_R      EQU      0X40005400
2  GPIO_PORTB_AFSEL_R    EQU      0X40005420
3  GPIO_PORTB_DEN_R      EQU      0X4000551C
4  GPIO_PORTB_AMSEL_R    EQU      0X40005528
5  GPIO_PORTB_PDR        EQU      0X40005514
6  GPIO_PORTB_IS         EQU      0X40005404
7  GPIO_PORTB_IBE        EQU      0X40005408
8  GPIO_PORTB_IEV        EQU      0X4000540C
9  GPIO_PORTB_IM         EQU      0X40005410
10 GPIO_PORTB_ICR        EQU      0X4000541C
11 GPIO_PORTB_RIS        EQU      0X40005414
12 PB_INP                EQU      0X4000503C
13 PB_OUT                EQU      0X400053C0
14 SYSCCTL_RCGC2_R       EQU      0X400FE608
15
16         AREA init_gpio, CODE,   READONLY,   ALIGN=2
17         THUMB
18         EXPORT          PORTB_Init
19
20
21 PORTB_Init  PROC
22
23             LDR          R1,=SYSCCTL_RCGC2_R
24             LDR          R0,[R1]
25             ORR          R0,R0,#0X02 ;only port b
26             STR          R0,[R1]
27             NOP
28             NOP
29             NOP
30             LDR          R1,=GPIO_PORTB_DIR_R
31             LDR          R0,[R1]
32             ORR          R0,R0,#0XF0
33             BIC          R0,R0,#0X0F
34             STR          R0,[R1]

```

```

23             LDR          R1,=SYSCCTL_RCGC2_R
24             LDR          R0,[R1]
25             ORR          R0,R0,#0X02 ;only port b
26             STR          R0,[R1]
27             NOP
28             NOP
29             NOP
30             LDR          R1,=GPIO_PORTB_DIR_R
31             LDR          R0,[R1]
32             ORR          R0,R0,#0XF0
33             BIC          R0,R0,#0X0F
34             STR          R0,[R1]
35             LDR          R1,=GPIO_PORTB_AFSEL_R
36             LDR          R0,[R1]
37             BIC          R0,R0,#0XFF
38             STR          R0,[R1]
39             LDR          R1,=GPIO_PORTB_PDR
40             MOV          R0,#0X0F
41             STR          R0,[R1]
42             LDR          R1,=GPIO_PORTB_DEN_R
43             LDR          R0,[R1]
44             ORR          R0,R0,#0XFF
45             STR          R0,[R1]
46             LDR          R1,=GPIO_PORTB_AMSEL_R
47             LDR          R0,[R1]
48             BIC          R0,R0,#0XFF
49             STR          R0,[R1]
50             LDR          R1,=PB_OUT
51             MOV          R0,#0X20
52             STR          R0,[R1]
53             BX           LR
54         ENDP
55         END

```

Figure 9. GPIO PORTB INITIALIZATION OF Q5


```

1 RELOAD_VALUE EQU 0X0000C000
2 RELOAD_ADDRESS EQU 0X20000400
3 NVIC_ST_CTRL EQU 0XE000E010
4 NVIC_ST_RELOAD EQU 0XE000E014
5 NVIC_ST_CURRENT EQU 0XE000E018
6 SHP_SYSPRI3 EQU 0XE000ED20
7 PB_OUT EQU 0X400053C0
8
9 AREA init_isr, CODE, READONLY, ALIGN=2
10 THUMB
11 EXPORT InitSysTick
12
13 InitSysTick PROC
14 LDR R1,=NVIC_ST_CTRL
15 MOV R0,#0
16 STR R0,[R1]
17 LDR R1,=NVIC_ST_RELOAD
18 LDR R0,=RELOAD_VALUE
19 STR R0,[R1]
20 LDR R1,=RELOAD_ADDRESS
21 STR R0,[R1]
22 LDR R1,=NVIC_ST_CURRENT
23 LDR R0,=RELOAD_VALUE
24 STR R0,[R1]
25 LDR R1,=SHP_SYSPRI3
26 MOV R0,#0X40000000
27 STR R0,[R1]
28 LDR R1,=NVIC_ST_CTRL
29 MOV R0,#0X03
30 STR R0,[R1]
31 CPSIE I
32 BX LR
33 ENDP
34 END

```

Figure 10. SYSTICK INITIALIZATION OF Q5