

## Develop Your Projects

During development, you can use the Vivado Design Suite. You can implement project files in your project. Run.bat file will be used only evaluation phase by us.

## Arrange Environment Files

- Open Run.bat file using the text editor.
- You must arrange the first line according to the installation directory. Under the installation directory, there must be a “settings64.bat” file. You should give this file path in the first line.

```
1 call C:\Xilinx\Vivado\2017.4\settings64.bat
2
3 mkdir Simulation_Files
4 cd Simulation_Files
5
6 ::Register Simulation
7 call xvlog ../Register.v
8 call xvlog ../RegisterSimulation.v
9 call xvlog ../Helper.v
```

## Example Submission Files

The required project files are given under “ExampleSubmission.zip” files. You must use these modules **without** changing names. The explanation for each file is given below. **The files must be the same as given.** Please do not put files in a folder. **If you do not submit it as ExampleSubmission.zip, the evaluation may not execute. You may get ZERO points.**

Name	Explanation	Require Edit
Register.v	Register Module	YES
RegisterSimulation.v	Simulation Test Bench of Register Module.	You can add new tests to the given test scenario.
RegisterFile.v	Register File Module	YES
RegisterFileSimulation.v	Simulation Test Bench of Register Module	You can add new tests to the given test scenario.
AddressRegisterFile.v	Address Register File Module	YES
AddressRegisterFileSimulation.v	Simulation Test Bench of Address Register Module	You can add new tests to the given test scenario.
InstructionRegister.v	Instruction Register Module	YES
InstructionRegisterSimulation.v	Simulation Test Bench of Instruction Register Module	You can add new tests to the given test scenario.
ArithmeticLogicUnit	Arithmetic Logic Unit Module	YES
ArithmeticLogicUnitSimulation.v	Simulation Test Bench of Arithmetic Logic Unit Module	You can add new tests to the given test scenario.
Memory.v	Memory Module	NO
RAM.mem	The data file of memory module	You can add new tests to the given test scenario.
ArithmeticLogicUnitSystem.v	Arithmetic Logic Unit System Module	YES

ArithmeticLogicUnitSystemSimulation.v	Simulation Test Bench of Arithmetic Logic Unit System Module	You can add new tests to the given test scenario.
Helper.v	Helper module for the simulation modules.	NO
Run.bat	Execution Script of Testbench Files	Only first line
Report.pdf	Report file of the Project 1	You must replace it with your report.
GroupMembers.xlsx	Student Numbers and Names of the group members. (If your teammate does not make any contribution, please <b>DO NOT WRITE</b> his/her name.)	YES

## Run TestBench

- Open Command Prompt.
- Go to the project directory to arrange for submission.
- Write “Run.bat” command. Click Enter.

```

C:\Windows\System32\cmd.exe
C:\Users\SoftSensorsLab\VivadoProjects\BLG222E_2324_Project1\Submission>Run.bat
C:\Users\SoftSensorsLab\VivadoProjects\BLG222E_2324_Project1\Submission>call D:\Xilinx\Vivado\2017.4\settings64.bat
A subdirectory or file Simulation_Files already exists.
INFO: [VRFC 10-2263] Analyzing Verilog file "C:/Users/SoftSensorsLab/VivadoProjects/BLG222E_2324_Project1/Submission/Register.v" into library work
INFO: [VRFC 10-311] analyzing module Register
INFO: [VRFC 10-2263] Analyzing Verilog file "C:/Users/SoftSensorsLab/VivadoProjects/BLG222E_2324_Project1/Submission/RegisterSimulation.v" into library work
INFO: [VRFC 10-311] analyzing module RegisterSimulation
INFO: [VRFC 10-2263] Analyzing Verilog file "C:/Users/SoftSensorsLab/VivadoProjects/BLG222E_2324_Project1/Submission/Helper.v" into library work
INFO: [VRFC 10-311] analyzing module FileOperation
INFO: [VRFC 10-311] analyzing module CrystalOscillator
Vivado Simulator 2017.4
Copyright 1986-1999, 2001-2016 Xilinx, Inc. All Rights Reserved.
Running: D:/Xilinx/Vivado/2017.4/bin/unwrapped/win64.o/xelab.exe -top RegisterSimulation -snapshot regsim -debug typical
Multi-threading is on. Using 6 slave threads.
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module work.CrystalOscillator
Compiling module work.Register
Compiling module work.FileOperation
Compiling module work.RegisterSimulation
Built simulation snapshot regsim

***** xsim v2017.4 (64-bit)
**** SW Build 2086221 on Fri Dec 15 20:55:39 MST 2017
**** IP Build 2085800 on Fri Dec 15 22:25:07 MST 2017
** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

source xsim.dir/regsim/xsim_script.tcl
# xsim {regsim} -autoloadwcfg -runall
Vivado Simulator 2017.4
Time resolution is 1 ps
run -all

=====
Register Simulation Started
[PASS] Test No: 1, Component: Q, Actual Value: 0x0025, Expected Value: 0x0025
[PASS] Test No: 2, Component: Q, Actual Value: 0x0024, Expected Value: 0x0024
[PASS] Test No: 3, Component: Q, Actual Value: 0x0025, Expected Value: 0x0025
[PASS] Test No: 4, Component: Q, Actual Value: 0x0026, Expected Value: 0x0026
[PASS] Test No: 5, Component: Q, Actual Value: 0x0025, Expected Value: 0x0025
[PASS] Test No: 6, Component: Q, Actual Value: 0x0012, Expected Value: 0x0012
[PASS] Test No: 7, Component: Q, Actual Value: 0x0025, Expected Value: 0x0025

```

- Under the “Simulation\_Files” folder created by “Run.bat”, there are “debug.txt” and “evaluation.csv” files. The “debug.txt” file consists of testbench results for you. You should fix your design in case there are failed cases. The “evaluation.csv” file consists of the same results for the automatic evaluation system.