

## Lab 5: Arithmetic Logic Unit

The purpose of the lab is to build an Arithmetic Logic Unit (ALU). An ALU is a combinational circuit that can perform mathematical operations, and is an essential building block for most circuits ([https://en.wikipedia.org/wiki/Arithmetic\\_logic\\_unit](https://en.wikipedia.org/wiki/Arithmetic_logic_unit)).

- 1) Design an ALU. It should be able to perform **addition, subtraction, comparison, shift left** and **shift right**. Choose one **arithmetic**, one **logical** and one **shift** operation from the list of functions on the Wikipedia page and include these operations as well. Your ALU should therefore be able to do **eight** operations in total. Implement it in VHDL in a modular fashion. Display the output through LEDs. Show the RTL schematics and working FPGA to your TA and get their approval. Include RTL schematics and representative photos of your working FPGA in your report.