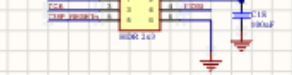
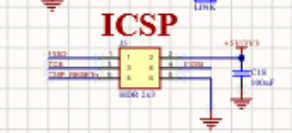
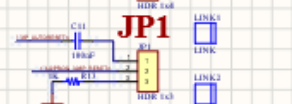
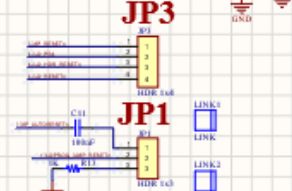
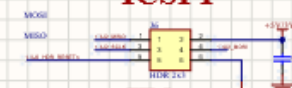
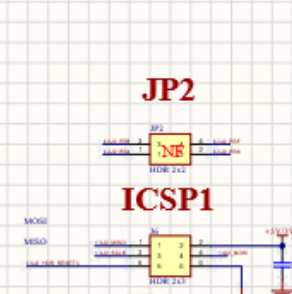
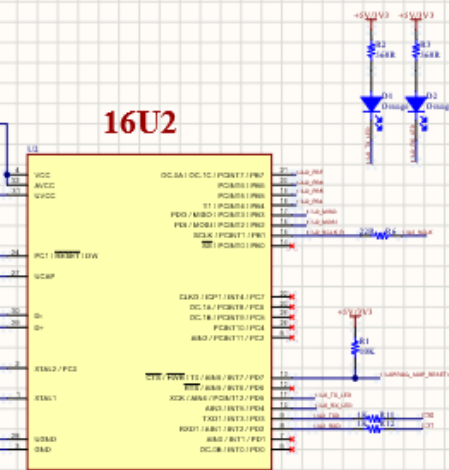
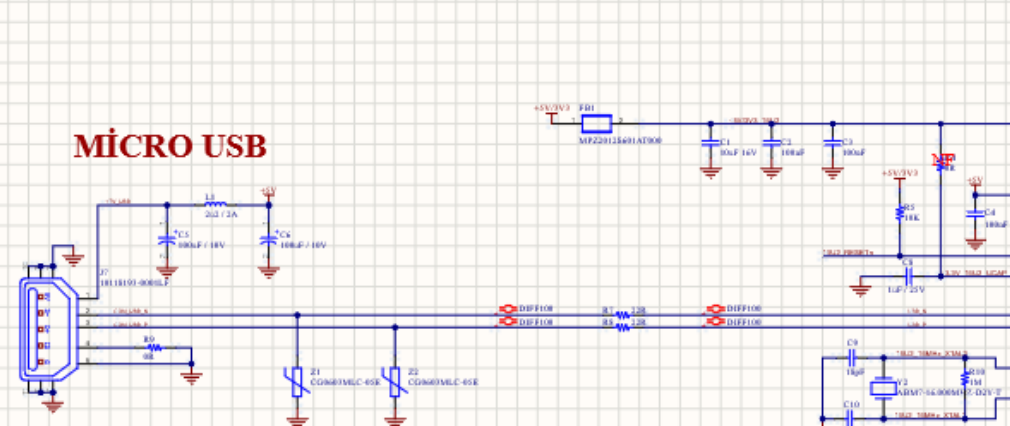


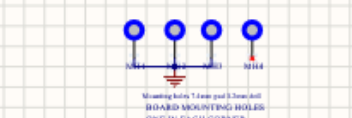
[illegible]

**DISCUSS IN QTR:**  
*Round 1P1*  
 "Johnston was awarded a \$100K R&D. In this case, "101 2 is used to count 320P" when there is a credit 320P in qualified from *Academic 100*.  
 "3" 1012 0P1 credit Awarded. Award 2013. "101 2 10000 jobs is exempted by 1012 during *ERRT*. If paid for, then after Round from 1 0122 will go into 0P1 credit 101s from credit minus you save Enrich 1012 10000000000 1200 and about 100 million. <http://www.alexandersonsbooks.com>."



## MOUNTING HOLE

Mounting holes 7.6mm and 5.08mm drill  
BOARD MOUNTING HOLES



## RESET(16U2)

The diagram illustrates the RESET circuit for the 16U2 microcontroller. A 10k resistor is connected between the +5V supply and the input of an AND gate. A 100nF capacitor is connected between the input of the AND gate and ground. The output of the AND gate is connected to the RESET pin of the 16U2. The 16U2 is shown with its pins labeled: 1 (GND), 2 (VCC), 3 (GND), 4 (VCC), 5 (GND), 6 (VCC), 7 (GND), 8 (VCC), 9 (GND), 10 (VCC), 11 (GND), 12 (VCC), 13 (GND), 14 (VCC), 15 (GND), 16 (VCC), 17 (GND), 18 (VCC), 19 (GND), 20 (VCC), 21 (GND), 22 (VCC), 23 (GND), 24 (VCC), 25 (GND), 26 (VCC), 27 (GND), 28 (VCC), 29 (GND), 30 (VCC), 31 (GND), 32 (VCC), 33 (GND), 34 (VCC), 35 (GND), 36 (VCC), 37 (GND), 38 (VCC), 39 (GND), 40 (VCC), 41 (GND), 42 (VCC), 43 (GND), 44 (VCC), 45 (GND), 46 (VCC), 47 (GND), 48 (VCC), 49 (GND), 50 (VCC), 51 (GND), 52 (VCC), 53 (GND), 54 (VCC), 55 (GND), 56 (VCC), 57 (GND), 58 (VCC), 59 (GND), 60 (VCC), 61 (GND), 62 (VCC), 63 (GND), 64 (VCC), 65 (GND), 66 (VCC), 67 (GND), 68 (VCC), 69 (GND), 70 (VCC), 71 (GND), 72 (VCC), 73 (GND), 74 (VCC), 75 (GND), 76 (VCC), 77 (GND), 78 (VCC), 79 (GND), 80 (VCC), 81 (GND), 82 (VCC), 83 (GND), 84 (VCC), 85 (GND), 86 (VCC), 87 (GND), 88 (VCC), 89 (GND), 90 (VCC), 91 (GND), 92 (VCC), 93 (GND), 94 (VCC), 95 (GND), 96 (VCC), 97 (GND), 98 (VCC), 99 (GND), 100 (VCC).

[illegible]

**LAYOUT NOTE:**  
 1) Route all the POWER tracks with minimum track width 8.4mm.  
 2) Route all the other tracks by 6.4mm and change them by the end of the device to 0.2mm. To change all of them at once, use this filter  
 "not !onN1(100) and not !onN2(GND) and !onN3 and !onLayer(L1)" or  
 "onLayer(L2)" and then set 0.2mm width in PCB Inspector panel.