Given:

Processor Address Size: 24 bits

Cache Capacity: 4K words of 32 bits = 4 * 1024 = 4096 words

Line Size: 2 × 16-bit words = 1 line = 32 bits = 4 bytes

Associativity: 4-way

Processor Word Size: 16-bit

Solution:

1. Calculate Total Cache Size in Bytes

- 4096 words × 4 bytes (32 bits) = 16,384 bytes (16 KB)

2. Calculate Number of Cache Lines

- Each cache line = 4 bytes
- Number of lines = 16,384 / 4 = 4096 lines

3. Determine Number of Sets

- It is a 4-way set associative cache
- Number of sets = 4096 lines / 4 = 1024 sets

4. Breakdown of 24-bit Address

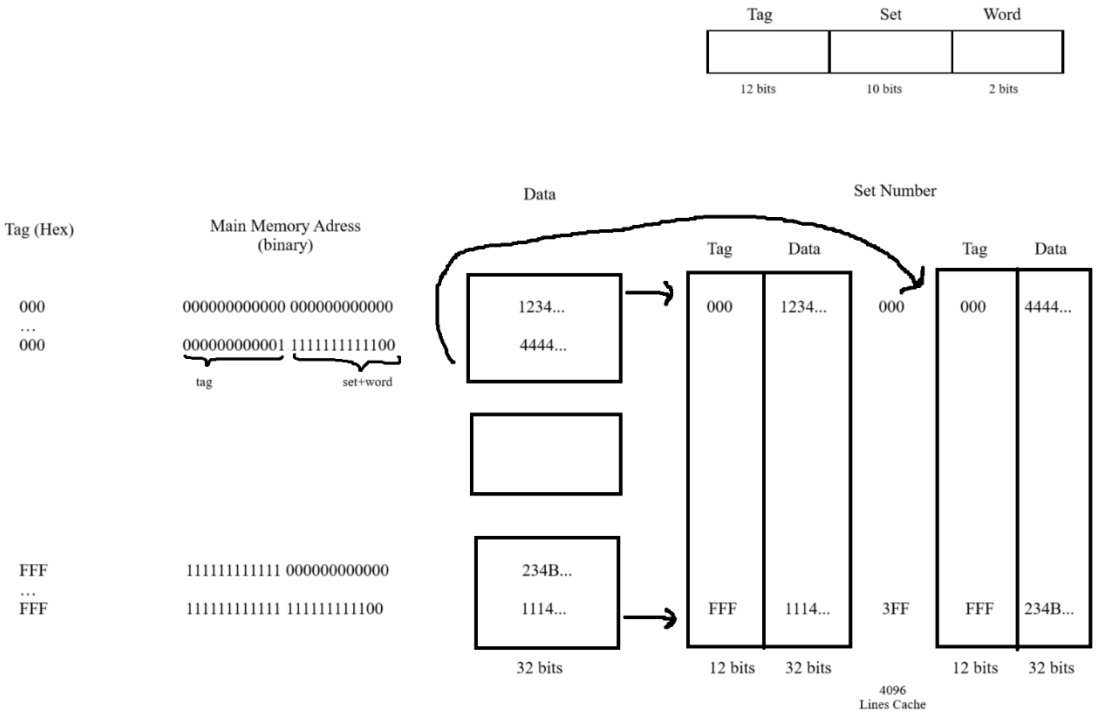
Now, split the 24-bit memory address into:

Block Offset (Word Offset):
- Each line holds 2 words (each 16 bits = 2 bytes), total line = 4 bytes
- To identify 1 word in a line → needs 1 bit (2 words = 2^1)
- To locate the byte → 2 bytes per word = 1 bit
- So: 1 bit for Word and 1 bit for byte in Word ⇒ Total Offset = 2 bits

Set Index: 1024 sets = 2^10; so, 10 bits for Set Index

Tag: 24 − (10 + 2) = 12 bits for Tag

Diagram


Tag
Set
Word
12 bits
10 bits
2 bits
Data
Set Number
Tag (Hex)
Main Memory Adress
(binary)
Tag
Data
Tag
Data
000
…
000
000000000000 000000000000
000000000001 111111111100
tag
set+word
1234...
4444...
000
1234...
000
000
4444...
FFF
…
FFF
111111111111 000000000000
111111111111 111111111100
234B...
1114...
FFF
1114...
3FF
FFF
234B...
32 bits
12 bits
32 bits
12 bits
32 bits
4096
Lines Cache