



# STD20NF20 STF20NF20, STP20NF20

N-channel 200 V, 0.10  $\Omega$ , 18 A DPAK, TO-220, TO-220FP  
low gate charge STripFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>W</sub>
STD20NF20	200 V	< 0.125 $\Omega$	18 A	110 W
STF20NF20	200 V	< 0.125 $\Omega$	18 A	30 W
STP20NF20	200 V	< 0.125 $\Omega$	18 A	110 W

- Exceptional dv/dt capability
- Low gate charge
- 100% avalanche tested

## Application

- Switching applications

## Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

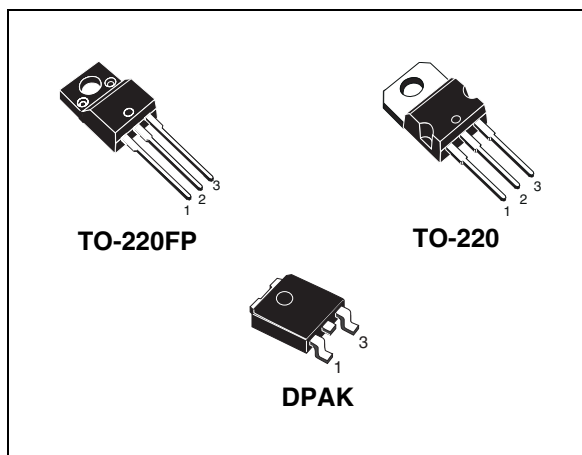


Figure 1. Internal schematic diagram

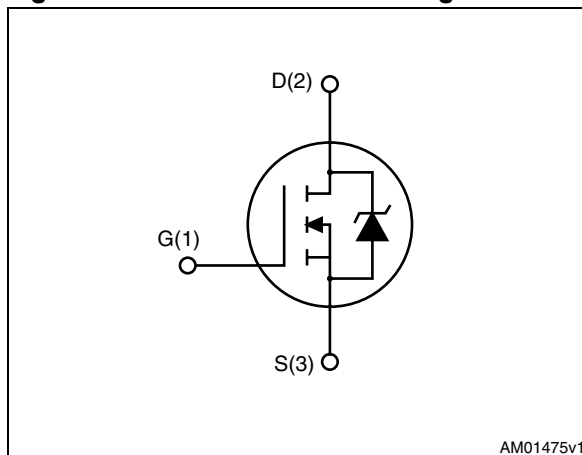


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD20NF20	20NF20	DPAK	Tape and reel
STF20NF20	20NF20	TO-220FP	Tube
STP20NF20	20NF20	TO-220	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, DPAK	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	200		V
$V_{GS}$	Gate- source voltage	$\pm 20$		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	18		A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	11		A
$I_{DM}^{(1)}$	Drain current (pulsed)	72		A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	110	30	W
	Derating factor	0.72	0.2	W/ $^{\circ}\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15		V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^{\circ}\text{C}$ )		2500	V
$T_{stg}$	Storage temperature	-55 to 175		$^{\circ}\text{C}$
$T_j$	Max. operating junction temperature			

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 18\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	TO-220	DPAK	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.38	1.38	5	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	50 <sup>(1)</sup>	62.5	$^{\circ}\text{C}/\text{W}$
$T_I$	Maximum lead temperature for soldering purpose			300	$^{\circ}\text{C}$

1. When mounted on 1inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	18	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	110	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	200			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$		0.10	0.125	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 25\text{ V}$ , $I_D = 10\text{ A}$	-	13		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	940 197 30		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 100\text{ V}$ , $I_D = 10\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 15)	-	15 30 40 10		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 160\text{ V}$ , $I_D = 20\text{ A}$ , $V_{GS} = 10\text{ V}$ (see Figure 16)	-	28 5.6 14.5	39	nC nC nC

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		18 72	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ (see Figure 20)	-	155 775 10		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ , $T_j = 150\text{ }^{\circ}\text{C}$ (see Figure 20)	-	183 1061 11.6		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, DPAK

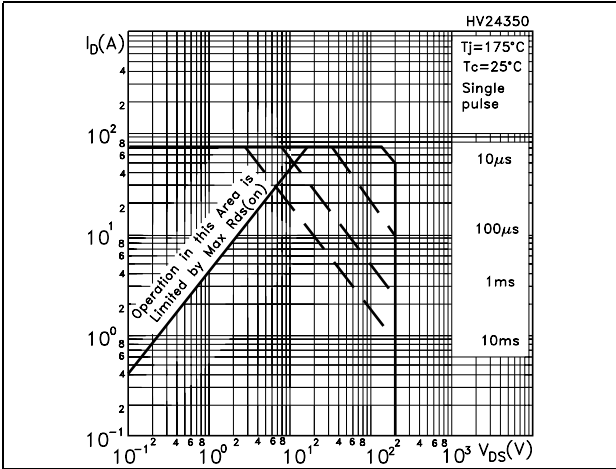


Figure 3. Thermal impedance area for TO-220, DPAK

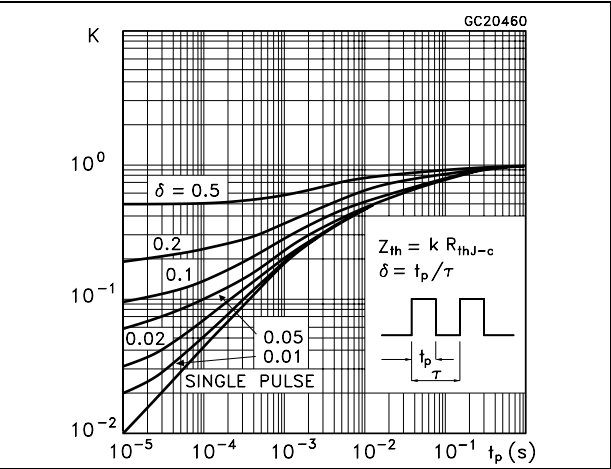


Figure 4. Safe operating area for TO-220FP

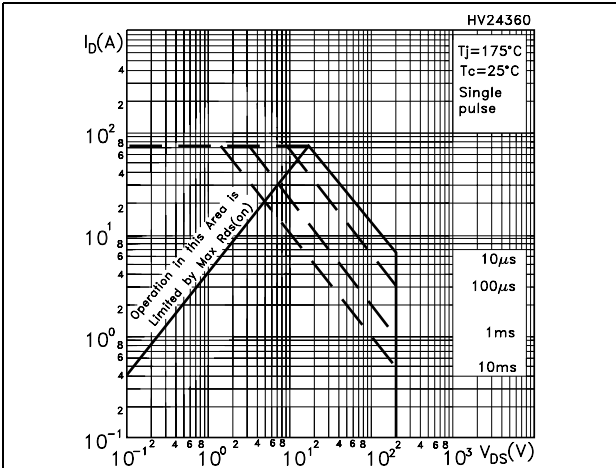


Figure 5. Thermal impedance for TO-220FP

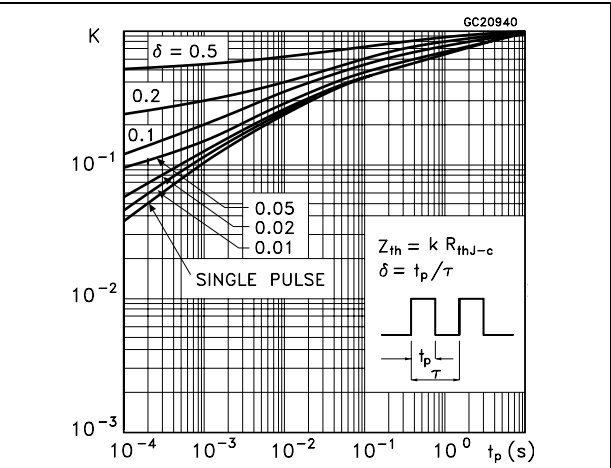


Figure 6. Output characteristics

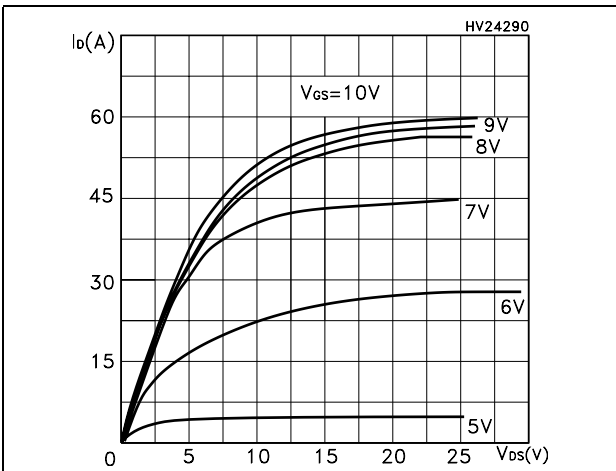


Figure 7. Transfer characteristics

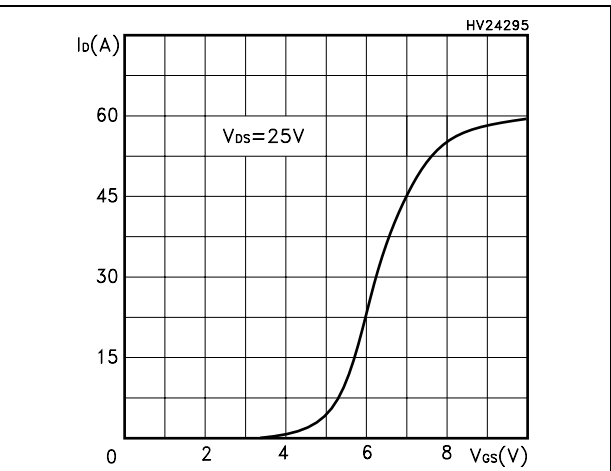


Figure 8. Transconductance

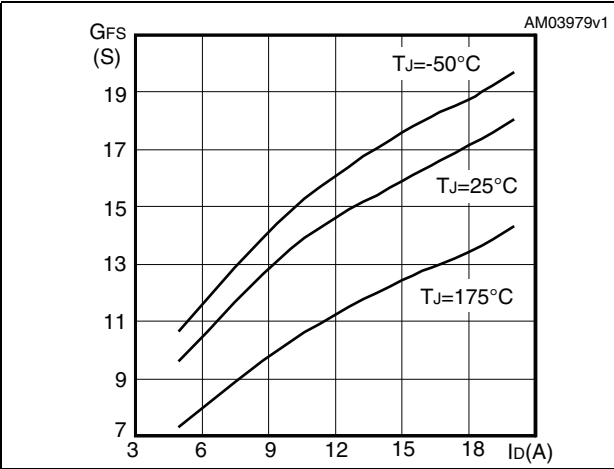


Figure 9. Static drain-source on resistance

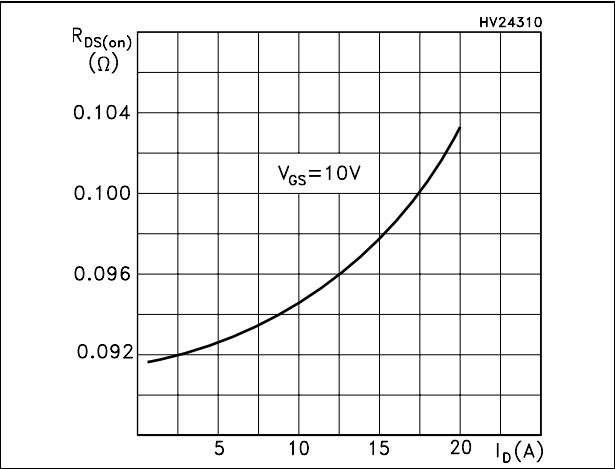


Figure 10. Gate charge vs gate-source voltage

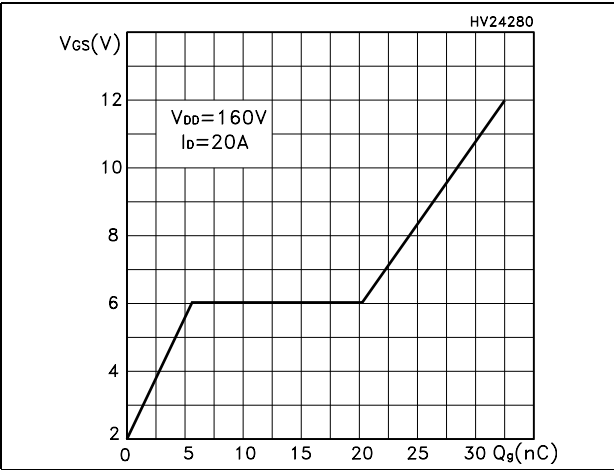


Figure 11. Capacitance variations

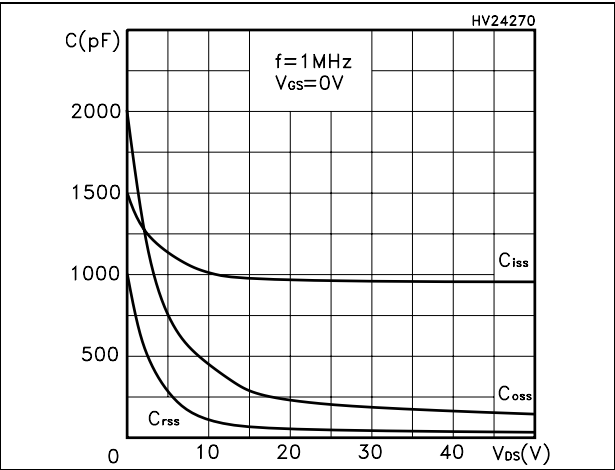


Figure 12. Normalized gate threshold voltage vs temperature

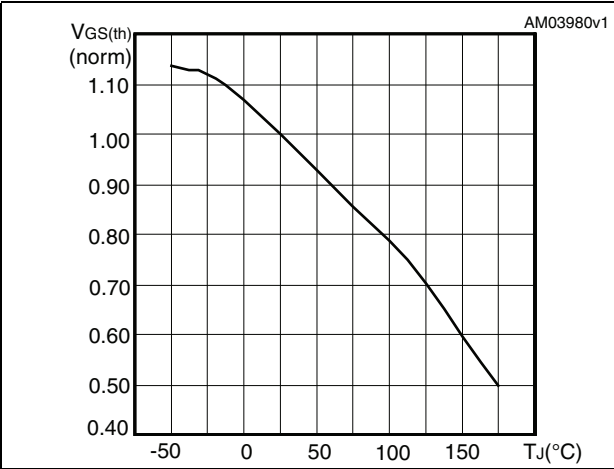


Figure 13. Normalized on resistance vs temperature

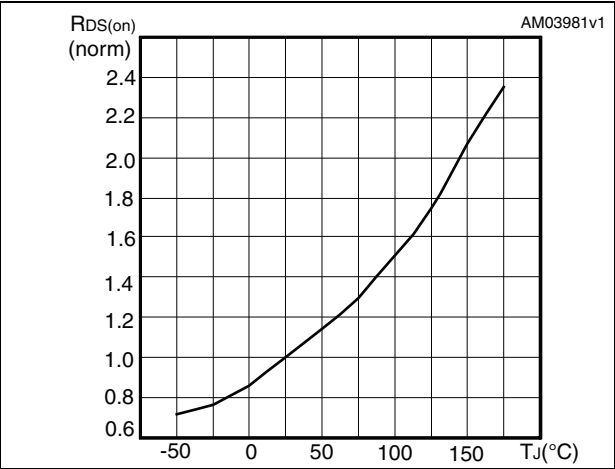
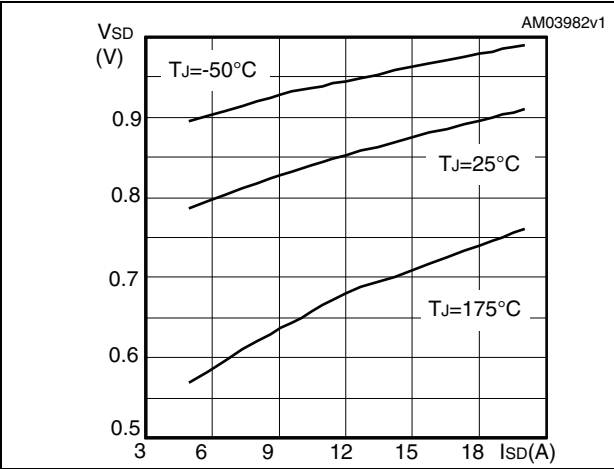


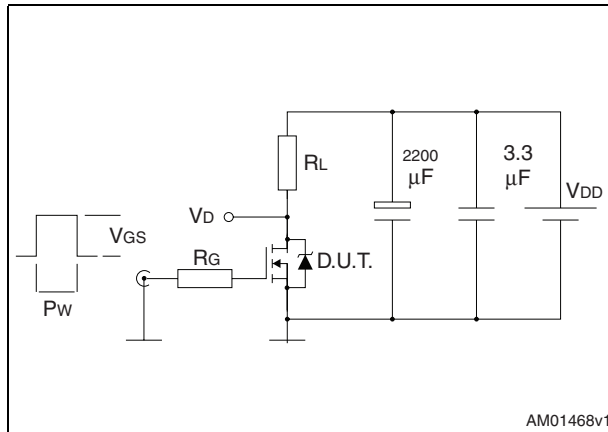
Figure 14. Source-drain diode forward characteristics



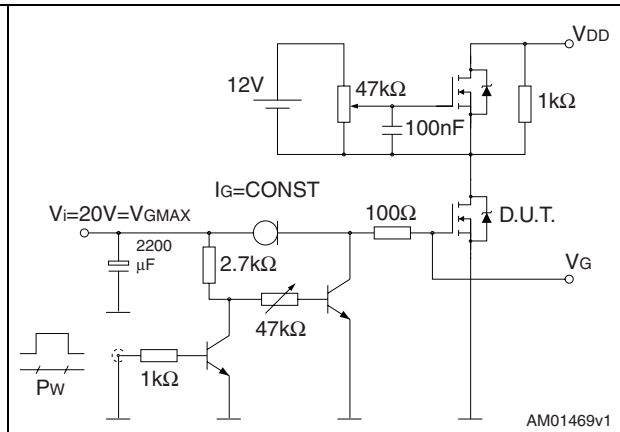


### 3 Test circuits

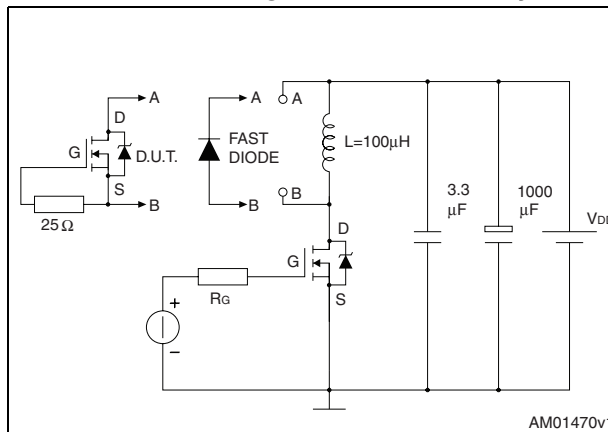
**Figure 15. Switching times test circuit for resistive load**



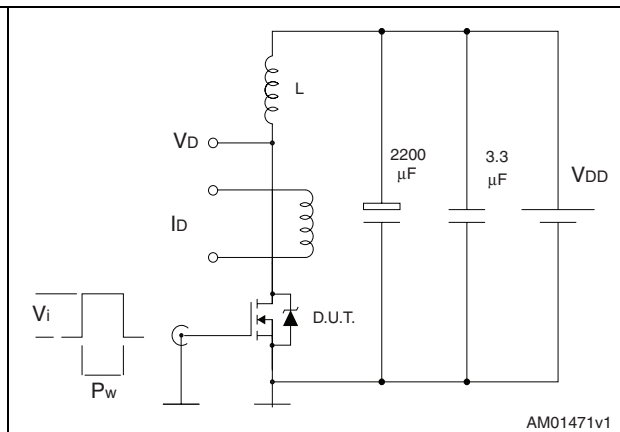
**Figure 16. Gate charge test circuit**



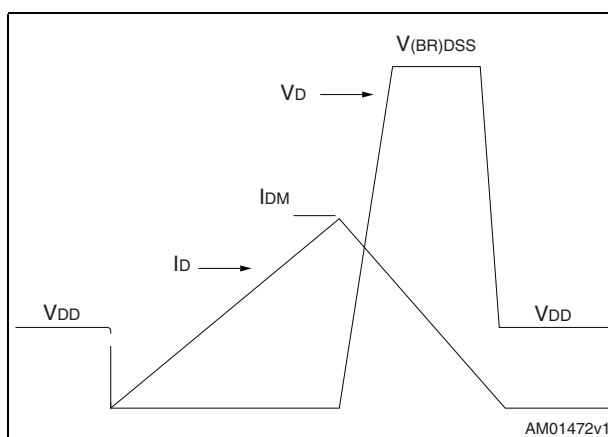
**Figure 17. Test circuit for inductive load switching and diode recovery times**



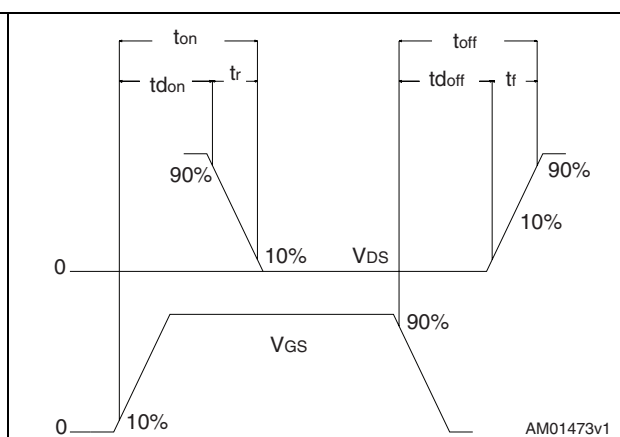
**Figure 18. Unclamped inductive load test circuit**



**Figure 19. Unclamped inductive waveform**



**Figure 20. Switching time waveform**

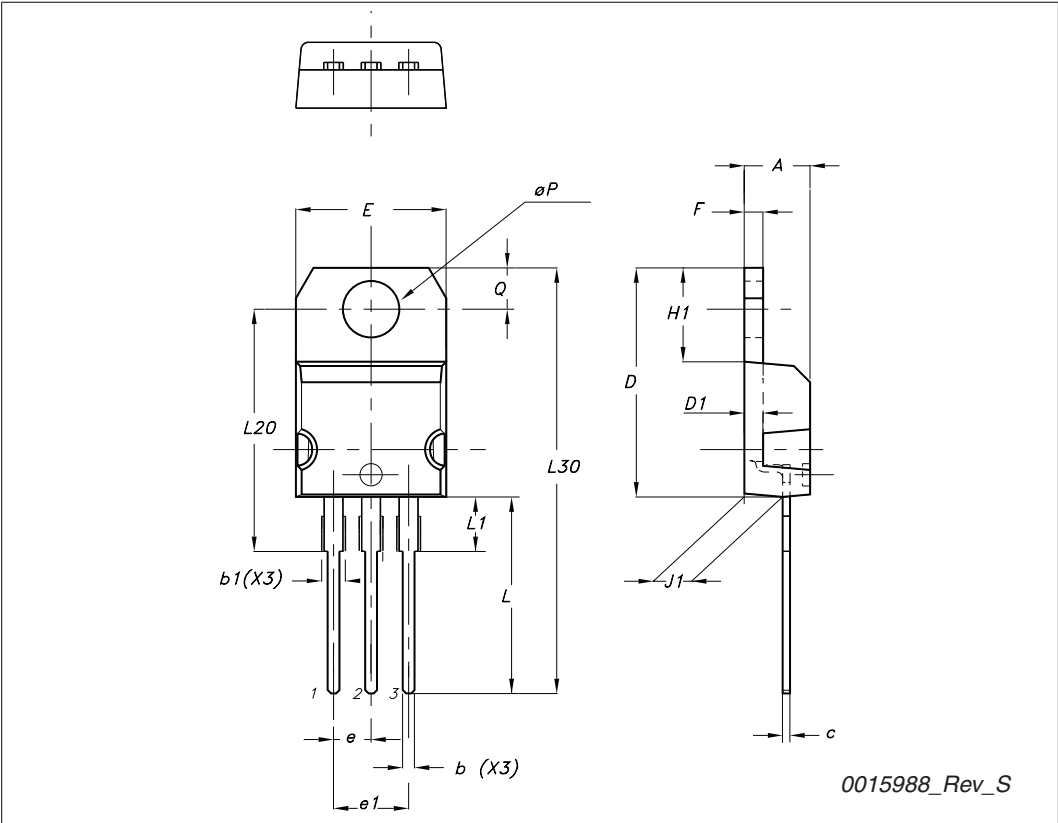


## 4 Package mechanical data

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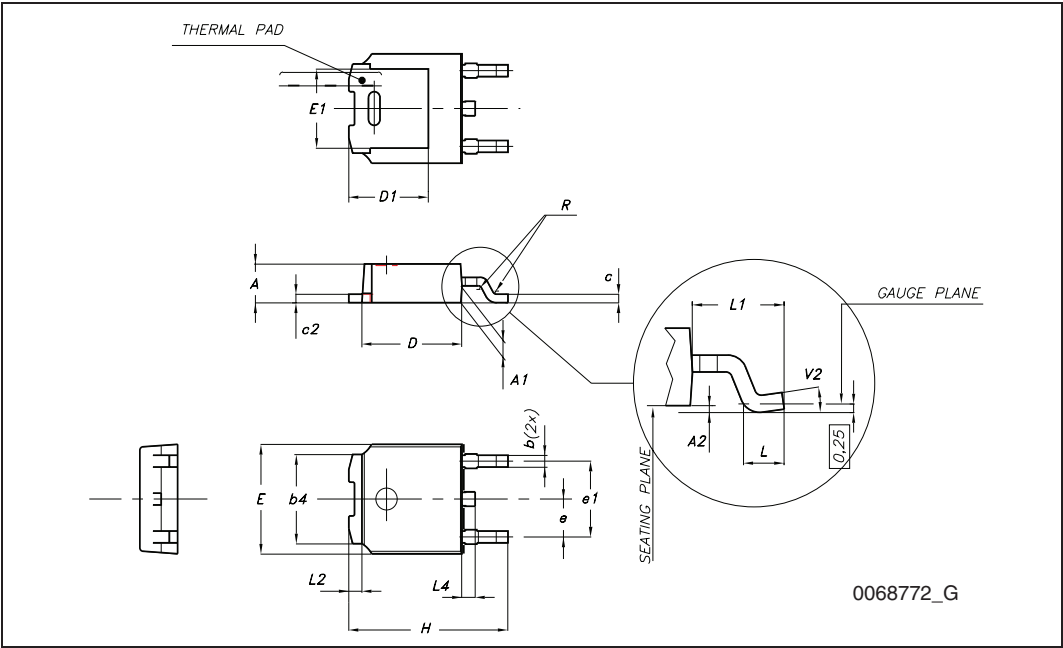
TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95



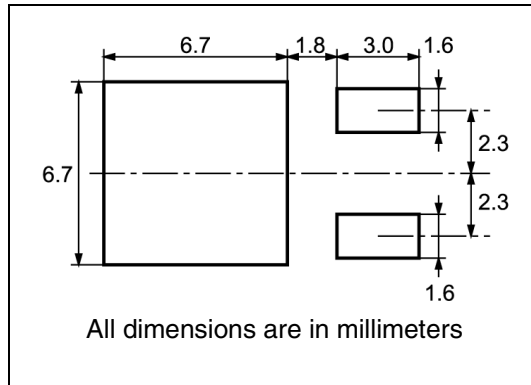
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °

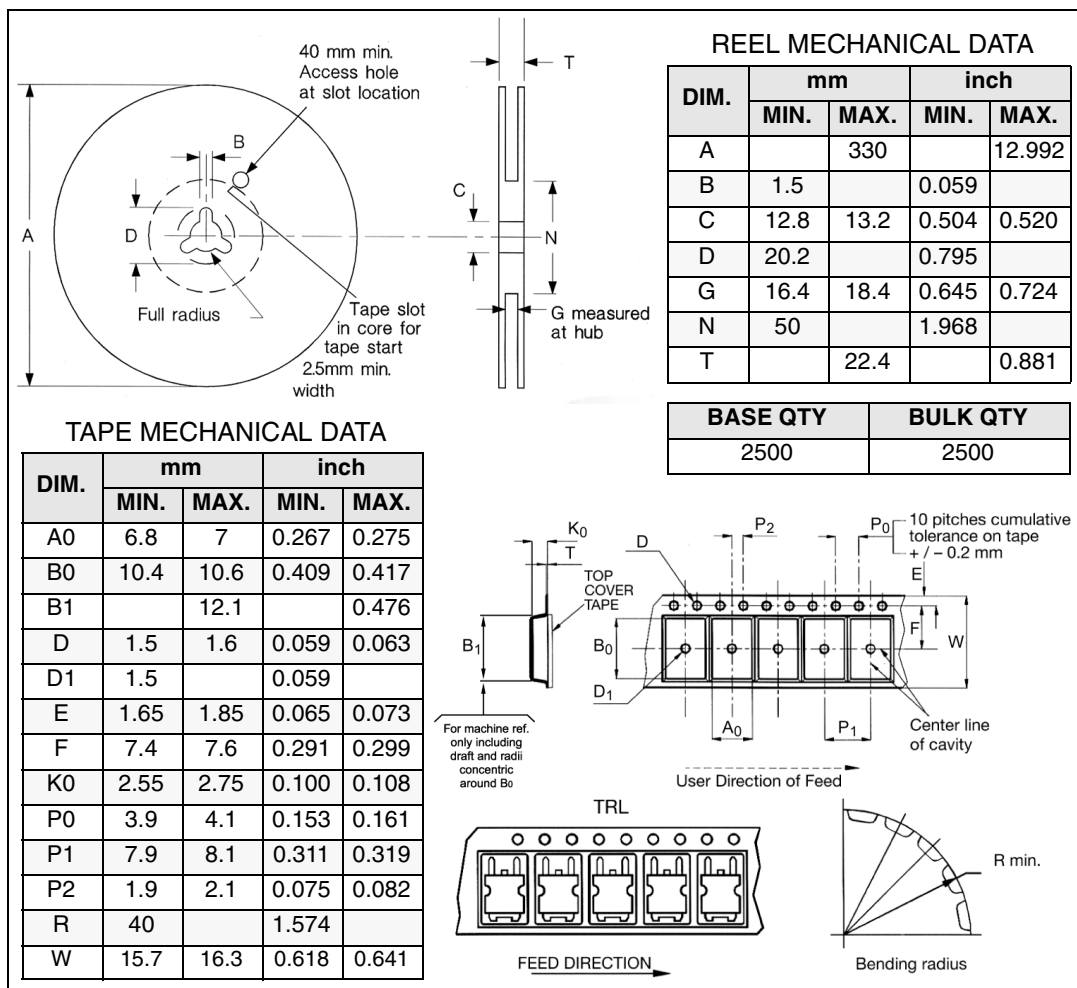


## 5 Packaging mechanical data

### DPAK FOOTPRINT



### TAPE AND REEL SHIPMENT



## 6 Revision history

**Table 8. Revision history**

Date	Revision	Changes
25-Jan-2007	1	First release
20-Mar-2007	2	Typo mistake in first page (order codes)
27-Apr-2007	3	Updates on <a href="#">Table 6: Dynamic</a>
10-Dec-2009	4	Modified device summary on first page

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