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LAB1 Report

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In this lab we were supposed to investigate the performance of a pipeline processor by calculating number of stalls due to RAW dependencies using SimpleScalar simulator. Our team carefully analyzed different potential hazards and took into account all the different scenarios and corner cases. Following are our results for the EIO trace of the cc1 benchmark:

% Performance Drop

Q1) 5-stage pipeline:
old CPI = 1 (for ideal pipeline)
new CPI = 1.6642
% Performance Drop = 100(inst_count * new CPI * T/ inst_count * old CPI * T - 1)= 66.42 % drop*
Q2) 6-stage pipeline:
old CPI = 1 (for ideal pipeline)
new CPI = 1.3903
% Performance Drop = 100(inst_count * new CPI * T/ inst_count * old CPI * T - 1)= 39.03 % drop*

Architecture	old CPI	new CPI	% Performance Drop
5-stage pipeline:	*1*	*1.6642*	*66.42 %*
6-stage pipeline:	*1*	*1.3903*	*39.03%*

% Microbenchmark Analysis

Our microbenchmark is written a form of a *for* loop which executes for 1 million times. The code was compiled using -O0 optimization flag and the *for* loop equivalent in the assembly generated was closely analyzed to identify the hazards(snippet included in *mbq1.c*). There are 8 RAW hazards that caused 2-cycle stalls and 2 RAW hazards that caused 1-cycle stalls in this microbenchmark so we expected 8 million 2-cycle stalls and 2 million 1-cycle stalls. These results matched closely with our simulation results which are 8000855 and 2000079 respectivly.