

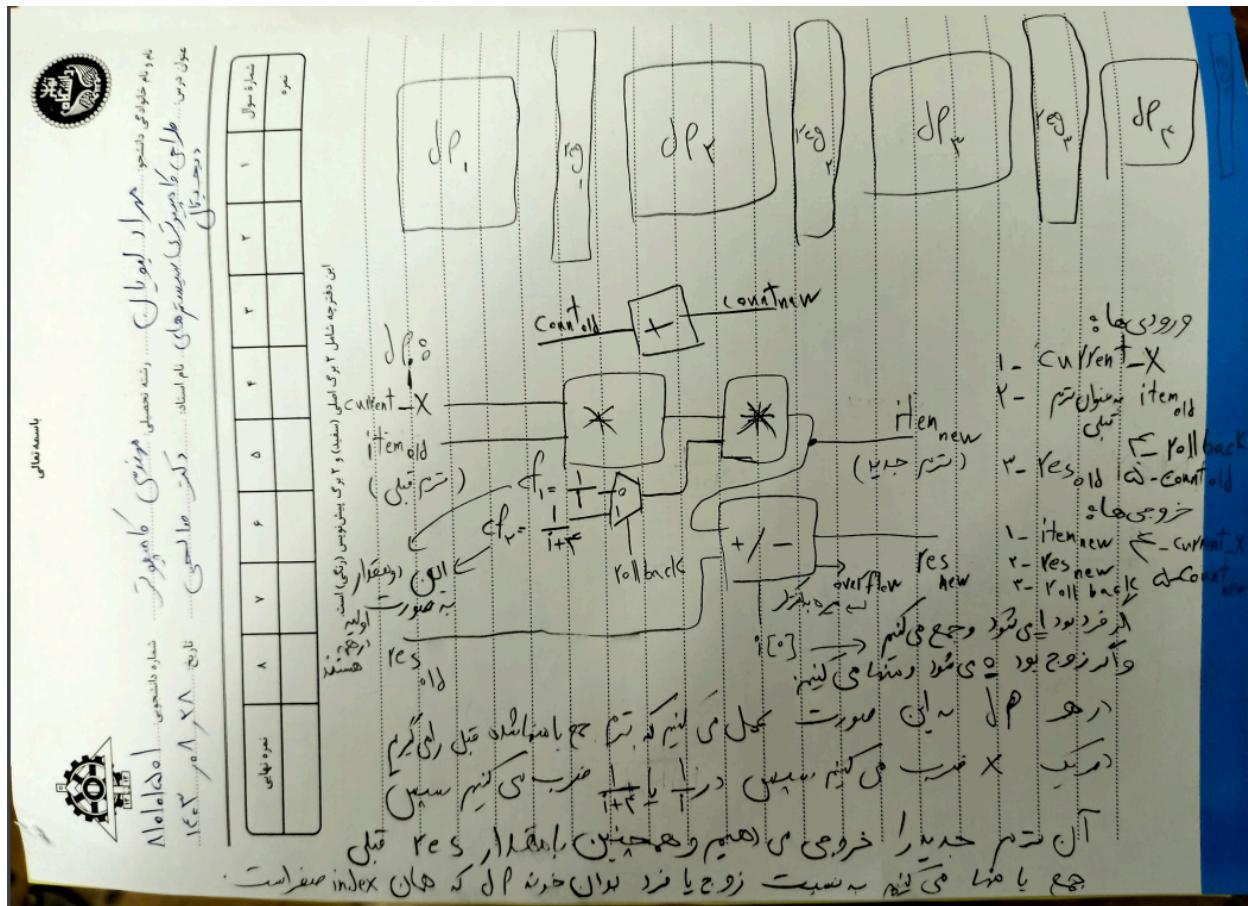
In the name of God

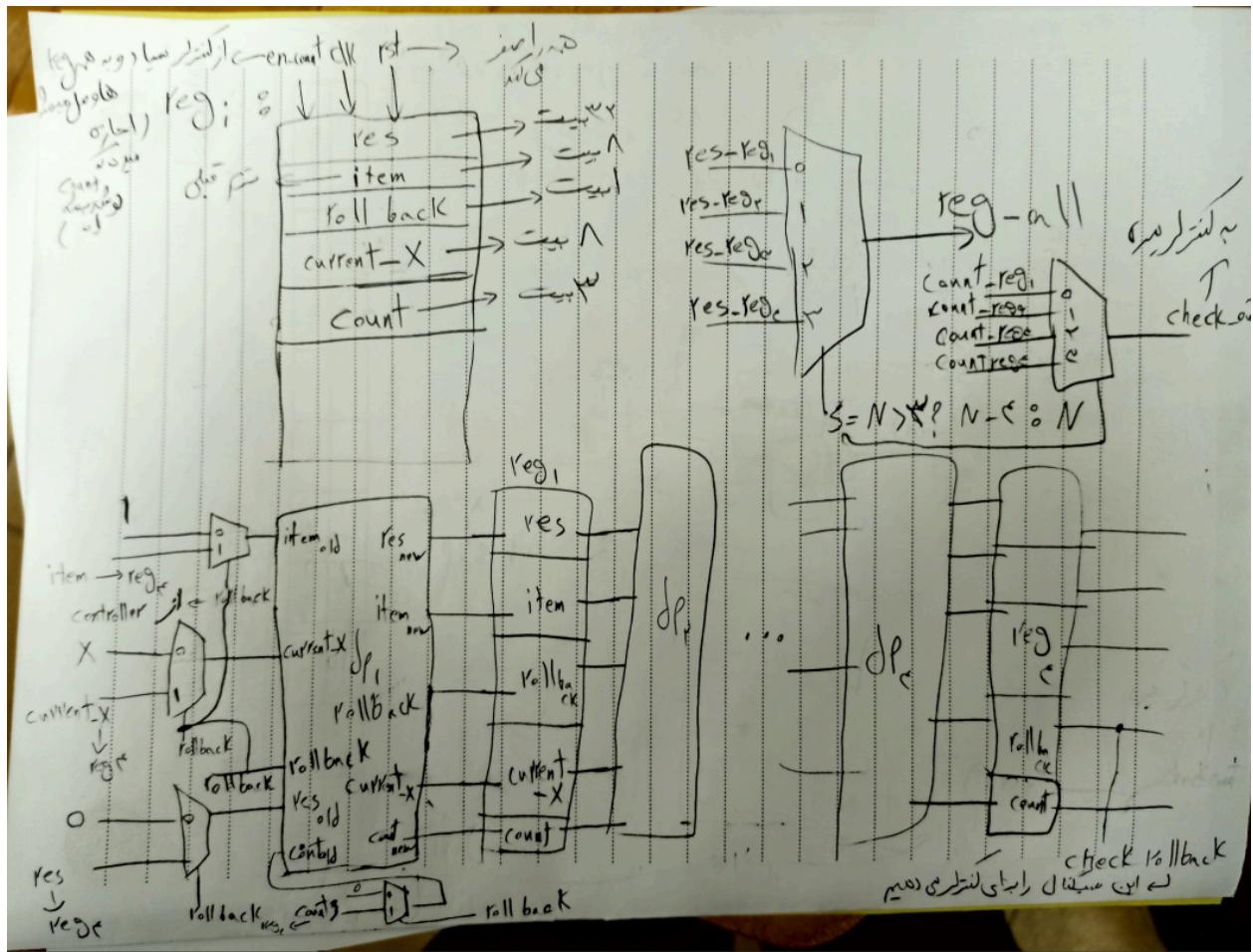
Title : project MidTerm of CAD course in UT

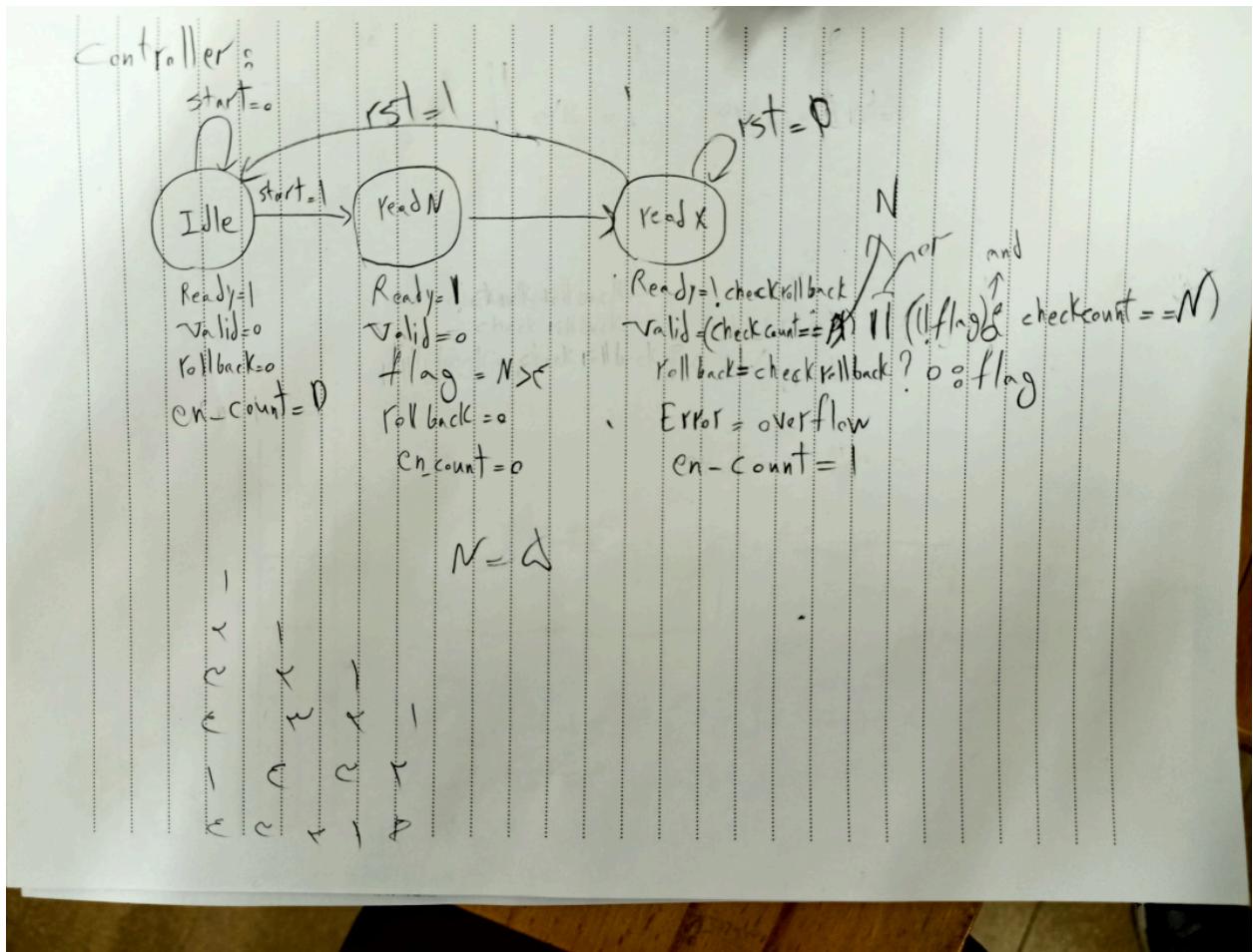
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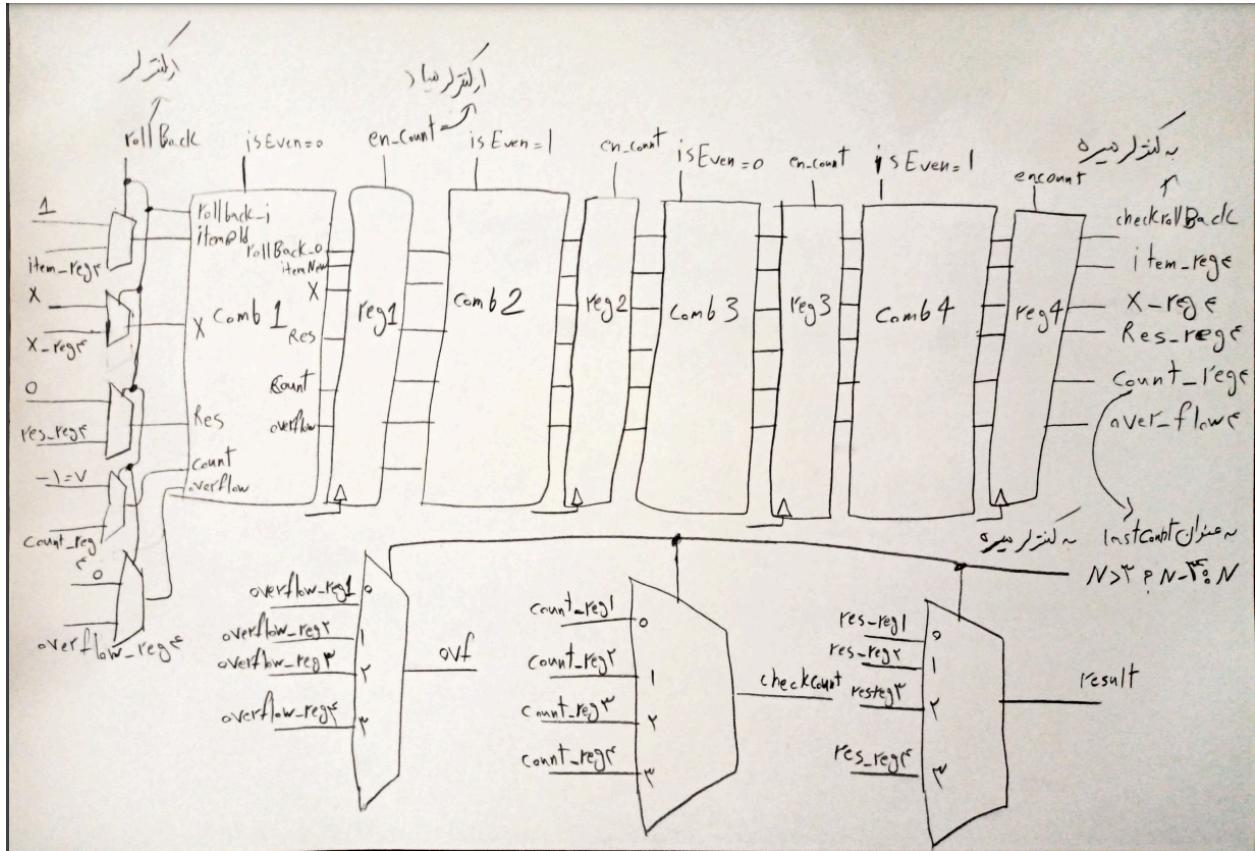
## Exam Design :

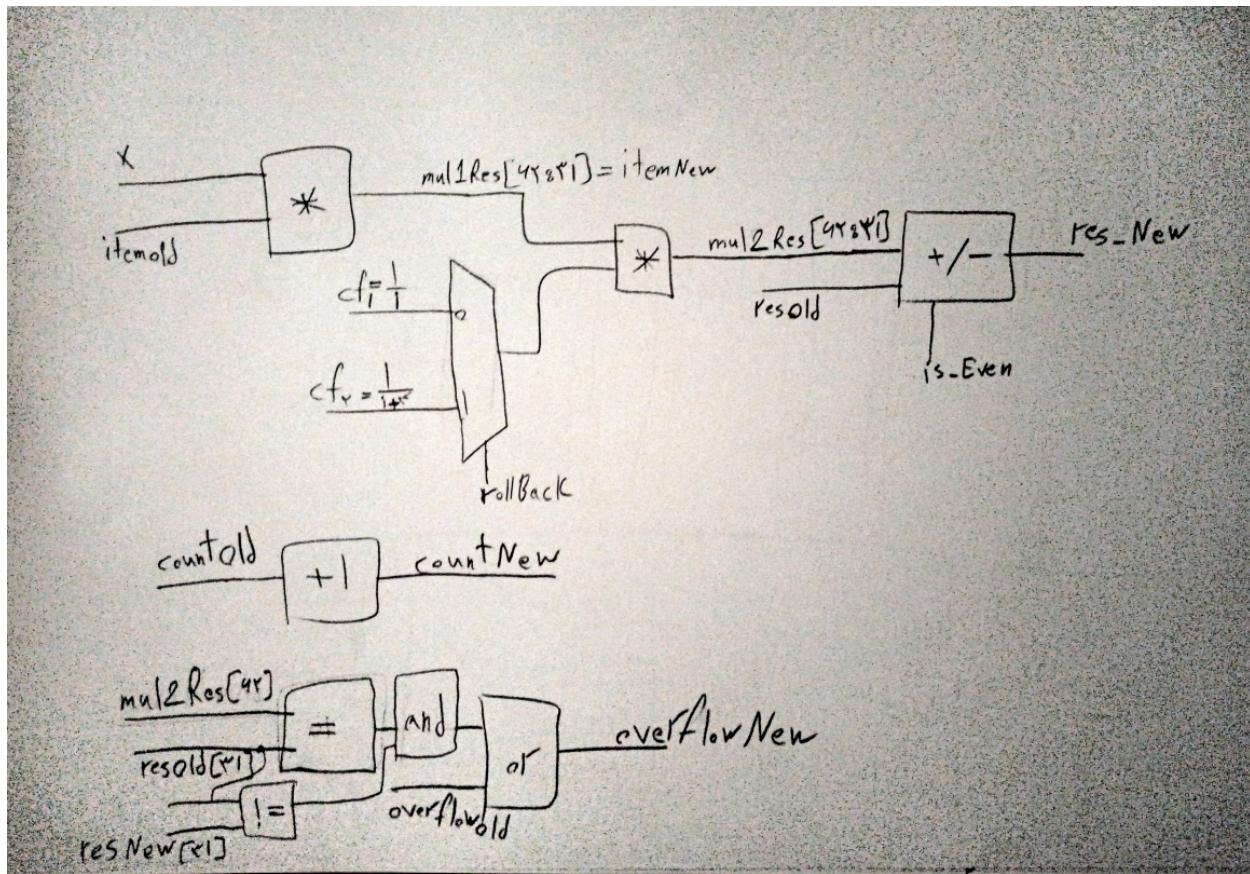


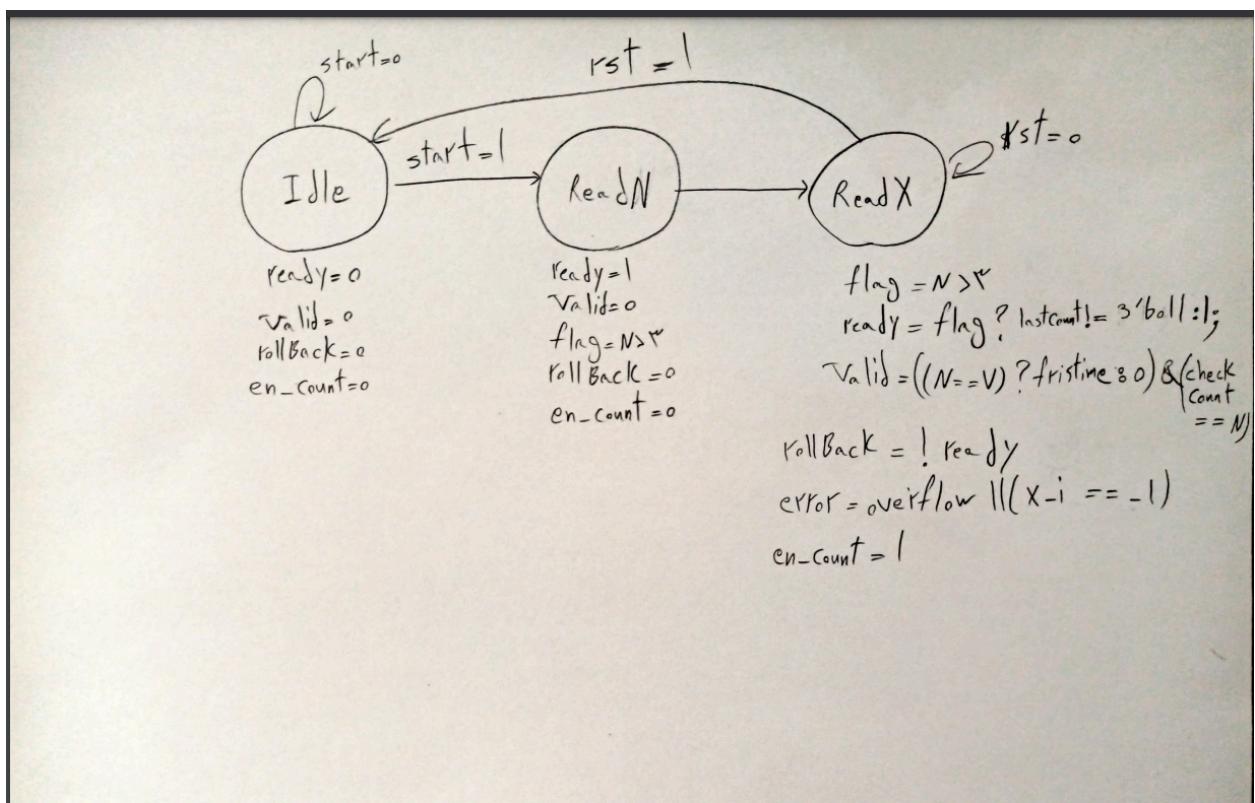
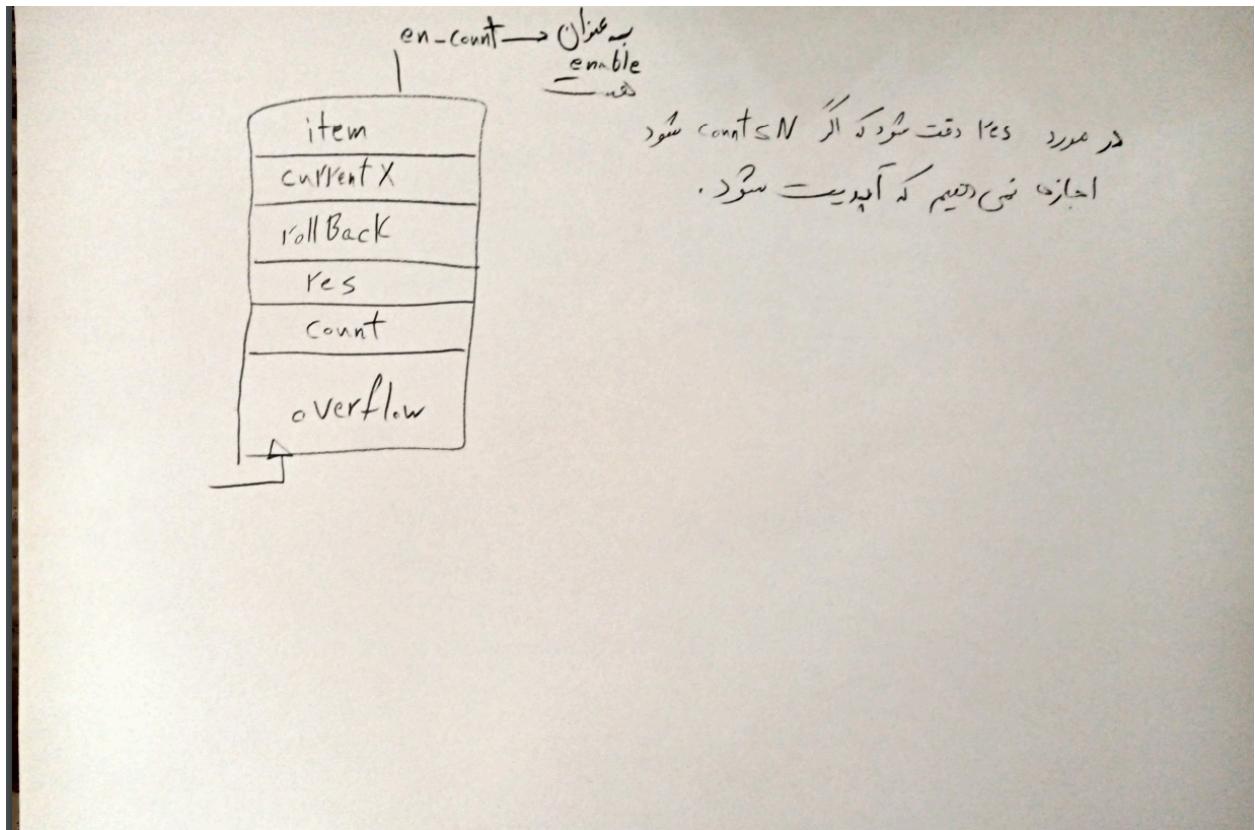




## Take Home design :







Difference :

In datapath part we add a logic for overflow in a way that the overflow in stage i is equal to :

```
overFlow_i = overFlow_i-1 or ((resOld[31] == mul2Res[62])and(resNew[31] != resOld[31]))
```

And also add an overflow register in every stage and carry it to the next part .

Also we should export the selected index stage as output and also initial it at first of every new input as 0.

In controller we add a new signal that is called first time , At first we initial the count as 7 and if we have  $N = 7$  then we see an incorrect valid as first so we define a firstTime signal that get 0 value at first and after a clock if ps is in readX state it get 1 value then after that as we see 7 on checkCount we can see valid = 1. Also the valid signal logic has changed a bit.