

# HW4 Computer Architecture

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## Assembly code:

```
add s1, zero, zero
addi s2, zero, 400
Loop: lw t1, 1024 (s2)
      lw t2, 1028 (s2)
      sub s1, t1, t2
      slt t3, s1, zero
      bne t3, zero, L1
      sub s1, zero, s1
L1:   sw s1, 1024 (s2)
      addi s2, s2, -4
      bne s2, zero, Loop
```

Changes :

- Reducing the value of s2 register to 400
- All offsets are changed to 1024

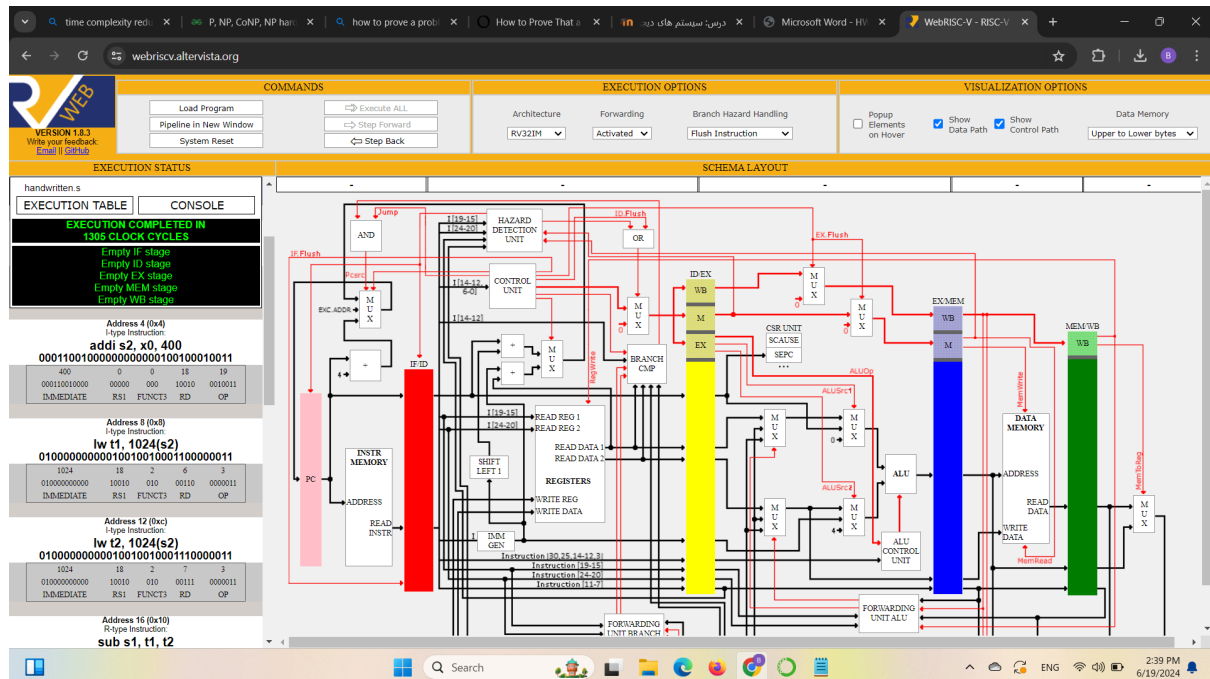
1- Deactivated Data Forwarding: The execution time is over 2000 clock cycles.

The screenshot shows the WebRISC-V simulator interface. The top bar displays the URL [web riscv.altervista.org](http://web riscv.altervista.org). The interface is divided into several panels:

- COMMANDS:** Includes buttons for Load Program, Execute ALL, Step Forward, and Step Back.
- EXECUTION OPTIONS:** Includes Architecture (RV32IM), Forwarding (Deactivate), Branch Hazard Handling (Flush Instruction), and Visualization Options (Show Data Path, Show Control Path, Data Memory).
- EXECUTION STATUS:** Shows the current cycle and the instruction being executed. The instruction is `addi s2, x0, 400` at Address 4 (0x4).
- SCHEMA LAYOUT:** Shows the execution flow graph. The text **OVER 2000 CLOCK CYCLES** is displayed in red.

The bottom of the interface shows a Windows taskbar with the date and time 2:39 PM 6/19/2024.

## 2- Data Forward Activated: The execution time is 1305 clock cycles.



Conclusion : Activating data forwarding increases the speed of operation systems and it causes them to consume less computational power.