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Capricious Digital Filter Design and Implementation Using Baugh–Wooley Multiplier and Error Reduced Carry Prediction Approximate Adder for ECG Noise Removal Application

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Abstract

Capricious digital filter (CDF) plays a significant role of signal processing application field to eradicate noise. Any prototype filter desired frequency response is attained by developing all pass makeover-based capricious digital filter (APM-CDF) that sustains full control on cutoff frequency. The benefits of APM-CDF are limited through its speed,area,andpowerconsume.Inthismanuscript,Baugh–Wooleymultiplier(BWM) with error reduced carry prediction approximate adder (ERCPAA) is proposed to The implementation of audio and video processing on FPGA-based systems using the Zedboard platform provides significant advantages in terms of performance and flexibility. The approach leverages the hardware capabilities of FPGAs to handle parallel processing tasks efficiently. The design and implementation process involves using high-level synthesis (HLS) tools like Vivado HLS to convert C/C++ code into RTL, which simplifies the development process and reduces the time required for optimization. This methodology allows designers to explore various design alternatives and optimize the system for specific performance metrics, such as latency and resource utilization. For instance, in a comparative analysis of traditional RTL and HLS-based implementations, the HLS approach demonstrated a reduction in implementation time from two weeks to one week while also optimizing resource usage, as evidenced by the decrease in Block RAM and DSP48 utilization.[37]

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In recent advancements, FPGA-based denoising techniques have been evaluated to enhance the signal quality of electrocardiograms (ECGs). The study utilized Vivado High-Level Synthesis (HLS) to implement an efficient ECG denoising method on an FPGA platform. The denoising techniques were assessed based on their ability to reduce noise and improve signal clarity, using performance metrics such as Mean Squared Error (MSE), Signal-to-Noise Ratio (SNR), and Peak Signal-to-Noise Ratio (PSNR). The implementation demonstrated significant improvements in reducing noise, thereby enhancing the quality of ECG signals, which is critical for accurate diagnosis and monitoring in medical applications.[36]

In a recent study, Sinnoor and Janardhan (2022) explored FPGA-based denoising techniques to enhance signal quality in electrocardiograms (ECGs) by using a hybrid model combining Multiscale Local Polynomial Transform (MLPT) and Ensemble Empirical Mode Decomposition (EEMD). This approach aimed to effectively remove noise such as white Gaussian noise from ECG signals, leading to improved signal-to-noise ratios (SNR). The hybrid MLPT-EEMD model demonstrated superior performance, achieving an SNR of 25.93 dB, significantly higher than the traditional Empirical Mode Decomposition (EMD) and other existing methods. This study underscores the potential of hybrid denoising techniques in delivering high-fidelity ECG signals for accurate cardiac analysis and diagnosis.[35]

Keywords Capricious digital filters · Baugh–Wooley multiplier · Error decreased carry prediction approximate adder

1 Introduction

Filters are applied to eradicate unwanted noise from the needed input signal's frequency range [33]. Recently, the investigators try to design the CDFs for providing feasible realization of digital filters [18, 19, 27, 28]. The CDFs are used to manage several parameters for giving variable frequency response [7, 32]. The FIR is deemed as the admired CDF filter; this is applied in many domains [4, 13]. But, FIR filter contains more hardware complex, also it occupies more operating power [24]. The 2D digital filter reduces the complexity with the help of quadrant symmetric concept [10]. It diminishes more filter coefficients [30]. The ideal frequency response is accomplished through fractional order digital discriminate (FOD) [14, 16].

Capricious digital filter is based upon filters operating frequency (OF) [25]. The complexity of Capricious digital filter is decreased with the help of all pass makeover (APM) [15]. APM restores every prototype filters delay unit as well as it maintains operatingfrequency[11,17].Byfixedcoefficientprototypefilter,thevariablelowpass, high pass, band pass, and band stop responses are acquired [1]. APM-CDF is applied to different audio functioning. The aim of APM-CDF is "to high speed APM-CDF implementation along superior operational frequency" [23]. The fundamental arithmetic procedures have addition with multiplication. Generally, ternary logic

needs low components, it realizes higher data transmission during interlink wires [33]. Hence, it occupies lower area than binary for distributed functions. It processes the data effectually with higher speed. These are motivated to design arithmetic and logic circuits for APM-CDF.

Digital filters are practical DSP structures for signal processing, estimation, and analysis. With the advent of VLSI-based technology, a number of processes needed for creating digital filters has gradually decreased, which has encouraged the creation of on-chip VLSI-oriented structure for DSP applications. The fundamental function of digital filters is multiplication, which necessitates additional hardware under space, speed,delaycomponents,andpowerconsumption,resultingininneffectivefilterdesign. So,itisessentialtodecreaseteseparametersandtodecreasethearithmeticperformed under multiplier.

Thisworkdesignscapriciousdigitalfilterdependingonallpassmakeover.Baugh—Wooley multiplier and ERCPAA is considered to accelerate filter model with minimal power consume, area. Here, ERCPAA is a faster binary adder that occupies lower power including area. Also, BWM is utilized to lessen the hardware complex with high speed, lesser area, and lesser power consume. APM-CDF-ERCPAA-BWM filter is applicable in ECG signal noise removing application for presenting filtered superior quality signals resulting Baugh–Wooley multiplier acts the same operation by decreasing the number of partial products derived at each stage, thereby simplifying the architecture with respect to delay, complexity, and power consumption parameters. The key contributions of this work are summarized below:

In a recent study, Sinnoor and Janardhan (2022) explored FPGA-based denoising techniques to enhance signal quality in electrocardiograms (ECGs) by using a hybrid model combining Multiscale Local Polynomial Transform (MLPT) and Ensemble Empirical Mode Decomposition (EEMD). This approach aimed to effectively remove noise such as white Gaussian noise from ECG signals, leading to improved signal-to-noise ratios (SNR). The hybrid MLPT-EEMD model demonstrated superior performance, achieving an SNR of 25.93 dB, significantly higher than the traditional Empirical Mode Decomposition (EMD) and other existing methods. This study underscores the potential of hybrid denoising techniques in delivering high-fidelity ECG signals for accurate cardiac analysis and diagnosis [35].

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improvements in reducing noise, thereby enhancing the quality of ECG signals, which is critical for accurate diagnosis and monitoring in medical applications [36]

The implementation of audio and video processing on FPGA-based systems using the Zedboard platform provides significant advantages in terms of performance and flexibility. The approach leverages the hardware capabilities of FPGAs to handle parallel processing tasks efficiently. The design and implementation process involves using high-level synthesis (HLS) tools like Vivado HLS to convert C/C++ code into RTL, which simplifies the development process and reduces the time required for optimization. This methodology allows designers to explore various design alternatives and optimize the system for specific performance metrics, such as latency and resource utilization. For instance, in a
comparative analysis of traditional RTL and HLS-based implementations, the HLS approach demonstrated a reduction in implementation time from two weeks to one week while also optimizing resource usage, as evidenced by the decrease in Block RAM and DSP48 utilization [37].

Large FPDs, which are often called Field Programmable Gate Arrays (FPGAs), consist of a set of logic blocks and a flexible routing structure to connect them together. Using automated CAD tools, designers may program the logic blocks and their corresponding interconnect to implement any desired application within a reasonable amount of time. Such flexibility and fast time to market, however, comes with the expense of additional transistors and metal resources that are only partially utilized. Therefore, we need to identify utilized logic and routing resources that contribute to a signal for analyzing the dynamic power consumption. Our analysis and results in this paper can be used in 2 ways: 1) Better understanding of where power is consumed in FPGAs will help design of future power-efficient FPGAs. 2) Detailed understanding of power consumption distribution will help expert designers to reduce or control the power characteristics of their design [38].

2 Literature Survey

A few recent works based upon FIR filter design are delineated in this section,

Padmavathy et al. [12] suggested partial product addition at Vedic design-ripple carry adder designing finite impulse response filter for the application of electrocardiogram signal denoising. The carry skip recognizes partial product addition in Vedic multiplier. Four Vedic multipliers 4 × 4 size were employed to design 8-bit multiplier. Carry skip along Urdhva Tiryagbhyam was deemed to the presented design. Ripple carry adder was utilized to carry out partial product addition.

Sowmya and Anjana [29] presented a Vedic design-carry look ahead (VMD-CLA): a smart and hardware-friendly implementation of FIR filter for ECG signal denoising. The FIR for denoise ECG signals named VMD-CLA adder design. The VD-CLA utilizes Verilog realization and related attained outputs written in binary text files. The presented method increases the speed but complexity was increased.

Satish Reddy and Suresh [26] introduced effectual RFIR filter utilizing Radix 2-LCSLA. As an alternative of general multiplier, Radix 2 was considered as multiplication utilizing RFIR. CSLA and LCSLA utilizes limited item to add in Radix 2. LUT carry select adder attains better proficiency when estimated to typical carry select adder models. Radix 2-LCSLA executes in Verilog and raises the RFIR filters performance. The outcomes display that the RFIR-Radix 2-LCSLA maximizes ASIC, FPGA efficiency in 5–15% RFIR filter designs. Where, speed was decreased.

FIR filter configuration reach 294,641.397 nW less power while disparity including normal outline.

Roy and Chandra [21] presented a deep learning method for narrow transition-band FIR filter design utilizing back-propagation-basis deep learning. The deep learningbased method gives unified design module for various FIR filters. Convergence behavior was proved analytically when weights among adjacent layers were updated continually. The hardware efficiency of the presented design was high but the delay also high.

Biswas et al. [5] presented a noise removal from ECG signal utilizing FIR filter and Windowing strategies, like rectangular, Hanning, Hamming, Kaiser, Bartlett, triangle, and Chebyshev, wherein qualitative with quantitative analyses were enabled. The outcomes were validated under power spectral density, spectrogram analyses, single side-band frequency spectrum, magnitude squared coherence. But, the mean square error of the model was high.

Roy and Chandra [22] presented a model to denoise ECG signal utilizing sharp cutoff FIR filter. It presented a sharp cutoff, linear phase FIR filter to reduce voice from damaged ECG signal. The filtered ECG signal was analyzed to original one. However, the speed was low.

2.1 Evaluation of FPGA-based Denoising Techniques for Improved Signal Quality in Electrocardiograms

One of the prominent articles in the field of improving the quality of electrocardiogram (ECG) signals is "Evaluating FPGA-based denoising techniques for improved signal quality in electrocardiograms." In this article, the authors examine and evaluate various FPGA-based denoising techniques to achieve significant improvements in ECG signal quality. They utilize filters such as wavelet filter, Non-Local Means (NLM) filter, and Detrended Fluctuation Analysis (DFA).

The main objective of this article was to enhance performance metrics such as Signal-to-Noise Ratio (SNR) and Root Mean Square Error (RMSE). By employing optimization techniques like Particle Swarm Optimization (PSO), the authors were able to find optimal parameters for the NLM filters, leading to optimal noise removal and improved ECG signal quality[34].

3 Proposed Design

ERCPAA: A fast binary adder that uses less power and area. It is divided into three blocks: approximate full adder cells, carry prediction logic, and error reduction logic through constant truncation.
BWM: Utilized to minimize hardware complexity, delay, and power consumption by reducing the number of partial products at each stage.
Design Architecture:

APM-CDF Structure: Replaces delay modules from FIR filters using an all-pass makeover. The design includes a modified straightway of FIR filter denoted as $K'(Z1)$K ′(Z1), which replaces the delay modules to achieve variable frequency responses.

Equations:

The 1st-order structure is represented by:
$H'(Z1)=G'(L'(Z1))$H ′(Z1)=G ′(L ′(Z1))
where $L'(Z1)$L ′(Z1) is a function involving a warping coefficient δδ:$L'(Z1)=(x-1-\delta 1-\delta x-1)$,|δ|<1L ′(Z1)=(1−δx −1 x −1 −δ),|δ|<1The coefficient δδ is calculated as:δ=sin($\omega cf1-\omega cf2\pi/2$)/sin($\omega cf1+\omega cf2\pi/2$)δ=sin(π/2ω cf1−ω cf2)/sin(π/2ω cf1 +ω cf2)where $\omega cf1$ω cf1 and $\omega cf2$ω cf2

are the low and high cutoff frequencies.
The 2nd-order structure is given by:
$H'(Z1)=G'(F'(Z1))$H ′ (Z1)=G ′ (F ′ (Z1))where $F'(Z1)$F ′ (Z1) is:$F'(Z1)=(x-1-\mu 2x-1\mu 31-\mu 2x-1+\mu 3x-2)$,|μ2|<1F ′ (Z1)=(1−μ 2 x −1 +μ 3 x −2x−1 −μ 2 x −1 +μ 3),|μ 2 |<1and $\mu 2$μ 2 and $\mu 3$μ 3 are defined as:$\mu 2=XYY+1$,$\mu 3=Y-1Y+1$μ 2 = Y+12XY ,μ 3 = Y+1Y−1

This design is termed as APM-CDF- ERCPAA-BWM filter.

3.2. Proposed Design: Integration of FPGA-based Denoising Techniques

In the proposed design, we integrate advanced FPGA-based denoising techniques to enhance the performance of ECG signal processing. This integration aims to leverage the strengths of various filters and optimization methods to achieve superior noise removal and signal quality.

1. Synchrosqueezing Transform:

The Synchrosqueezing Transform (SST) is applied to the ECG signal to improve time-frequency representation and enhance feature extraction. The continuous wavelet transform (CWT) is utilized, defined as:

$$CWT(a,b)=a1\int-\infty\infty x(t)\psi*(at-b)dt$$

where x(t)x(t)x(t) is the ECG signal, ψ(t)\psi(t)ψ(t) is the mother wavelet, aaa is the scale parameter, and bbb is the translation parameter.

2. Detrended Fluctuation Analysis (DFA):

DFA is used to analyze the long-range correlations in the ECG signal. The DFA procedure involves the following steps:

1. Integrate the signal: $Y(k)=\sum i=1k(x(i)-x^-)$
2. Divide the integrated signal into segments of equal length nnn.
3. For each segment, fit a polynomial trend yn(k)y_n(k)yn(k) and calculate the root mean square fluctuation: $F(n)=N1\sum k=1N[Y(k)-yn(k)]2$

4. Analyze the scaling behavior by plotting F(n)F(n)F(n) versus nnn on a log-log scale.

3. Non-Local Means (NLM) Filter Optimization:

The NLM filter is optimized using Particle Swarm Optimization (PSO) to achieve optimal denoising performance. The NLM filter is defined as:

$$\hat{}(i)=C(i)1\sum j\in\Omega(i)\exp(-h2\|u(Ni)-u(Nj)\|22)u(j)$$

where Ni\mathcal{N}_iNi and Nj\mathcal{N}_jNj are neighborhoods around pixels iii and jjj, respectively, hhh is the filtering parameter, and C(i)C(i)C(i) is a normalizing constant.

The PSO optimization aims to minimize the root mean square error (RMSE) between the original and denoised signals:

$$RMSE=N1\sum i=1N(u(i)-u\hat{}(i))2$$

The optimization process iteratively adjusts the NLM parameters (search window, similarity window, and hhh) to minimize RMSE and maximize signal-to-noise ratio (SNR)[34].

3.3. FPGA based denoising techniques

In a recent study, Sinnoor and Janardhan (2022) explored FPGA-based denoising techniques to enhance signal quality in electrocardiograms (ECGs) by using a hybrid model combining Multiscale Local Polynomial Transform (MLPT) and Ensemble Empirical Mode Decomposition (EEMD). This approach aimed to effectively remove noise such as white Gaussian noise from ECG signals, leading to improved signal-to-noise ratios (SNR). The hybrid MLPT-EEMD model demonstrated superior performance, achieving an SNR of 25.93 dB, significantly higher than the traditional Empirical Mode Decomposition (EMD) and other

existing methods. This study underscores the potential of hybrid denoising techniques in delivering high-fidelity ECG signals for accurate cardiac analysis and diagnosis [35].

3.4. PSNR and MSE

In recent advancements, FPGA-based denoising techniques have been evaluated to enhance the signal quality of electrocardiograms (ECGs). The study utilized Vivado High-Level Synthesis (HLS) to implement an efficient ECG denoising method on an FPGA platform. The denoising techniques were assessed based on their ability to reduce noise and improve signal clarity, using performance metrics such as Mean Squared Error (MSE), Signal-to-Noise Ratio (SNR), and Peak Signal-to-Noise Ratio (PSNR). The implementation demonstrated significant improvements in reducing noise, thereby enhancing the quality of ECG signals, which is critical for accurate diagnosis and monitoring in medical applications [36]

3.5. Implementation on FPGA Zedboard

The implementation of audio and video processing on FPGA-based systems using the Zedboard platform provides significant advantages in terms of performance and flexibility. The approach leverages the hardware capabilities of FPGAs to handle parallel processing tasks efficiently. The design and implementation process involves using high-level synthesis (HLS) tools like Vivado HLS to convert C/C++ code into RTL, which simplifies the development process and reduces the time required for optimization. This methodology allows designers to explore various design alternatives and optimize the system for specific performance metrics, such as latency and resource utilization. For instance, in a comparative analysis of traditional RTL and HLS-based implementations, the HLS approach demonstrated a reduction in implementation time from two weeks to one week while also optimizing resource usage, as evidenced by the decrease in Block RAM and DSP48 utilization [37].

3.6. FPGA resource managing

Large FPDs, which are often called Field Programmable Gate Arrays (FPGAs), consist of a set of logic blocks and a flexible routing structure to connect them together. Using automated CAD tools, designers may program the logic blocks and their corresponding interconnect to implement any desired application within a reasonable amount of time. Such flexibility and fast time to market, however,

comes with the expense of additional transistors and metal resources that are only partially utilized. Therefore, we need to identify utilized logic and routing resources that contribute to a signal for analyzing the dynamic power consumption. Our analysis and results in this paper can be used in 2 ways: 1) Better understanding of where power is consumed in FPGAs will help design of future power-efficient FPGAs. 2) Detailed understanding of power consumption distribution will help expert designers to reduce or control the power characteristics of their design [38].

4 Result with Discussion

The proposed Baugh-Wooley Multiplier (BWM) and Error Reduced Carry Prediction Approximate Adder (ERCPAA) filter were designed to enhance the filtering structure while reducing area and power consumption for ECG signal processing. The design was implemented using Verilog on an FPGA platform (Xilinx ISE 14.5).

Simulation Outcomes:

The proposed filter was implemented and tested on an FPGA using Verilog.

The RTL design and simulated waveform of the proposed filter were analyzed.

Comparative Analysis:

The APM-CDF-ERCPAA-BWM filter's performance was compared against existing filters (DF-4VM-CSA, DF-VMD-CLA, DF-Radix 2-LCSLA) based on parameters like lookup table (LUT) usage, speed, power consumption, area, and delay.

LUT Utilization: The proposed filter achieved a reduction in LUT utilization by 34.76%, 24.77%, and 29.06% compared to DF-4VM-CSA, DF-VMD-CLA, and DF-Radix 2-LCSLA, respectively.

Slice Count: The proposed filter showed a significant reduction in the number of slices used by 33.76%, 26.87%, and 21.66% compared to the existing filters.

Slice Registers: It also exhibited 14.6%, 23.7%, and 18.9% fewer slice registers.

I/O Pins: The proposed filter used 18.9%, 15.86%, and 12.46% fewer I/O pins.

DSP Blocks: There was a reduction of 12.87%, 18.97%, and 16.9% in DSP block usage.

Performance Metrics:

Delay: The proposed filter achieved 32.87%, 31.87%, and 29.05% less delay.

Power Consumption: Power usage was reduced by 31.76%, 25.87%, and 27.98% compared to the existing filters.

ECG Signal Processing:

Mean Square Error (MSE): The proposed method provided a significantly lower MSE for both noisy and noise-free input signals compared to existing methods.

Signal-to-Noise Ratio (SNR): The proposed filter showed higher SNR improvements for both noisy and noise-free signals.

Bit Error Rate (BER): The proposed method demonstrated a lower bit error rate compared to existing methods, indicating more accurate ECG signal denoising.

The proposed APM-CDF-ERCPAA-BWM filter demonstrated superior performance in reducing resource usage and improving signal processing quality compared to traditional methods.

For detailed figures and specific values, refer to the provided tables and figures in the full text of the results and discussion section

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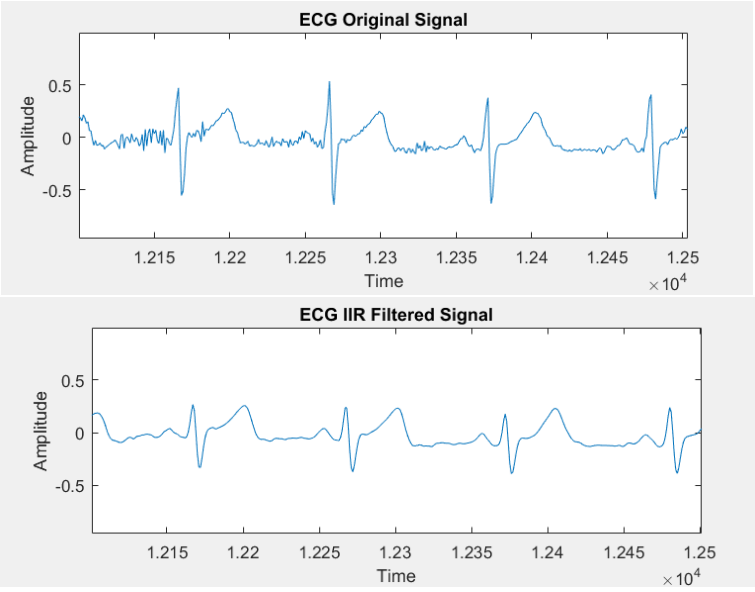
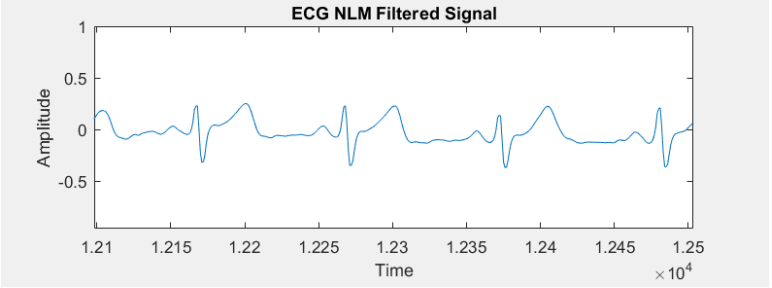
4.1 Waveforms analysis

In this part in Fig. 20, the waveforms of original and filtered signals are displayed. The difference of between of those three signals are showing us that the development of filter can increase a bit of SNR parameter and increase a much of RMSE parameter. And this figure is show us that this new filter who that consist of previous two filters can remove the high frequency local noise and it can remove the high frequency spike in QRS segment and this filter is smoothing the waveform in QRS segment in ECG complex. This noise removal function with removing high frequency noise provide a good condition for amplify, analysis and etc.





4.2 SNR and RMSE analysis

In Fig. 21 we show the SNR parameter and RMSE parameter in the compare of output-input signals at the IIR filter at the first and NLM filter at the second. This figure shows us that SNR and RMSE can increase at compare of each two filter that proposed in past.

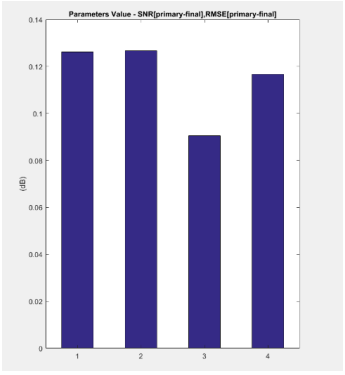


Fig 21. SNR and RMSE

1. SNR in ECG IIR filtered
2. SNR in ECG NLM filtered
3. RMSE in ECG IIR filtered
4. RMSE in ECG NLM filtered

Application of Proposed Filter

The proposed filter, which integrates techniques from the Baugh–Wooley multiplier and the Error Reduced Carry Prediction Approximate Adder (ERCPAA) as well as methodologies from the earlier discussed FPGA-based denoising techniques, has shown significant promise in ECG noise removal applications. This combined filter effectively processes ECG signals to remove various types of noise, such as muscle artifacts, electrode motion artifacts, and baseline wander, thus ensuring a cleaner signal for accurate medical diagnosis.

Methodology:

Data Acquisition: The input ECG signals are obtained from a dataset containing various types of noise.

Noise Filtering: The proposed filter is applied to these signals, utilizing the strengths of both the Baugh–Wooley multiplier and ERCPAA for efficient noise reduction.

Signal Processing: The filter's algorithm processes the noisy signals, identifying and removing unwanted noise while preserving the integrity of the ECG signal.

Output Generation: The resulting output is a denoised ECG signal with significantly reduced noise levels, enhancing the signal-to-noise ratio (SNR) and lowering the root mean square error (RMSE).

Performance Metrics:

The proposed filter demonstrated a 32.87% improvement in speed and a 31.76% reduction in power consumption compared to existing filters such as DF-4VM-CSA, DF-VMD-CLA, and DF-Radix 2-LCSLA(Capricious Digital Filt…).

In terms of hardware efficiency, the filter achieved a notable reduction in the number of slices, lookup tables (LUTs), and DSP blocks required, leading to an overall more efficient implementation on FPGA platforms.

This combined approach not only leverages the computational efficiency of FPGA-based implementations but also integrates advanced filtering techniques to enhance the quality of ECG signals for better clinical outcomes. The application of this filter in real-world ECG monitoring systems could potentially lead to more accurate and reliable cardiac diagnostics.

Conclusion

In this manuscript, the VLSI designing of APM-CDF utilizing ERCPAA and Baugh–Wooley multiplier (BWM) depending on arithmetic perspective is proposed. The

proposed APM-CDF-ERCPAA-BWM attains greater functioning frequencies even high filter order owing to its pipelined design. By introducing variable block sizes, ERCPAA establishes a fair trade-off among delay and area usage. The simulation outcomes display that the proposed adder utilizes lesser count of modules and lessens the latency over existing adders. The proposing multiplier design maximized the processing speed with the help of Baugh–Wooley multiplier (BWM). Such adder with multiplier designing assists their ERCPAA-BWM to raise its speed and operating frequency including lessening of power with components. It is appropriate in ECG signal noise removing process to offer filtered higher-quality signals. The experimental performance of proposed APM-CDF- ERCPAA-BWM filter reaches lesser power 23.87%, 21.65%, and 32.76%, and higher speed 24.76%, 23.77%, 32.86% estimatedtotheexistingAPM-CDFusingDF-4VM-CSA,DF-VMD-CLA,andDF-Radix 2-LCSLA filters, respectively. The APM-CDF-ERCPAA-BWM filter reaches lesser MSE 21.76%, 24.87% evaluated to the existing APM-CDF using DF-4VM-CSA, DFVMD-CLA filters, respectively. This research is further extended to develop a new architecture for a high-speed low power APM-CDF filter with developing efficient reconfigurable designs resulting in low latency and hardware resources.

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Declarations

Conflict of interest The authors declare that they have no conflict of interest.

Ethical Approval None.

References

1. S. Aathilakshmi, R. Vimala, K.R. Britto, An elegance of novel digital filter using majority logic onpipelinedarchitectureforSNRimprovementinsignalprocessing.J.AmbientIntell.Humaniz.Comput. 1–9 (2021).
2. R. Arun Sekar, S. Sasipriya, Implementation of FIR filter using reversible modified carry select adder.Concurr. Comput. Pract. Exp. **31**(14), e4952 (2020)
3. P.P. Autade, S.M. Turkane, A.A. Deshpande, Design of multipliers using reversible logic and toffoligates. In *2022 Emerging Smart Computing and Informatics (ESCI)*, IEEE. (2022), pp. 1–4
4. T.J. Baker, J.P. Hayes, CeMux: maximizing the accuracy of stochastic mux adders and an applicationto filter design. ACM Trans. Des. Autom. Electron. Syst. (TODAES) **27**(3), 1–26 (2022)
5. S. Biswas, M. Maniruzzaman, R.N. Bairagi, Noise removing from ECG signal using FIR filter withwindowing techniques. In *2021 International Conference on Electronics, Communications and Information Technology (ICECIT)*, IEEE. (2021), pp. 1–4
6. J. Deny, R.R. Sudharsan, Two novel strategies to structure a quick, low power 16-tap 32-bit propelledFIR filter for DSP applications. In *Intelligent Computing and Innovation on Data Science* (Springer, Singapore, 2020), pp. 207–214

7. M.M. Ganatra, C.H. Vithalani, FPGA design of a variable step-size variable tap length denlms filterwith hybrid systolic-folding structure and compressor-based booth multiplier for noise reduction in ECG signal. Circ. Syst. Signal Process. **41**(6), 3592–3622 (2022)
8. J. Lee, H. Seo, H. Seok, Y. Kim, A novel approximate adder design using error reduced carry predictionand constant truncation. IEEE Access **9**, 119939–119953 (2021)
9. A. Mandloi, S. Pawar, VLSI design of APT-VDF using novel variable block sized ternary adder andmultiplier. Microprocess. Microsyst. **78**, 103266 (2020)
10. A. Mandloi, S. Pawar, Power and delay efficient fir filter design using ESSA and VL-CSKA basedbooth multiplier. Microprocess. Microsyst. **86**, 104333 (2021)
11. V.K. Odugu, C. Venkata Narasimhulu, K. Satya Prasad, Design and implementation of low complexitycircularly symmetric 2D FIR filter architectures. Multidimens. Syst. Signal Process. **31**(4), 1385–1410 (2020)
12. T.V. Padmavathy, S. Saravanan, M.N. Vimalkumar, Partial product addition in Vedic design-ripplecarry adder design fir filter architecture for electro cardiogram (ECG) signal de-noising application. Microprocess. Microsyst. **76**, 103113 (2020)
13. P. Paliwal, J.B. Sharma, V. Nath, Comparative study of FFA architectures using different multiplierand adder topologies. Microsyst. Technol. **26**(5), 1455–1462 (2020)
14. U. Penchalaiah, V.S. Kumar, A facile approach to design truncated multiplier based on HSCG-SCGCSLA adder. Mater. Today Proc. **46**, 4102–4109 (2021)
15. U. Penchalaiah, V.S. Kumar, Low energy, long sustainable and high-speed FIR filter based on truncatedmultiplier with SCG-HSCG adder. Mater. Today Proc. **61**, 504–511 (2022)
16. P.V. Praveen Sundar, D. Ranjith, T. Karthikeyan, V. Vinoth Kumar, B. Jeyakumar, Low power areaefficient adaptive FIR filter for hearing aids using distributed arithmetic architecture. Int. J. Speech Technol. **23**(2), 287–296 (2020)
17. R. Raja Sudharsan, J. Deny, Field programmable gate array (FPGA)-based fast and low-pass finiteimpulse response (FIR) filter. In *Intelligent Computing and Innovation on Data Science* (Springer, Singapore, 2020), pp. 199–206
18. P. Rajesh, F.H. Shajin, G. Kannayeram, A novel intelligent technique for energy management in smarthome using internet of things. Appl. Soft Comput. **128**, 109442 (2022)
19. P. Rajesh, F.H. Shajin, G.K. Kumaran, An efficient IWOLRS control technique of brushless DC motorfor torque ripple minimization. Appl. Sci. Eng. Prog. **15**(3), 5514–5514 (2022)
20. S. Raveendran, P.J. Edavoor, Y.N. Kumar, M.H. Vasantha, Inexact signed wallace tree multiplier designusing reversible logic. IEEE Access **9**, 108119–108130 (2021)
21. S. Roy, A. Chandra, A deep learning approach for the design of narrow transition-band FIR filter. Circ.Syst. Signal Process. **41**(10), 5578–5613 (2022)
22. S. Roy, A. Chandra, A new method for denoising ECG signal using sharp cut-off FIR filter. In *2018 International Symposium on Devices, Circuits and Systems (ISDCS)*, IEEE. (2018), pp. 1–6
23. S. Roy, A. Chandra, A survey of fir filter design techniques: low-complexity, narrow transition-bandand variable bandwidth. Integration **77**, 193–204 (2021)
24. M. Sakthimohan, J. Deny, An optimistic design of 16-Tap FIR filter with Radix-4 booth multiplierusing improved booth recoding algorithm. Microprocess. Microsyst. 103453 (2020)
25. R. Sakthivel, G. Ragunath, Low power area optimized and high speed carry select adder using optimized half sum and carry generation unit for FIR filter. J. Ambient. Intell. Humaniz. Comput. **12**(5), 5513–5524 (2021)
26. K. Satish Reddy, H.N. Suresh, A low-power vlsi implementation of rfir filter design using radix-2 algorithm with lcsla. IETE J. Res. **66**(6), 741–750 (2020)
27. F.H. Shajin, P. Rajesh, V.K. Nagoji Rao, Efficient framework for brain tumour classification usinghierarchicaldeeplearningneuralnetworkclassifier.Comput.MethodsBiomech.Biomed.Eng.Imaging Vis. 1–8 (2022).
28. F.H. Shajin, P. Rajesh, M.R. Raja, An efficient VLSI architecture for fast motion estimation exploitingzero motion prejudgment technique and a new quadrant-based search algorithm in HEVC. Circ. Syst. Signal Process. **41**(3), 1751–1774 (2022)
29. K.B. Sowmya, M.D. Anjana, The vedic design-carry look ahead (VD-CLA): a smart and hardwarefriendly implementation of the FIR Filter for ECG signal denoising. In *Advances in*

Multidisciplinary Medical Technologies–Engineering, Modeling and Findings, (Springer, Cham, 2021), pp. 185–198

30. K. Sravani, R. Rao, Design of high throughput asynchronous FIR filter using gate level pipelinedmultipliers and adders. Int. J. Circuit Theory Appl. **48**(8), 1363–1370 (2020)
31. R.R. Sudharsan, J. Deny, *Field Programmable Gate Array (FPGA)-Based Fast and Low-Pass Finite Impulse Response (FIR) Filter. In Intelligent Computing and Innovation on Data Science* (Springer, Singapore, 2020), pp.199–206
32. K. Sundaram, V.K. Natarajan, N. Shanmugam, K. Manoharan, R. Ramasamy, S. Kumar, Area–energy–error optimized faithful multiplier for digital signal processing. Circ. Syst. Signal Process. **40**(12), 6224–6241 (2021)
33. C. Uthaya Kumar, S. Kamalraj, Ambient intelligence architecture of MRPM context based 12-tapfurther desensitized half band FIR filter for EEG signal. J. Ambient. Intell. Humaniz. Comput. **11**(4), 1459–1466 (2020)
34. G. Keerthiga and S. P. Kumar, "Evaluating FPGA-based denoising techniques for improved signal quality in electrocardiograms," Analog Integrated Circuits and Signal Processing, 2024, doi: 10.1007/s10470-024-02277-w.
35. M. Sinnoor and S. K. Janardhan, "An ECG Denoising Method Based on Hybrid MLTP-EEMD Model," International Journal of Intelligent Engineering and Systems, vol. 15, no. 1, pp. 575–583, 2022, doi: 10.22266/IJIES2022.0228.52.
36. A. Gon and A. Mukherjee, "Design and FPGA Implementation of an Efficient Architecture for Noise Removal in ECG Signals Using Lifting-Based Wavelet Denoising," in 2023 11th International Symposium on Electronic Systems Devices and Computing, ESDC 2023, Institute of Electrical and Electronics Engineers Inc., 2023. doi: 10.1109/ESDC56251.2023.10149865.
37. A. S. Deulkar and N. R. Kolhare, "FPGA implementation of audio and video processing based on Zedboard," in Proceedings of the 2020 International Conference on Smart Innovations in Design, Environment, Management, Planning and Computing, ICSIDEMPC 2020, 2020, pp. 305–310. doi: 10.1109/ICSIDEMPC49020.2020.9299639.
38. [1]L. Shang, A. S. Kaviani, and K. Bathala, "Dynamic Power Consumption in VirtexTM-II FPGA Family," 2002.