AVR Status Register

Hoda Roodaki

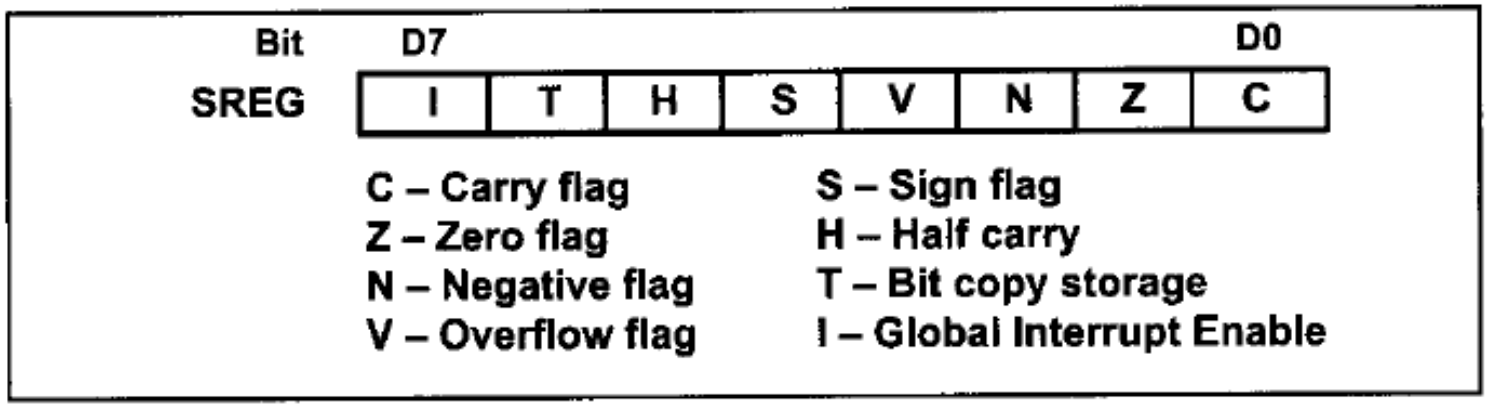
hroodaki@kntu.ac.ir

AVR STATUS REGISTER

- The AVR has a flag register to indicate arithmetic conditions such as the carry bit.
- The flag register in the AVR is called the *status register (SReg).*
  - The status register is an 8-bit register.
  - It is also referred to as the *flag register.*
  - The bits C, Z, N, V, S, and H are called *conditional flags,* meaning that they indicate some conditions that result after an instruction is executed.
  - Each of the conditional flags can be used to perform a conditional branch (jump).

AVR STATUS REGISTER

- Bits of Status Register (SREG)



  - ***C, the carry flag***
    - This flag is set whenever there is a carry out from the D7 bit.
      - This flag bit is affected after an 8-bit addition or subtraction.

AVR STATUS REGISTER

- ***Z, the zero flag***
  - The zero flag reflects the result of an arithmetic or logic operation.
    - If the result is zero, then Z = 1. Therefore, Z = 0 if the result is not zero.
- ***N, the negative flag***
  - Binary representation of signed numbers uses D7 as the sign bit.
    - The negative flag reflects the result of an arithmetic operation. If the D7 bit of the result is zero, then N = 0 and the result is positive.
    - If the D7 bit is one, then N = 1 and the result is negative.

AVR STATUS REGISTER

- ***v; the overflow flag***
  - This flag is set whenever the result of a signed number operation is too large, causing the high-order bit to overflow into the sign bit.
  - In general, the carry flag is used to detect errors in unsigned arithmetic operations while the overflow flag is used to detect errors in signed arithmetic operations.

AVR STATUS REGISTER

- ***H, Half carry flag***
  - If there is a carry from D3 to D4 during an ADD or SUB operation, this bit is set; otherwise, it is cleared.
  - This flag bit is used by instructions that perform BCD (binary coded decimal) arithmetic.
  - In some microprocessors this is called the AC flag (Auxiliary Carry flag).

ADD instruction and the status register

- The impact of the ADD instruction on the flag bits C, H, and Z of the status register.
  - All the flag bits C, Z, H, V, S, and N are affected by the ADD instruction,
  - V and S flag bits are related only to signed number operations.

Example

Show the status of the Z flag during the execution of the following program:

```
LDI    R20,4        ;R20 = 4
DEC    R20          ;R20 = R20 - 1
DEC    R20          ;R20 = R20 - 1
DEC    R20          ;R20 = R20 - 1
DEC    R20          ;R20 = R20 - 1
```

Solution:

The Z flag is one when the result is zero. Otherwise, it is cleared (zero). Thus:

After	Value of R20	The Z flag
LDI R20, 4	4	0
DEC R20	3	0
DEC R20	2	0
DEC R20	1	0
DEC R20	0	1

Example

Show the status of the C, H, and Z flags after the addition of 0x38 and 0x2F in the following instructions:

```
LDI   R16, 0x38
LDI   R17, 0x2F
ADD   R16, R17     ;add R17 to R16
```

Solution:

$38	0011 1000	
+ $2F	0010 1111	
$67	0110 0111	R16 = 0x67

C = 0 because there is no carry beyond the D7 bit.
H = 1 because there is a carry from the D3 to the D4 bit.
Z = 0 because the R16 (the result) has a value other than 0 after the addition.

Not all instructions affect the flags

- Some instructions affect all the six flag bits C, H, Z, S, V, and N
  - e.g., ADD.
- Some instructions affect no flag bits at all.
  - The load instructions are in this category.
- Some instructions affect only some of the flag bits.
  - The logic instructions (e.g., AND) are in this category.

Flag bits and decision making

- There are instructions that will make a conditional jump (branch) based on the status of the flag bits.

Table 2-5: AVR Branch (Jump) Instructions Using Flag Bits

Instruction	Action
BRLO	Branch if C = 1
BRSH	Branch if C = 0
BREQ	Branch if Z = 1
BRNE	Branch if Z = 0
BRMI	Branch if N = 1
BRPL	Branch if N = 0
BRVS	Branch if V = 1
BRVC	Branch if V = 0