COEN 122 Final Exam, 06-08-2021, 8:00 AM Student Name _____

1. (10 points)) Here is a series of address references given as word addresses: 4, 5, 6, 7, 8, 4, 5, 6, 7, 8, 23, 24, (assume the memory address takes five bits). Assuming a direct mapped cache with four two-word blocks (8 words in total) that is initially empty, indicate if it is a miss or hit for each reference, draw the cache and show the final contents of the cache. What is the miss ratio? How many bits are needed to implement this cache?

Reference:	Miss or hit	Reference:	Miss or hit
4		5	
5		6	
6		7	
7		8	
8		23	
4		24	

2. (10 points) Repeat the above question for a 2-way set associative cache with two-word blocks (8 words in total).

Reference:	Miss or hit	Reference:	Miss or hit
4		5	
5		6	
6		7	
7		8	
8		23	
4		24	

3. (20 points) Assume that memories in our pipeline are caches, and the cache miss penalty is 20 cycles per miss. The hit time is one cycle. The miss rates are as follows.

TLB miss rate	I cache miss rate	D cache miss rate	Page fault rate
1%	5%	8%	0

For give instruction mixture, assume the instruction count is *n*

	loads	store	R-type	branch	jumps
gcc	24%	12%	44%	18%	2%

3.1 What are the AMAT of TLB, I cache and D cache?

3.2 What is the average number of penalty cycles per instruction?

4. (20 points) Consider a system with the following parameters (byte addressable):

Virtual Addresses	31 bits
Physical Addresses	27 bits
Page size	4K Bytes
TLB	2-way set associative, 16 total entries
Cache	4-way set associative, block size: 8 words with total 1024 words

TLB

Index	Valid	Tag	PPN		Valid	Tag	PPN
000	0	0001	0071		1	0003	00C3
001	1	0001	0135		1	0000	0028
010	0	003A	01F4		1	1502	7868
011	1	0A02	1230		1	1403	7812
100	0	1B01	12A1		0	1D7F	8905
101	1	0003	124E		1	00D0	0053
110	1	0000	131F		1	0540	0034
111	1	0032	1209		1	111B	0E38

Page Table

VPN	PPN	Valid
000	71	1
001	28	1
002	93	1
003	AB	0
004	D6	0
005	53	1
006	1F	1
007	80	1
008	02	0
009	35	1
00A	41	0
00B	86	1
00C	A1	1
00D	D5	1
00E	8E	0
00F	D4	0
010	60	0
011	57	0
012	68	1
013	30	1
014	0D	0
015	2B	0
016	9F	0
017	62	0
018	C3	1
019	04	0
01A	F1	1
01B	12	1
01C	30	0
01D	4E	1
01E	57	1
01F	38	1

The content of the TLB and the first 32 entries of the page table are shown (all numbers are in hex except TLB indexes and valid bits)

- Show the number of bits used for the virtual page number and the virtual page offset

- Show the numbers of bits used for the TLB tag and TLB index

- How many entries are in the page table?

- Show the number of bits used for the physical page number and the physical page offset

- For the virtual address 0x02A068E6 what is the physical page number. Please do the following steps:
  - Virtual address in binary number
  - Indicate the page offset in the above binary address
  - Indicate the TLB index
  - Indicate the tag in hexadecimal number
  - Find the physical page number

- What is the physical address?

- What is the cache index for the above physical address?

5. (30 points) The Single Instruction Computer (SIC) has only one instruction that can do all operations our RISC-V does (you did a homework problem). The instruction has the following format

```
sbn a, b, c      # Mem[a]=Mem[a]- Mem[b]; if  (Mem[a]- Mem[b]<0) go to PC+c
```

For example, here is the program to copy a number from location a to location b:

```
Start:    sbn temp, temp, 1
          sbn temp, a, 1
          sbn b,b, 1
          sbn b, temp 1
```

Design a **single cycle datapath** and control for this instruction set architecture.

6. (10 points) Fill in the blank with the correct answer.

(1) The CPU time for executing a program is a product of the instruction count of that program, the CPI and _____.

(2) The computer architecture is defined by the instruction set architecture and _____.

(3) The RISC-V ALU control which tells the ALU what to do takes _____ input bits and generates _____ output bits.

(4) In a computer system with 2^{30} virtual memory space, 2^{24} physical memory space, and page size = 4k, the page table contains _____ entries assuming the program is very large.

(5) The five classic components of a computer are _____.

(6) The addressing mode of `beq x1, x2 100` is _____.

(7) TLB is a cache holding _____.

(8) Data dependence is defined as _____

(9) The binary code representing `lw x3, 100(x4)` (the opcode of lw is 3) is _____

(10) The addressing mode of `lw x3, 100(x4)` is _____