Coen 122 Final Exam

1)

Reference	M/H	Reference	M/H
4	M	5	H
5	H	6	H
6	M	7	H
7	H	8	H
8	M	23	M
4	H	24	M

Cache:

Index	V	Tag	D0	D1
00	1	11	M[23]	M[24]
01	0			
10	1	00	M[4]	M[5]
11	1	10	M[22]	M[23]

Miss Rate:
5/12
Bits needed: 4*(64+3) = 268

2)

Reference	M/H	Reference	M/H
4	M, 0 0100	5	H
5	H	6	H
6	M, 0 0110	7	H
7	H	8	H
8	M, 0 1000	23	M, 1 0111
4	H	24	M, 1 1000

Cache:

Index	V	Tag	D0	D1	V	Tag	D2	D3
0	1	110	M[23]	M[25]	1	010	M[8]	M[9]
1	1	001	M[6]	M[7]	1	101	M[22]	M[23]

Miss Rate: 5/12
Bits Needed: 4*(4+64) = 272

3)
Cache Miss Penalty: 20 cycles. Hit Time: 1 cycle.

TLB miss rate	I cache miss rate	D cache miss rate	Page fault rate
1%	5%	8%	0

For give instruction mixture, assume the instruction count is *n*

	loads	store	R-type	branch	jumps
gcc	24%	12%	44%	18%	2%

TLB AMAT:
HT + MR * MP
1 + (0.01 * 20) = 1.2

I-Cache AMAT:
1 + (0.05 * 20) = 2

D-Cache AMAT:
1 + (0.08 * 20) = 2.6

3.2 What is the average number of penalty cycles per instruction?

The average number of penalty cycles per instruction will be a constant * *n*.
4)

Bits of VPN and VPO
Page Offset = 12 bits
Virtual Page # = 31-12 = 19 bits
Physical Page # = 27 – 12 = 15 bits

Bits of TLB Tag and TLB Index
8 sets from (2^3 = 8)
TLB Index = 3 bits. TLB Tag = VPN(19) – 3 = 16 bits.

Entries in Page Table
2^VPN = 2^19

Bits for PPN and PPO
PPN = PA(27) – offset(12)
PPN = 15 bits.
PPO = 12 bits.

0x02A068E6 in binary
0000 0010 1010 0000 0110 1000 1110 0110

TLB Tag: 000 0010 1010 0000 0
TLB Index: 110
Page Offset: 1000 1110 0110
VPN: 0000 0010 1010 0000 0110

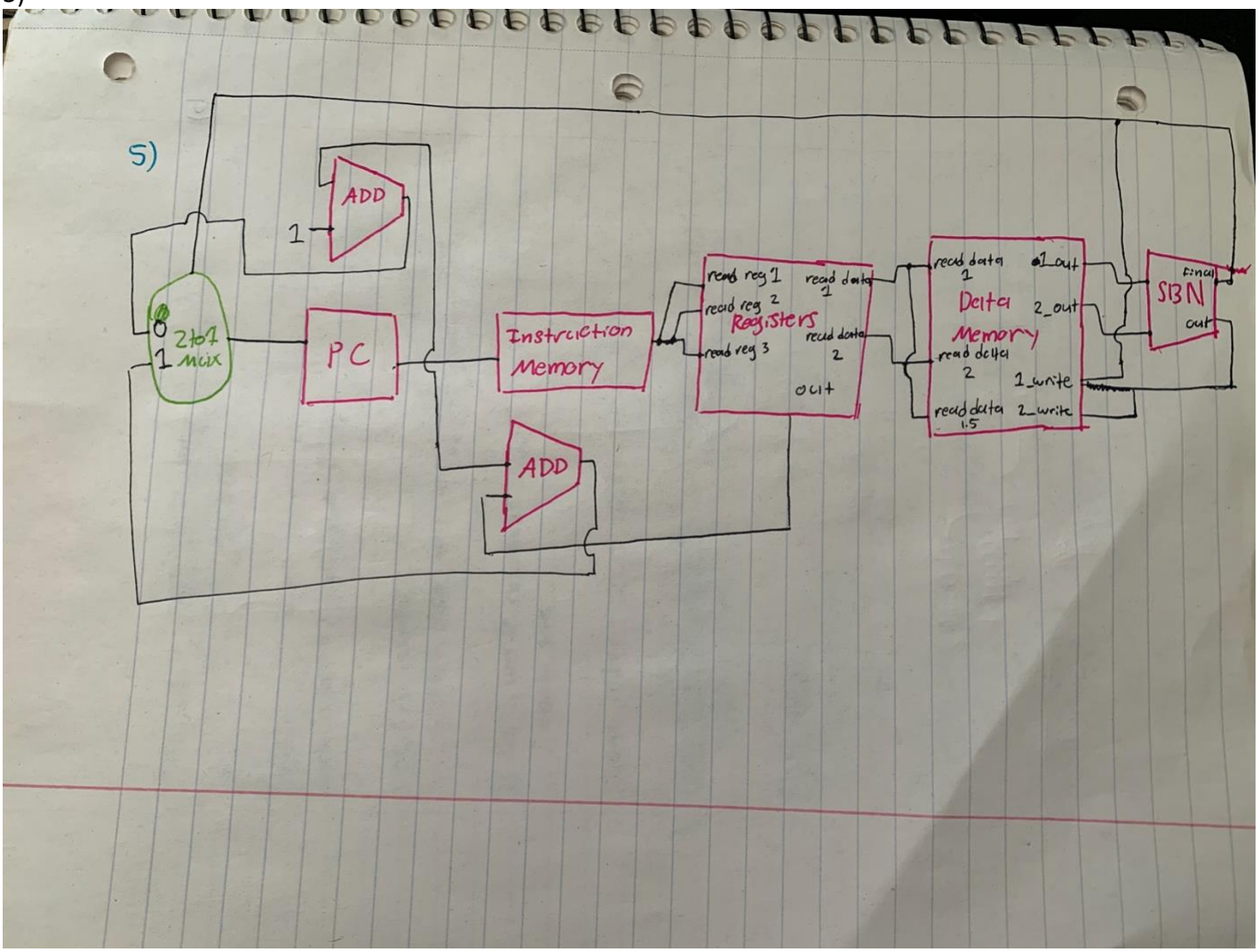
TLB Tag in Hex: 0x054
Therefore, PPN = 0034

Physical Address
0x0034 ➔ 0000 0000 0011 0100
Page offset ➔1000 1110 0110

Therefore, PA = 0000 0000 0011 0100 1000 1110 0110

Cache Index
2^5 = 32 sets so 5 bits.

5)



6)

1: Clock time

2: Computer Organization

3: 4, 3

4: 2^34/2^12 = 2^22

5: input, output, memory, datapath, control

6: PC-Relative

7: Translation

8: … the instruction refers to data from the preceding statement.

9: 0000 0000 0000 0000 0110 1000 0011 0011

10: Base Addressing