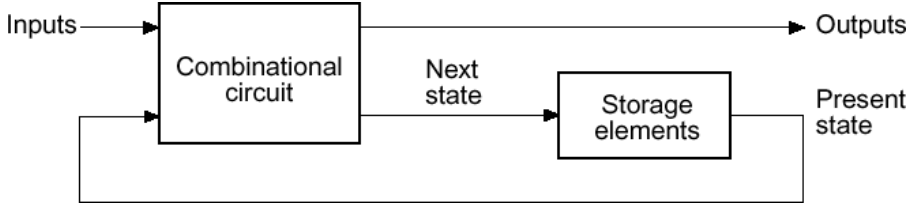
Sequential Logic
Flip-flops

Introduction

- Flip flop is a binary cell capable of storing one bit of data.
- Flip flop is a sequential circuit (means output= present input + past output).
- Flip flop contain memory element to store past output.
- Flip flops has two outputs:
  - Normal output
  - Complement output

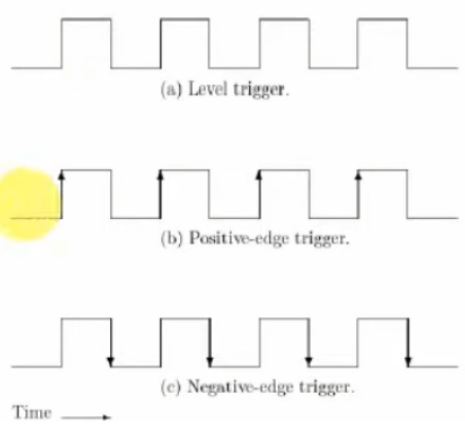


Introduction

- There are mainly four types of flip flops that are used in electronic circuits:
  - The basic flip flop or S-R Flip Flop
  - J-K Flip flop
  - Delay Flip flop (D Flip flop)
  - T (Toggle) Flip flop

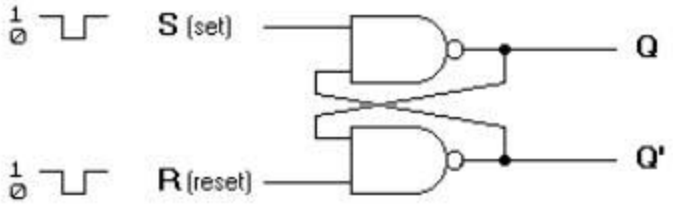
Flip Flops Vs Latch

Flip Flops	Latch
A Flip-flop always have a clock signal	latche doesn't have a clock signal
It checks the inputs but changes the output only at times defined by the clock signal or any other control signal.	Latch is an electronic device, which changes its output immediately based on the applied input. It is used to store either 1 or 0 at any specified time.
They are classified into asynchronous or synchronous flip flops.	There is no such classification in latches.
It is a edge triggered device.	It is a level triggered device.



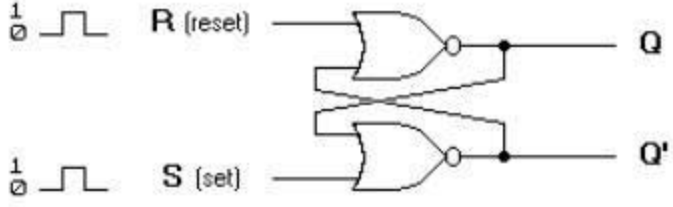
SR Flip Flop

- The SET RESET Flip Flop is designed with the help of two NOR gates and also two NAND gates. These flip flops are also called S-R Latch.



(a) Logic diagram

S R Flip Flop Using Two NAND Gate

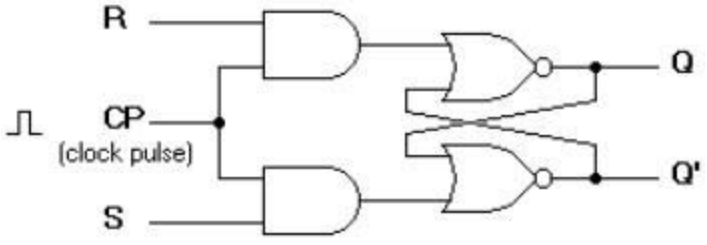


(a) Logic diagram

S R Flip Flop Using Two NOR Gate

SR Flip Flop

S R Flip Flop Using Two NOR Gate and two AND Gate



(a) Logic diagram

Truth Table for SR Flip Flop

S	R	Q(N+1)
0	0	Q(N)
0	1	0
1	0	1
1	1	Indeterminate/Invalid

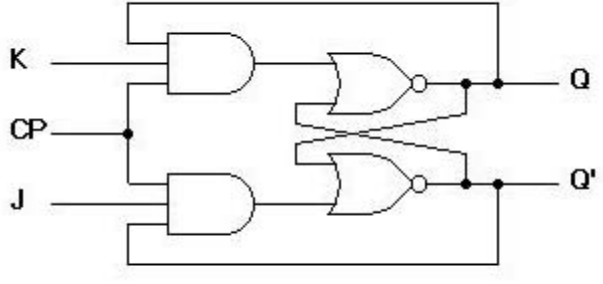
Characteristic table for SR Flip Flop

S	R	Q(N)	Q(N+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Characteristic equation:- **Q(N+1)=S+R`Q(N)**

J-K Flip Flop

- In SR flip Flop invalid state is present when both inputs are one. to avoid this JK Flip Flop is used. JK Flip Flop is refinement of SR Flip Flop.



(a) Logic diagram

Truth table of JK Flip Flop

J	K	Q(N+1)	
0	0	Q(N)	Hold
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	Q`(N)	toggle

J-K Flip Flop

Characteristic Table

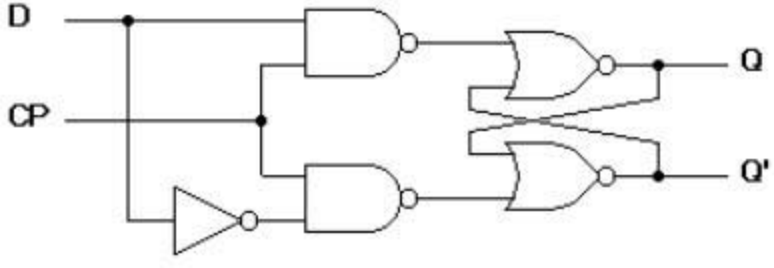
J	K	Q(N+1)	
0	0	Q(N)	Hold
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	Q`(N)	toggle

J	k	Q(N)	Q(N+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Characteristic Equation: Q(N+1)=JQ`(N)+K`Q(N)

Delay Flip Flop (D Flip Flop)

- It is also called transparent latch because in D flip Flop input and output are equal. SR Flip Flop are converted into D Flip Flop by applying inverter between S And R.



(a) Logic diagram with NAND gates

Truth table of D Flip Flop

D	Q(N+1)	
0	0	Clear to 0
1	1	Set to 1

D Flip Flop

D	Q(N+1)	
0	0	Clear to 0
1	1	Set to 1

Characteristic Table

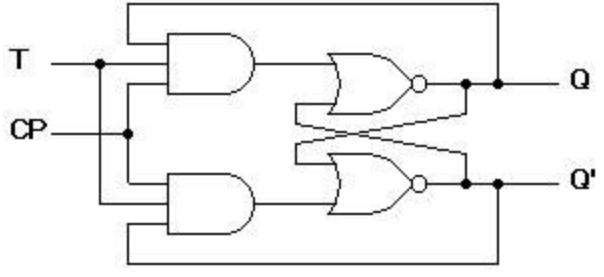
D	Q(N)	Q(N+1)
0	0	0
0	1	0
1	0	1
1	1	1

Characteristic Equation: Q(N+1)=D

T(Toggle) Flip Flop

- Toggle flip flop obtained from JK Flip Flop. in JK flip flop when inputs J and K connected to provide a single input by T.

$$J = K = T$$



(a) Logic diagram

Truth table of T Flip Flop

T	Q(N+1)
0	Q(N)
1	Q`(N)

T Flip Flop

T	Q(N+1)
0	Q(N)
1	Q`(N)

Characteristic Table

T	Q(N)	Q(N+1)
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic Equation: Q(N+1)= T'Q(N)+Q`(N)T

Thank you!