Group 28 Resistor

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Group 28
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Introduction and Physical Properties

1) Cell Description

This report will detail the simulation of an inverter using a resistive load. The value of the load was chosen to emulated the behavior observed by using an enhancement load nFET inverter. The benefits or drawbacks of this configuration will be explored in this report.

2) Cell Symbol

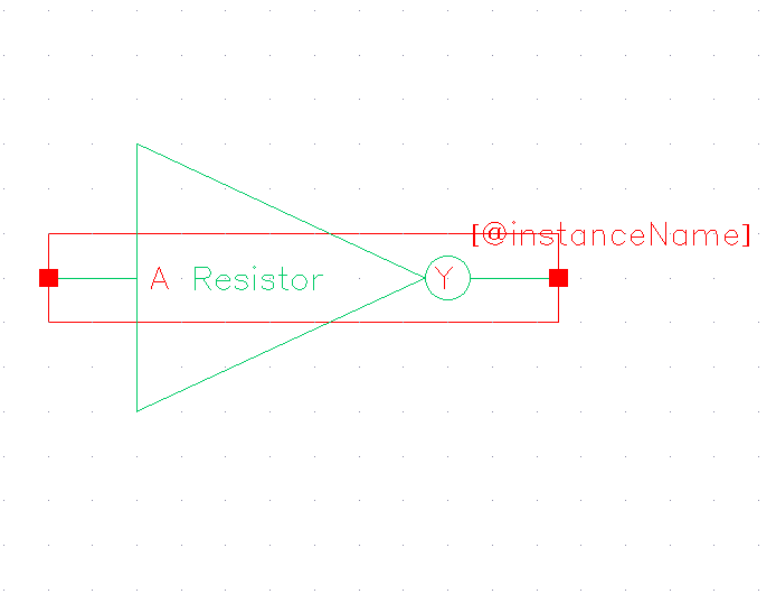

Figure 1: Inverter Symbol

Cell Truth Table

Cell Truth Table	
Cell Inputs {A}	Cell Outputs {Y}
0	1
1	0

3) Cell Schematic Diagram

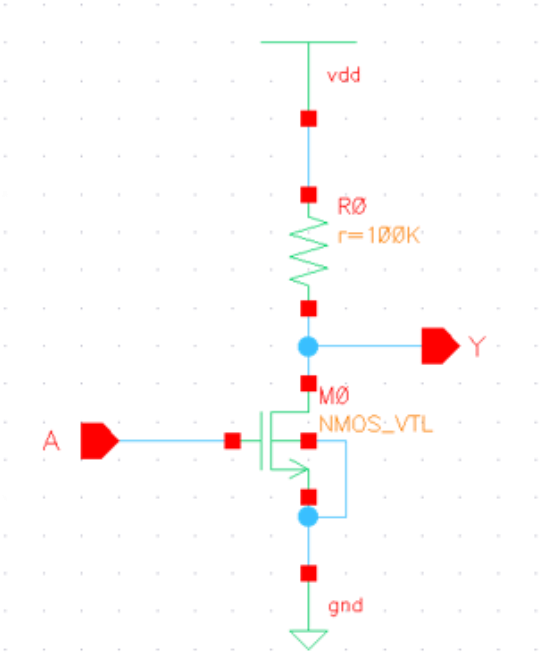

Figure 2: Inverter with Resistive Load

4,5) Cell Layout Diagram and Dimensions

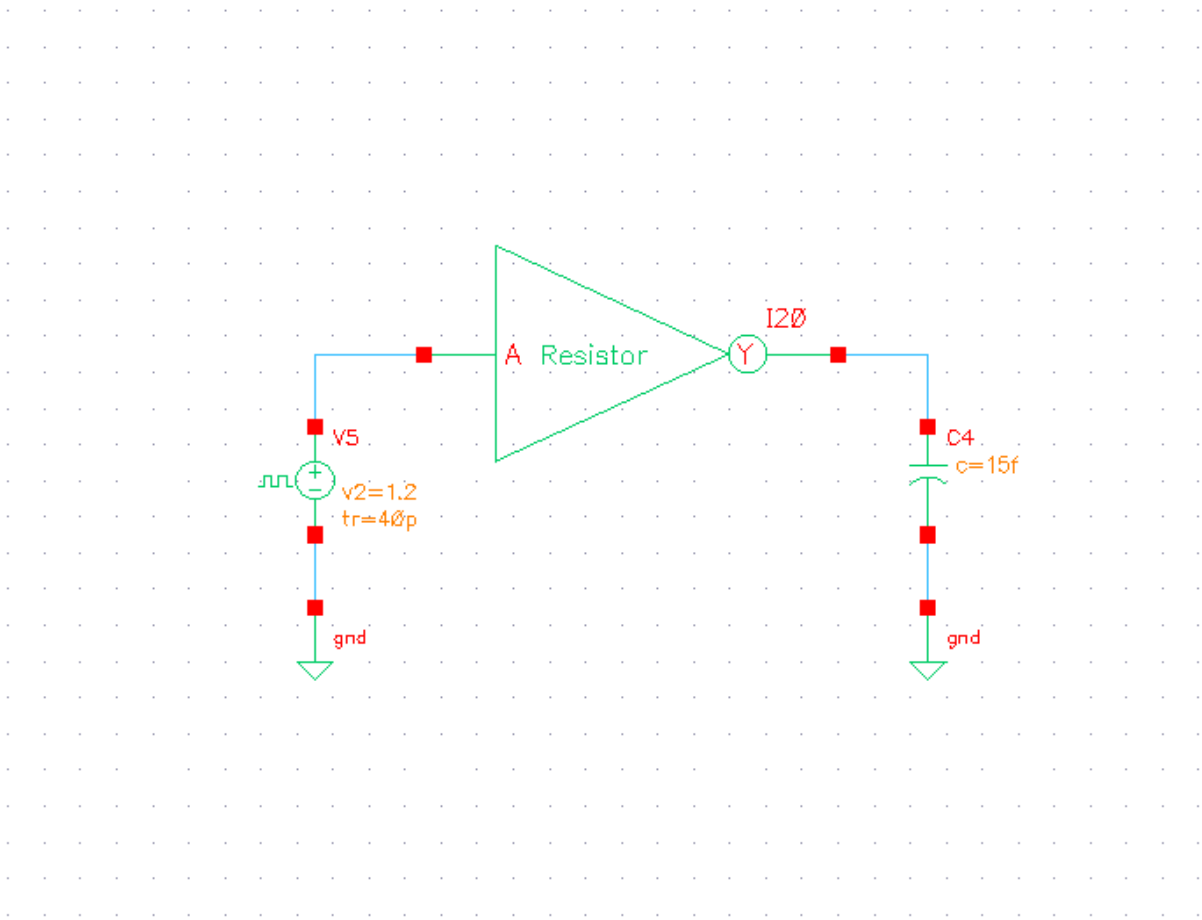

Figure 3: Inverter with Resistive Load Schematic

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
M0	90	50

Performance Analysis

6,7) Rise and Fall Times

In the rise time and fall time table below, please ONLY fill in data for Output Load (Fox) = 4 and you do NOT need to fill in the data for Output load (Fox) of 0, 1, 2, 8 and can leave them blank.

Input X: Output Rise Time Data t_r (ns)					
Input rise/fall time (ns)	Output Load (Fox)				
	0	1	2	4	8
0.04				1.915 ns	

Stack Input Combination: ***Replace with Boolean Product***

S, Input X: Output Fall Time Data t_f (ns)	
	Output Load (Fox)

S, Input X: Output Fall Time Data t_f (ns)					
Input rise/fall time (ns)	0	1	2	4	8
0.04				114.8 ps	

Stack Input Combination: ***Replace with Boolean Product***

8,9) Propagation Delays

In the propagation delay tables below, please ONLY fill in data for Output Load (Fox) = 4 and you do NOT need to fill in the data for Output load (Fox) of 0, 1, 2, 8 and can leave them blank.

Data Worst Case Low to High Propagation Delay Data t_{plh} (ns)					
Input rise/fall time (ns)	Output Load (Fox)				
	0	1	2	4	8
0.04				957.891 ps	

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Output Load (Fox)				
	0	1	2	4	8
0.04				91.141ps	

Worse Case Input Combination: ***Replace with Boolean Product***

10, 11) Prepare two additional tables (shown below) comparing the performance of the six inverters.

DC Analysis

Type	**V_{IH_DC}**	**V_{IL_DC}**	**V_{OH_DC}**	**V_{OL_DC}**
CMOS	613.3 mV	369.374mV	1.129 V	53.0749 mV
CMOS_Wide	614.032 mV	369.597 mV	1.12876 V	53.98402 mV
Enhancement mode NFET	624.679 mV	344.751 mV	508.4854 mV	117.3766 mV
Enhancement mode NFET_Long	550.588 mV	270.727 mV	528.8089 mV	66.04702 mV
Resistive load (100k Ohms)	612.429 mV	276.79 mV	1.12942 V	88.8312 mV
Resistive load_long (350k Ohms)	527.1055 mV	218.764 mV	527.105 mV	46.21169 mV

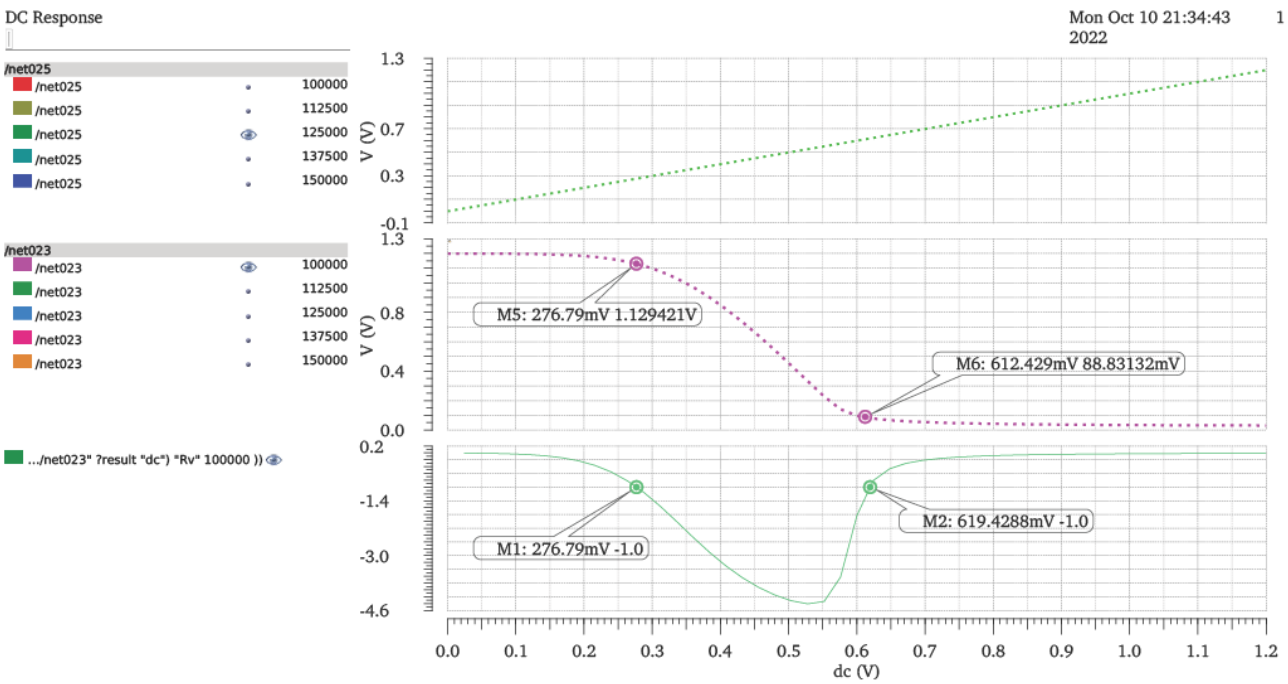

Figure 4: Inverter with Resistive Load DC Simulation

Transient Analysis

Type	tp_{lh}	tp_{hl}	t_r	t_f
CMOS	275.31 ps	92.428 ps	397.4 ps	115.4 ps
CMOS_Wide	70.8488 ps	27.66 ps	94.62 ps	29.35 ps
Enhancement mode NFET	352.924 ps	60.862 ps	1.224 ns	73.24 ns
Enhancement mode NFET_Long	836.513 ps	55.4595 ps	2.017 ns	75.0 ps
Resistive load	957.891 ps	91.141ps	1.915 ns	114,8 ps
Resistive load_long	2.03 ns	61.69 ps	2.816 ns	84.26 ps

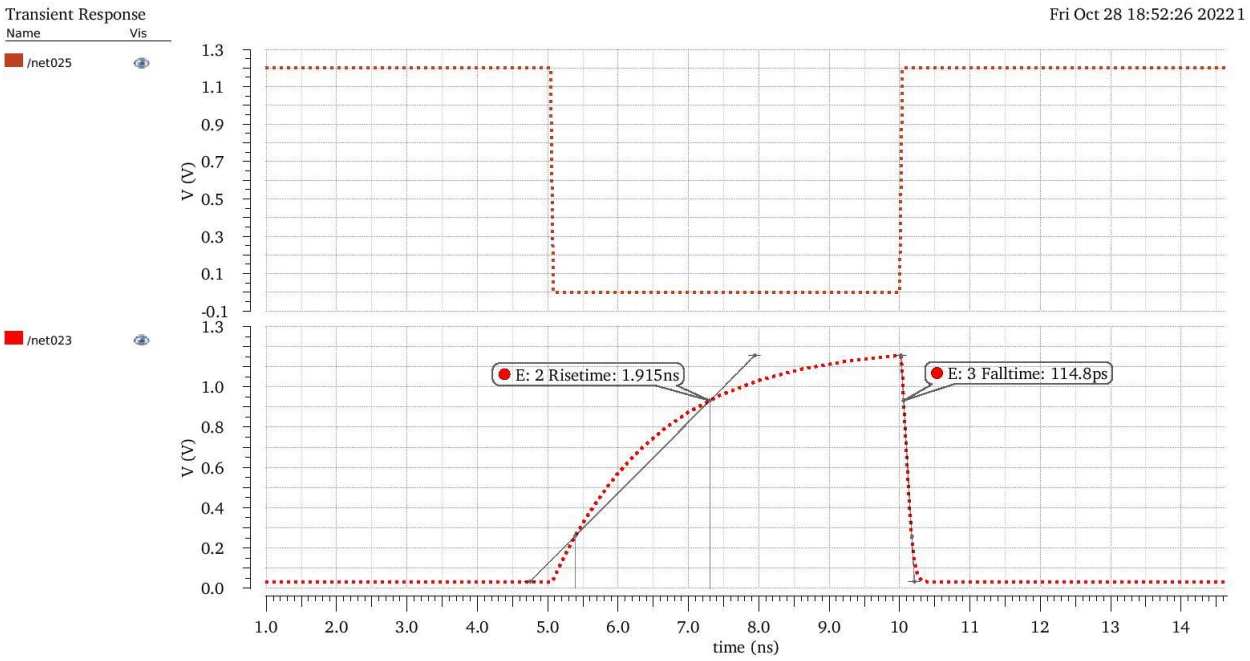

Figure 5: Inverter with Resistive Load Transient Fall/Rise time

Group 28 Resistor Long

Introduction and Physical Properties

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1) Cell Description

This report will detail the simulation of an inverter using a resistive load. The value of the load was chosen to emulated the behavior observed by using an enhancement load nFET inverter in the long configuration. The benefits or drawbacks of this configuration will be explored in this report.

2) Cell Symbol

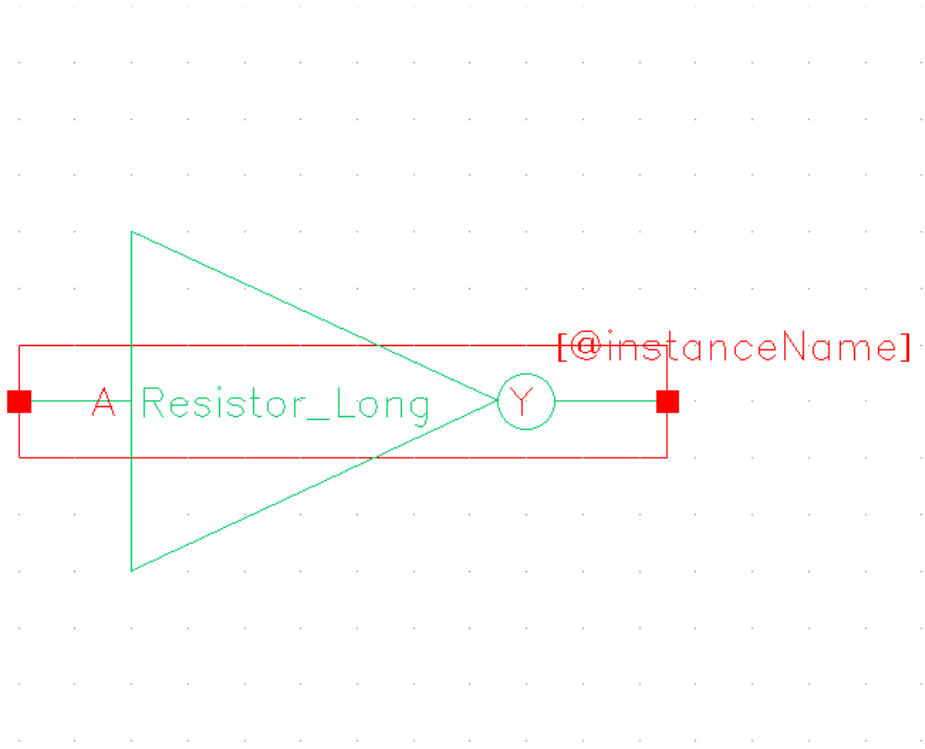

Figure 6: Inverter Symbol

Cell Truth Table

Cell Truth Table	
Cell Inputs {A}	Cell Outputs {Y}
0	1
1	0

3) Cell Schematic Diagram

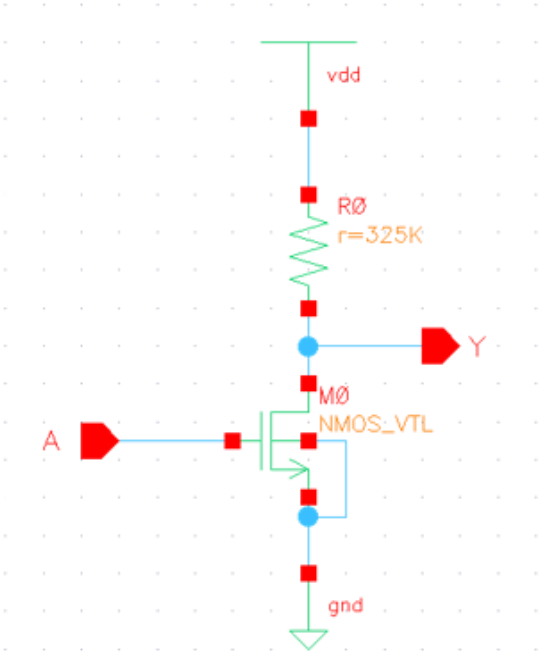

Figure 7: Inverter with Resistive Load

4,5) Cell Layout Diagram and Dimensions

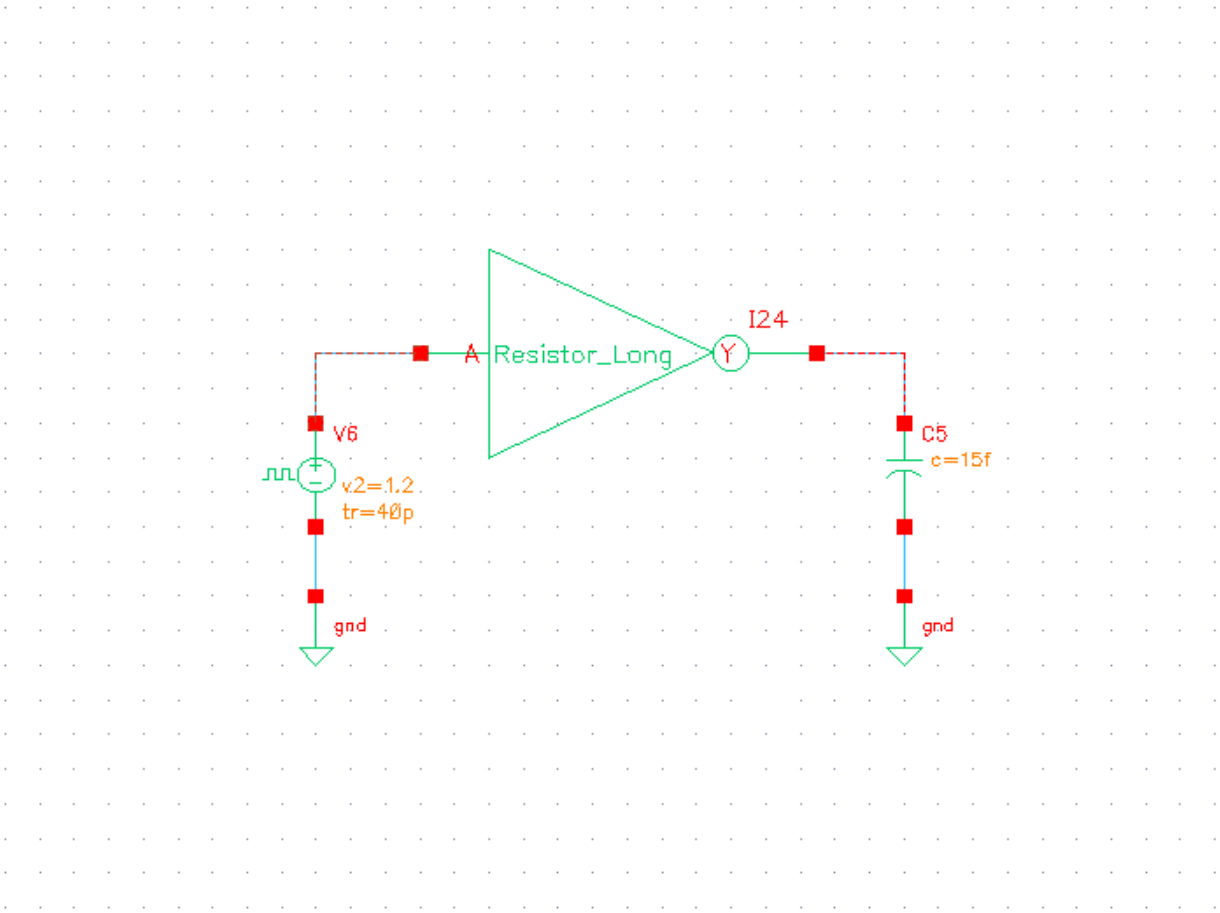

Figure 8: Inverter with Resistive Load Schematic (Long)

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
M0	90	50

Performance Analysis

6,7) Rise and Fall Times

In the rise time and fall time table below, please ONLY fill in data for Output Load (Fox) = 4 and you do NOT need to fill in the data for Output load (Fox) of 0, 1, 2, 8 and can leave them blank.

Input X: Output Rise Time Data t_r (ns)					
Input rise/fall time (ns)	Output Load (Fox)				
	0	1	2	4	8
0.04	X	X	X	2.816 ns	X

Stack Input Combination: ***Replace with Boolean Product***

S, Input X: Output Fall Time Data t_f (ns)	
	Output Load (Fox)

S, Input X: Output Fall Time Data t_f (ns)					
Input rise/fall time (ns)	0	1	2	4	8
0.04	X	X	X	84.26 ps	X

Stack Input Combination: ***Replace with Boolean Product***

8,9) Propagation Delays

In the propagation delay tables below, please ONLY fill in data for Output Load (Fox) = 4 and you do NOT need to fill in the data for Output load (Fox) of 0, 1, 2, 8 and can leave them blank.

Data Worst Case Low to High Propagation Delay Data t_{plh} (ns)					
Input rise/fall time (ns)	Output Load (Fox)				
	0	1	2	4	8
0.04	X	X	X	2.03 ns	X

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Output Load (Fox)				
	0	1	2	4	8
0.04	X	X	X	61.69 ps	X

Worse Case Input Combination: ***Replace with Boolean Product***

10, 11) Prepare two additional tables (shown below) comparing the performance of the six inverters.

DC Analysis

Type	V_{IH_DC}	V_{IL_DC}	V_{OH_DC}	V_{OL_DC}
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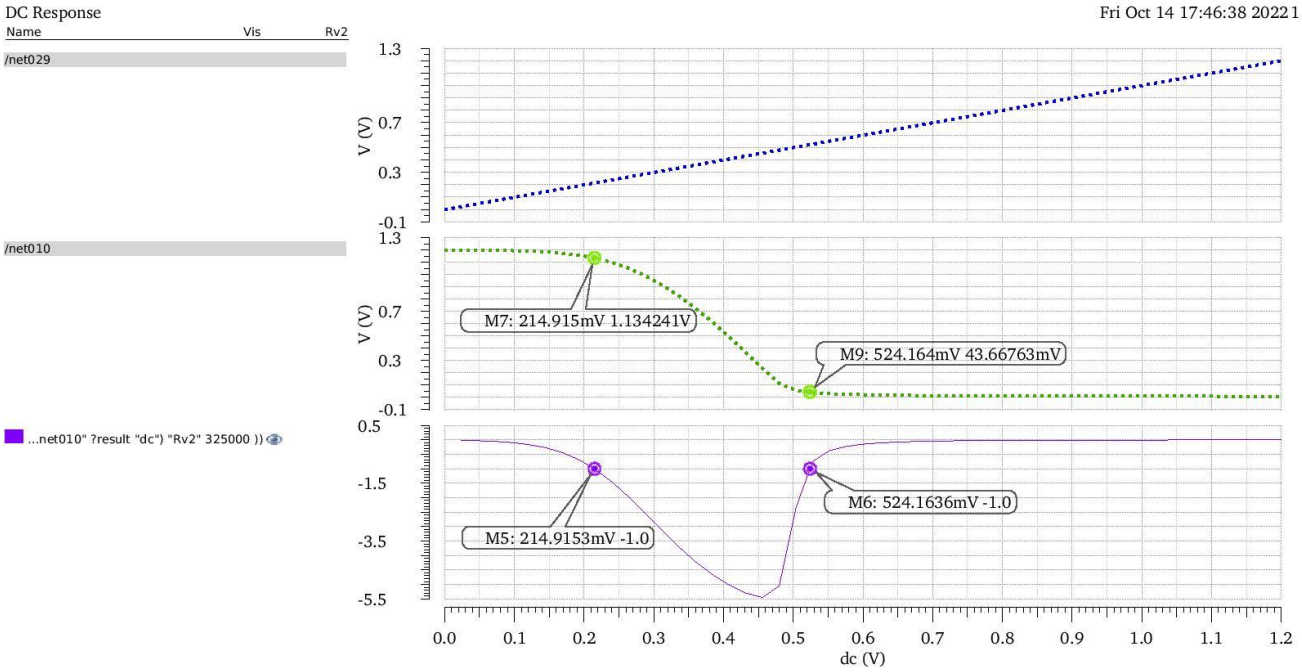

Figure 9: Inverter with Resistive Load DC Simulation

Transient Analysis

Type	tp_{lh}	tp_{hl}	t_r	t_f
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Enhancement mode NFET	352.924 ps	60.862 ps	1.224 ns	73.24 ns
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Resistive load	957.891 ps	91.141ps	1.915 ns	114,8 ps
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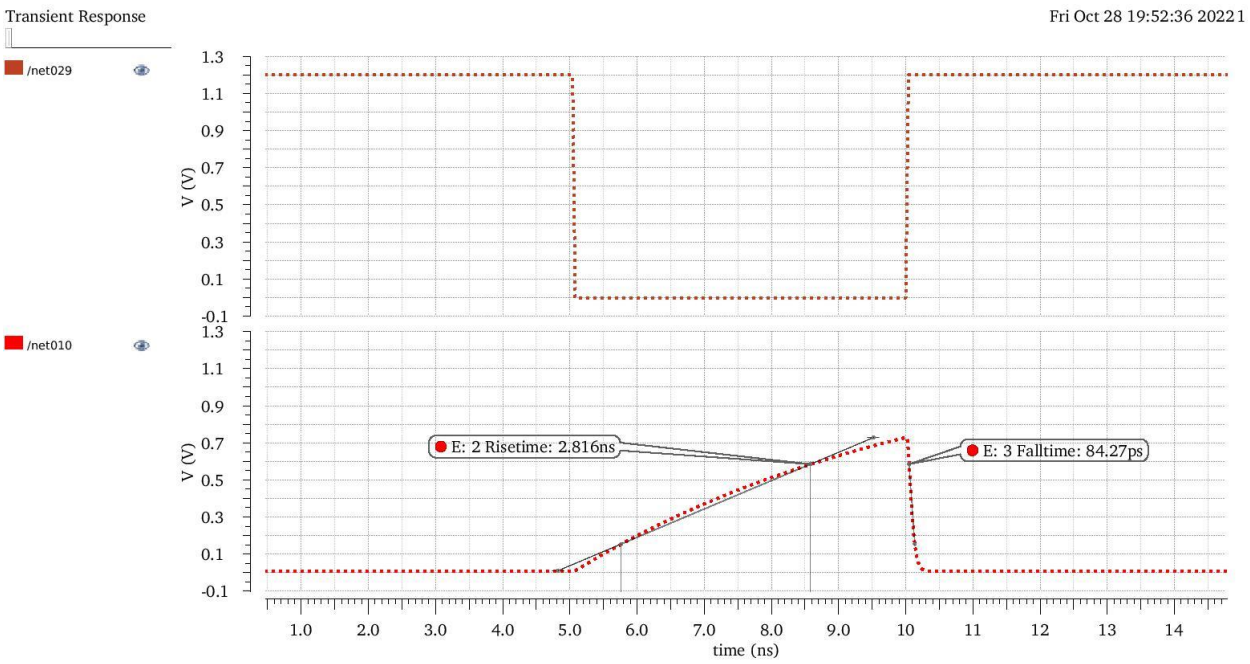

Figure 10: Inverter with Resistive Load Transient Fall/Rise time