Enhancement mode NFET

Juan Rivera-Mena, Mehul Shah and Jesus Zavala
Group 28
10/28/2022

Introduction and Physical Properties

1) **Cell Description**

There were three inverter configurations that were created and analyzed - the three inverter configurations were the static CMOS inverter, Enhancement mode-NFET and the resistive load Inverter. The Static CMOS Inverter has a pMOS and nMOS that are connected in series. Both the nMOS and pMOS receive the same input. The output depends on the input; if the nMOS is turned ON from the input, the output will be LOW. pMOS will be the opposite of an nMOS.

The Enhancement mode-NFET is a nMOS inverter - there is a nMOS that is replacing the pMOS, whose input is connected to VDD which constantly keeps this nMOS ON/HIGH. The second nMOS receives the input which turns ON or OFF depending on the input it receives. The body of both nMOS are connected to ground. The resistive load inverter is an nMOS inverter which uses a resistor on the drain. The resistor is replacing the pMOS which would have been connected to the nMOS if it was a regular pMOS.

2) **Cell Symbol**

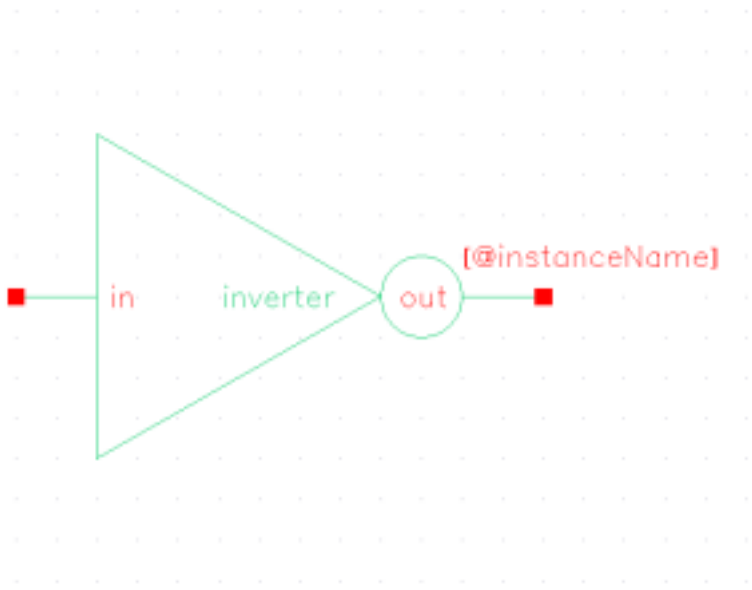


Figure 1: Example Logic Symbol for Enhancement NFET. All symbols are 1in tall.

Cell Truth Table

The truth table of the CMOS Inverter is shown below - when the CMOS inverter receives a LOW (0), the output will be a HIGH (1). When the Inverter receives a HIGH (1), it will output a LOW (0)

CMOS Inverter Truth Table	
Cell Inputs {0,1}	Cell Outputs {0,1} Y
0	1
1	0

3) **Cell Schematic Diagram**

The following schematics were created in Cadence Virtuoso.

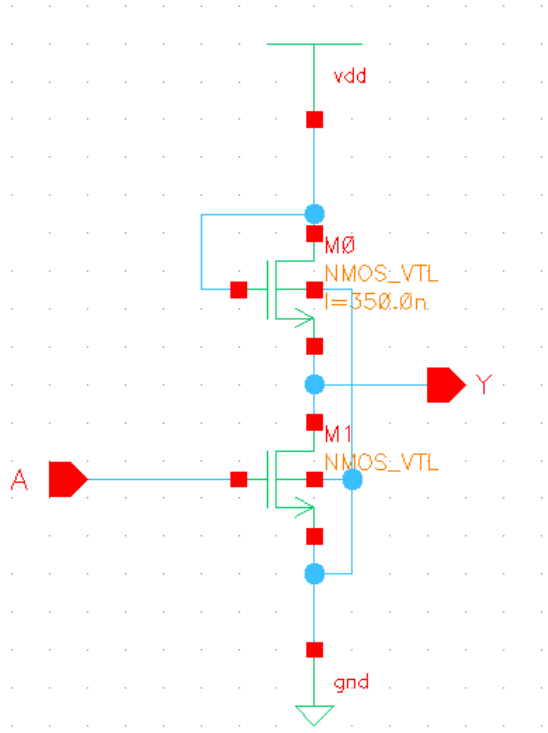
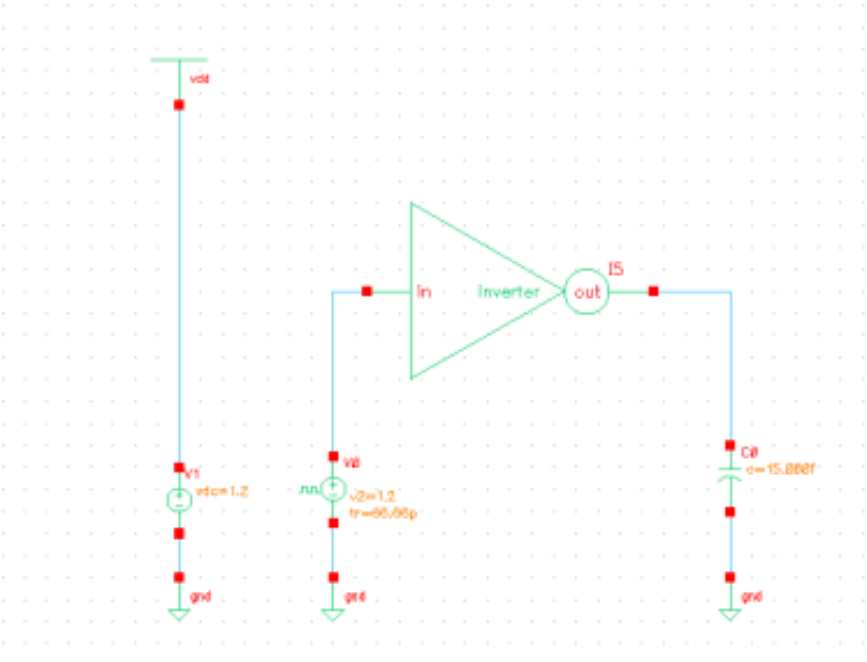


Figure 1: CMOS Enhancement Inverter where 'A' in the input and 'Y' is the output. All schematic symbols are 4" in height.

4,5) Cell Layout Diagram and Dimensions



Transistor Dimensions			
Type of Inverter	Transistor Instance Number	Length (nm)	Width (nm)
Enhancement Mode NFET Inverter	NMOS - MO	350	90
	NMOS - M1	50	90

Performance Analysis

6,7) Rise and Fall Times

Input X: Output Rise Time Data t_r (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04				1.224 ns	

Stack Input Combination: ***Replace with Boolean Product***

S, Input X: Output Fall Time Data t_f (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04				73.24 ns	

Stack Input Combination: ***Replace with Boolean Product***

8,9) Propagation Delays

Data Worst Case Low to High Propagation Delay Data t_{plh} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04				352.924 ps	

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04				60.862 ps	

Worse Case Input Combination: ***Replace with Boolean Product***

10, 11) Prepare two additional tables (shown below) comparing the performance of the six inverters.

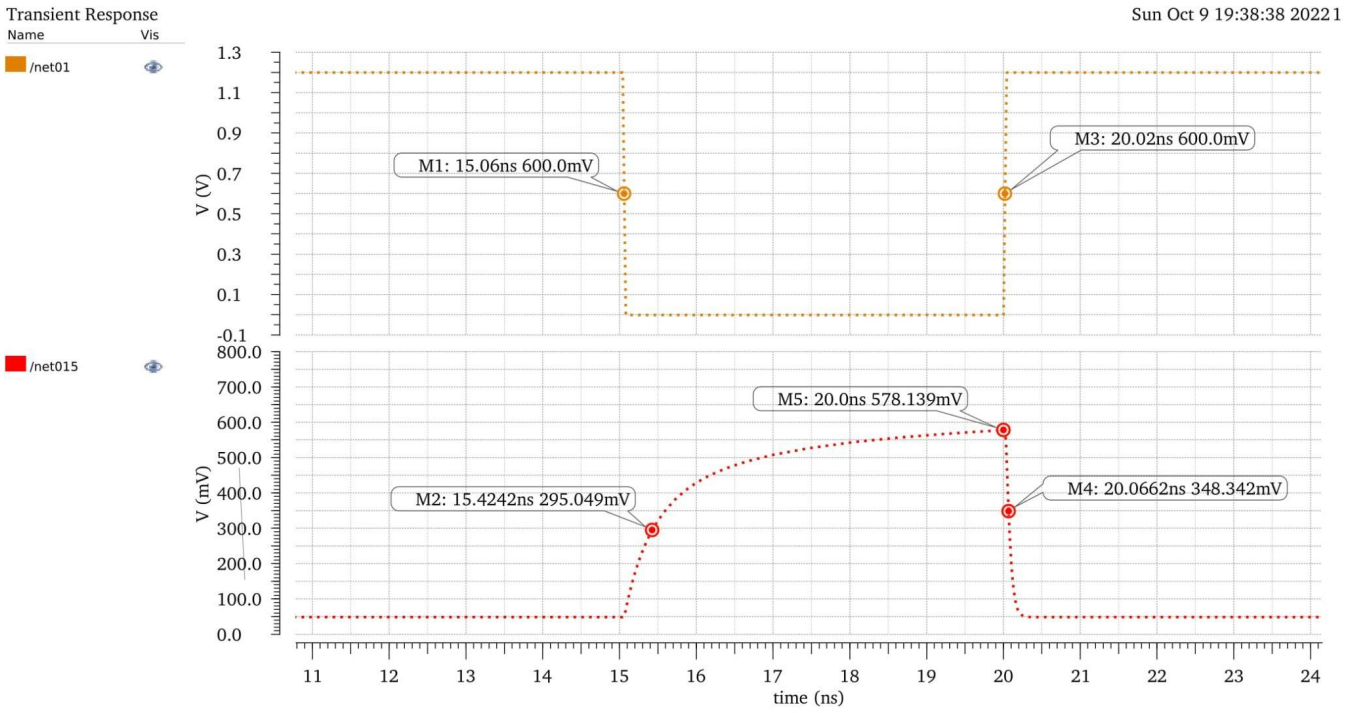
DC Analysis

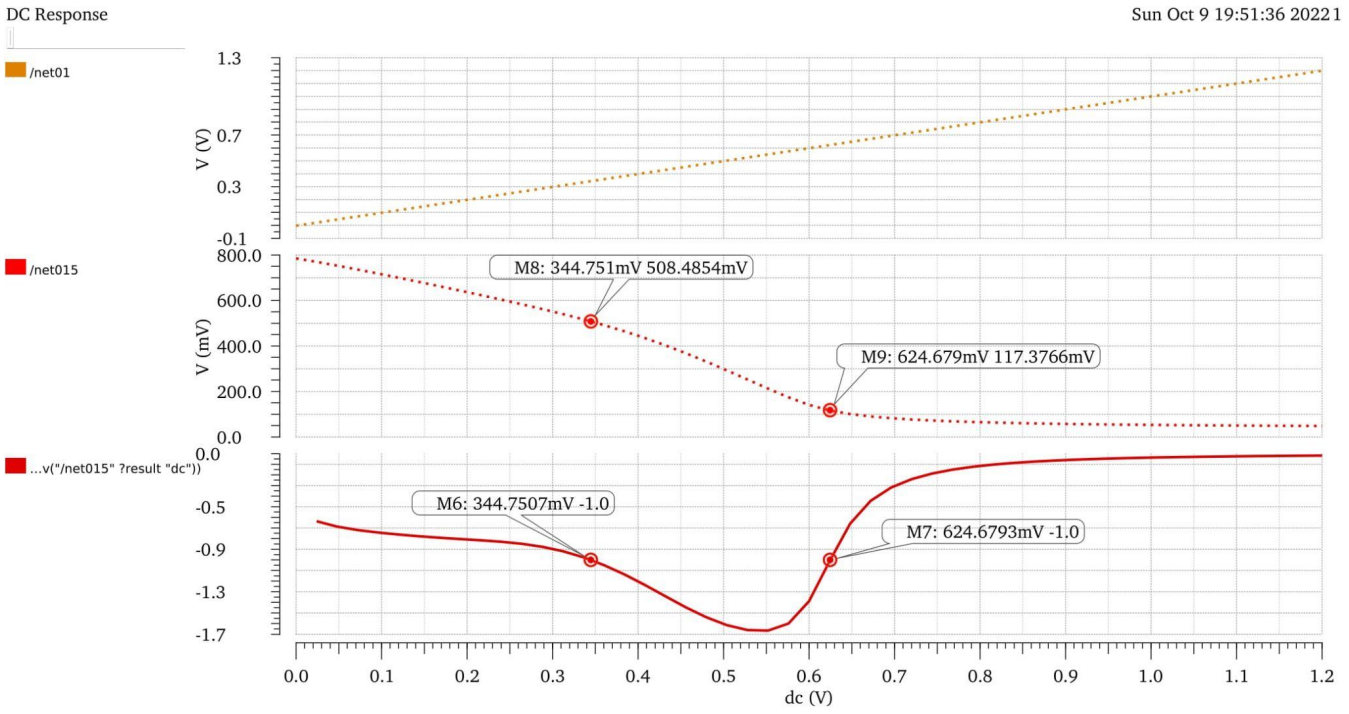
Type	V_{IH_DC}	V_{IL_DC}	V_{OH_DC}	V_{OL_DC}
CMOS	613.3 mV	369.374mV	1.129 V	53.0749 mV
CMOS_Wide	614.032 mV	369.597 mV	1.12876 V	53.98402 mV
Enhancement mode NFET	624.679 mV	344.751 mV	508.4854 mV	117.3766 mV
Enhancement mode NFET_Long	550.588 mV	270.727 mV	528.8089 mV	66.04702 mV
Resistive load (100k Ohms)	612.429 mV	276.79 mV	1.12942 V	88.8312 mV
Resistive load_long (350k Ohms)	527.1055 mV	218.764 mV	527.105 mV	46.21169 mV

Transient Analysis

Type	tp_{lh}	tp_{hl}	t_r	t_f
CMOS	275.31 ps	92.428 ps	397.4 ps	115.4 ps
CMOS_Wide	70.8488 ps	27.6606 ps	94.62 ps	29.35 ps
Enhancement mode NFET	352.924 ps	60.862 ps	1.224 ns	73.24 ns
Enhancement mode NFET_Long	836.513 ps	55.4595 ps	2.017 ns	75.0 ps
Resistive load	957.891 ps	91.141ps	1.915 ns	114,8 ps
Resistive load_long	2.03 ns	61.69 ps	2.816 ns	84.26 ps

12) DC and Transient Analysis Plots:





Enhancement mode NFET Long

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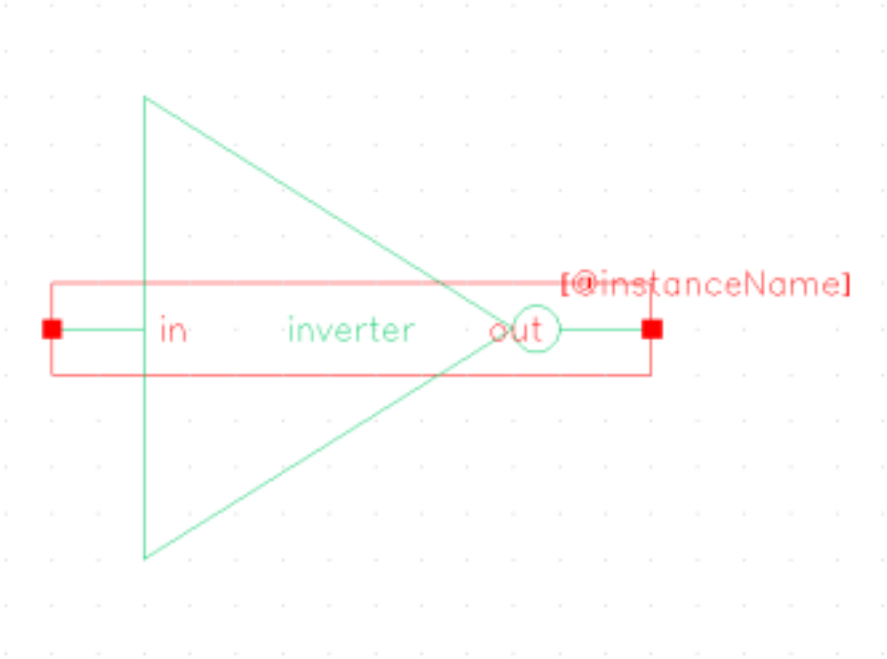
2) Cell Symbol



Cell Truth Table

The truth table of the CMOS Inverter is shown below - when the CMOS inverter receives a LOW (0), the output will be a HIGH (1). When the Inverter receives a HIGH (1), it will output a LOW (0)

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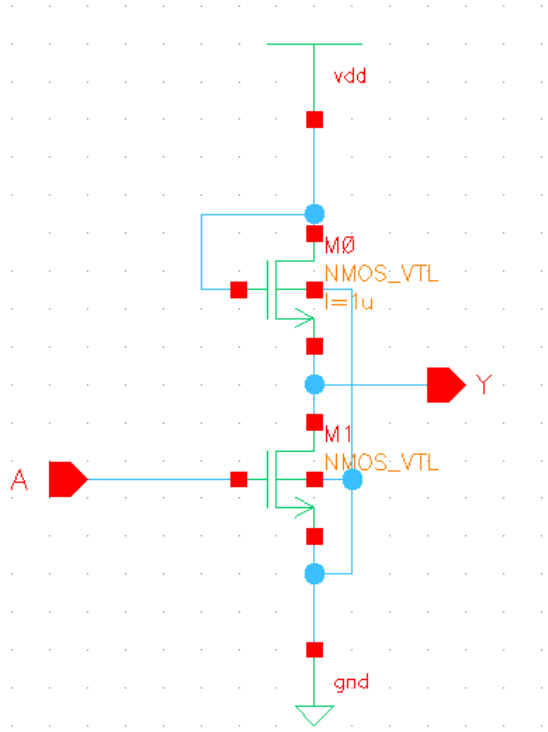
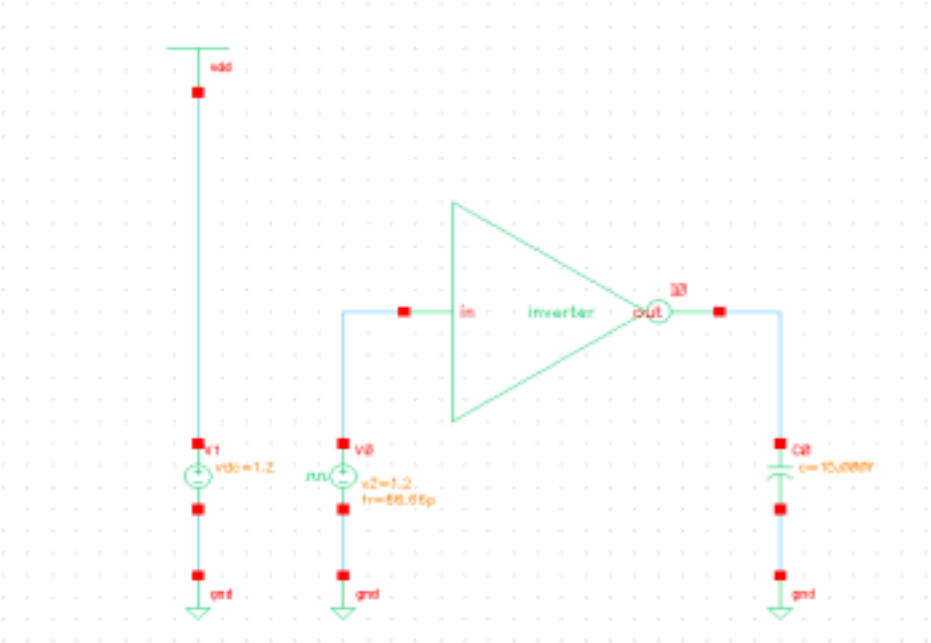


Figure 2: CMOS Enhancement Long Inverter where 'A' in the input and 'Y' is the output. All schematic symbols are 4" in height.

4,5) Cell Layout Diagram and Dimensions



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Input X: Output Rise Time Data t_r (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04				2.017 ns	

Stack Input Combination: ***Replace with Boolean Product***

S, Input X: Output Fall Time Data t_f (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04				75.0 ps	

Stack Input Combination: ***Replace with Boolean Product***

8,9) Propagation Delays

Data Worst Case Low to High Propagation Delay Data t_{plh} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04				836.513 ps	

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04				55.4595 ps	

Worse Case Input Combination: ***Replace with Boolean Product***

10, 11) Prepare two additional tables (shown below) comparing the performance of the six inverters.

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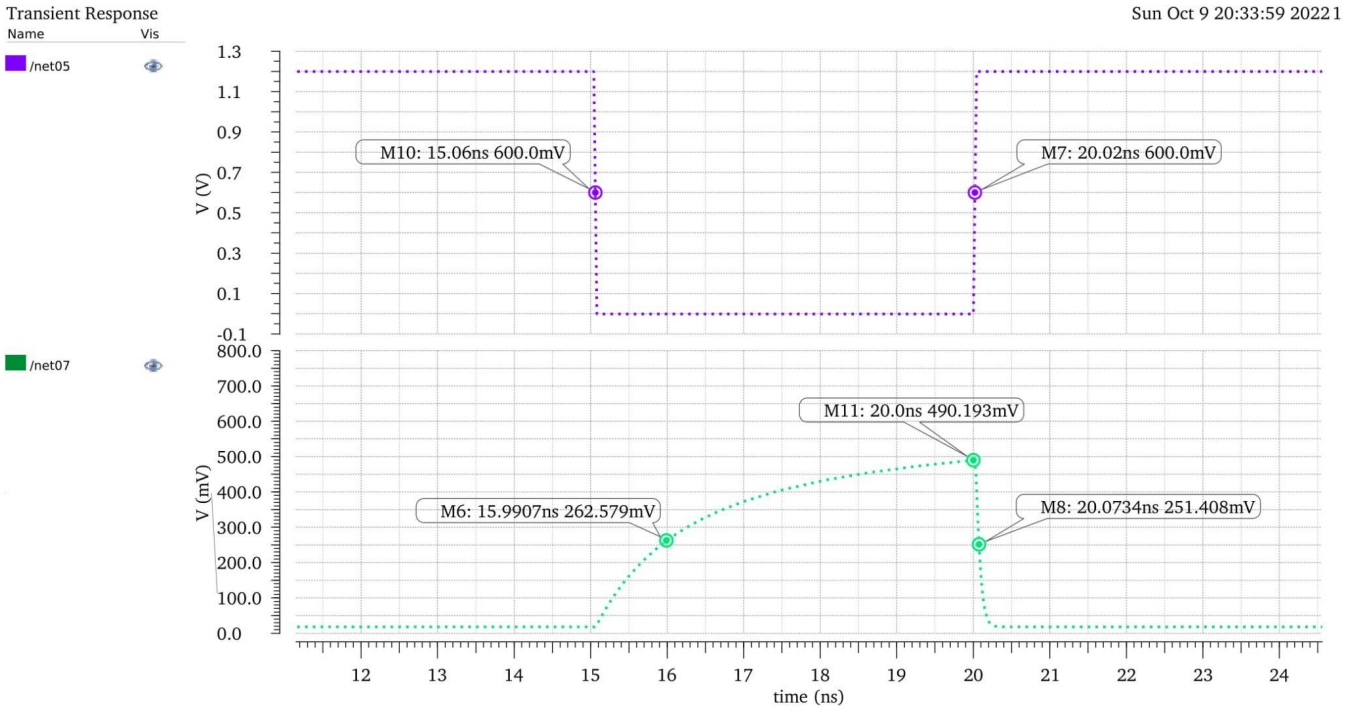

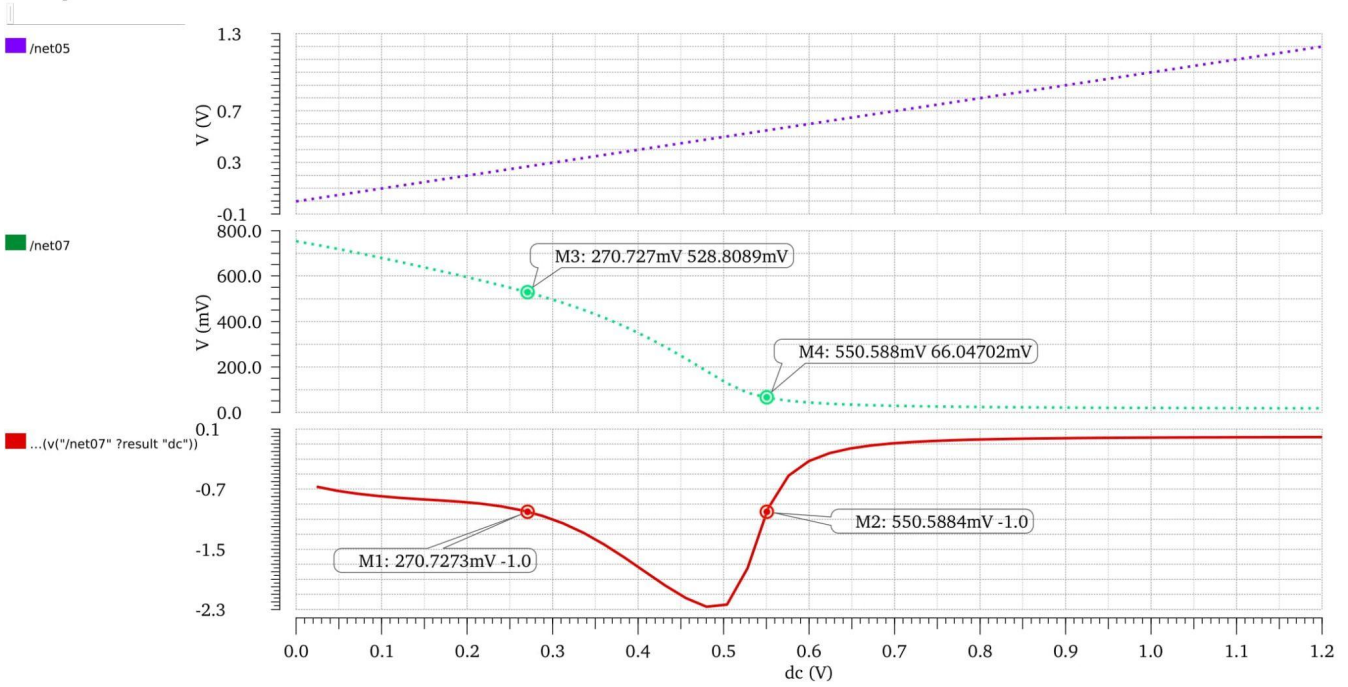
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/net07
...(v("/net07" ?result "dc"))
V (V)
V (mV)
M1: 270.7273mV -1.0
M2: 550.5884mV -1.0
M3: 270.727mV 528.8089mV
M4: 550.588mV 66.04702mV
dc (V)