1) Explain in your own words the variation of the DC output voltages VOH and VOL for the four inverters? In particular focus on the differences noted earlier in the NFET connected inverters and explain in your own words the variation of the switching times for all the inverters?

In terms of the output voltage, CMOS yields the highest voltage of 1.2V and CMOS long channel also almost yields the same. NFET yields an output voltage of —V and resistive load inverters, Von = –V. In all the three models, the long channel inverters yield more output voltage because of the more conductivity of electrons freely in long channels. Difference in NFET inverters is due to the NMOSFET connected to both VDD and ground and there is no PMOS in the inverter circuit. Variation in switching time in inverters is due to MOSFET, channels, resistors and switching in these inverter circuits are controlled by the power utilization lines.

2) List out the major drawbacks and benefits of using a NFET load and resistor for signal inversion from area, VTC (Voltage Transfer Characteristic), noise margin, leakage and fabrication point of view. Why do you think CMOS has become so popular in recent times?

The benefit of using a NFET load is the area that it uses, it will use the same lengths and widths for both transistors which improves the performance of the circuit. NFETs have nMOS which are faster than the pMOS in the circuits. There are two different kinds of NFETs, there is Enhancement and Depletion load - Enhancement can be operated in either that saturation or linear. The drawback of the Enhancement is that an nMOS is connected to a power source which creates a leakage in the system.
CMOS has become popular in recent times because they are lower in cost and easier to manufacture.

3) What happens if PMOS and NMOS are interchanged in an inverter connection? Where should you measure the output to get the desired inverted signal after interchanging their positions? What are the roles and responsibilities of each member of your lab team? Who did what part of the lab?

If the pMOS and nMOS are interchanged, it will create undesirable results - it will create degraded results. The reason why it would create degraded results is because nMOS can only pass a strong 0 and not a strong 1. So, if nMOS is connected to VDD, it will not output a strong VDD, it will output a degraded VDD. Vice versa for pMOS - it only outputs a strong 1 and not a strong 0.

4) What are the roles and responsibilities of each member of your lab team? Who did what part of the lab?
Jesus - CMOS simulations, Lab report
Mehul - NFET simulations, Lab report
Juan - Resistor Simulations, Lab report