Inverter

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Group 28
12/02/2022

Introduction and Physical Properties

Cell Description

The Static CMOS Inverter has a pMOS and nMOS that are connected in series. Both the nMOS and pMOS receive the same input. The output depends on the input; if the nMOS is turned ON from the input, the output will be LOW. pMOS will be the opposite of an nMOS

Cell Symbol

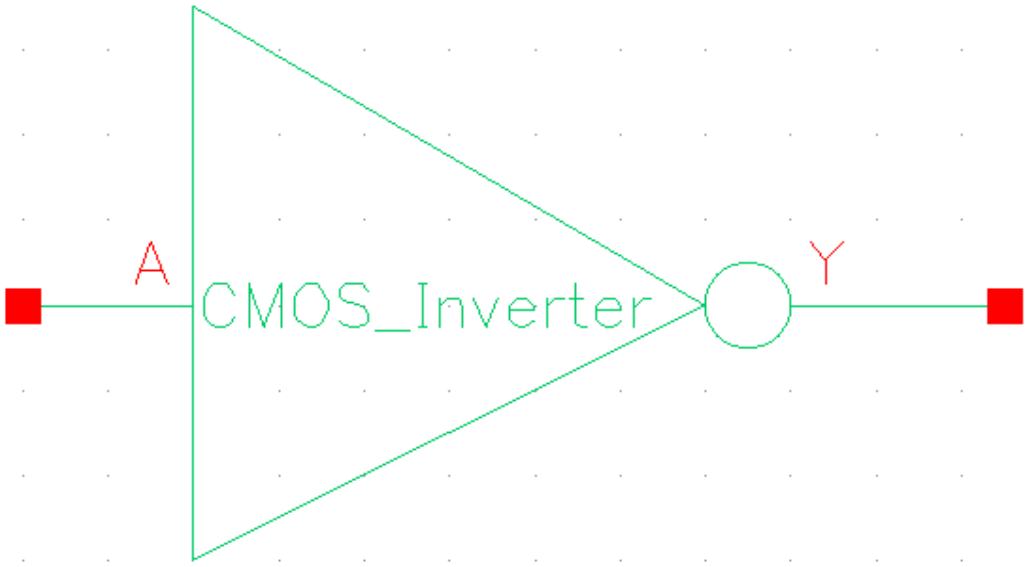

Figure 1: Example Logic Symbol for a CMOS Inverter.

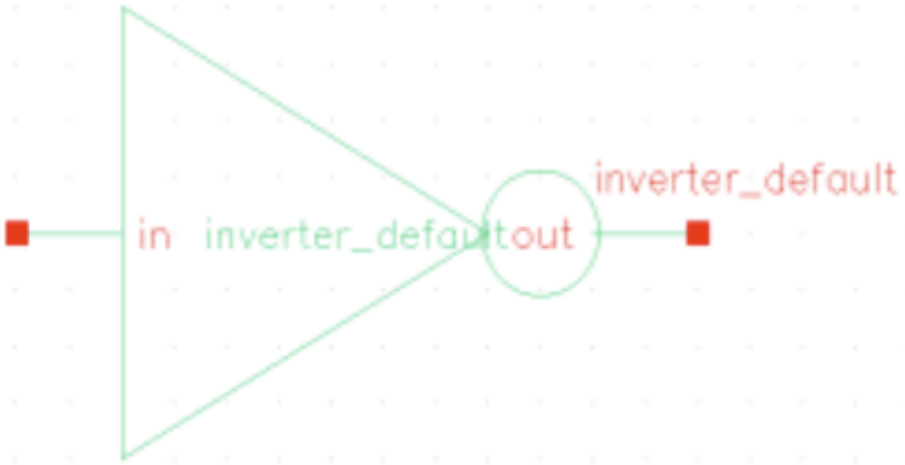

Figure 2: Schematic Diagram of Inverter symbol which is used as DUT.

Cell Truth Table

The truth table of the CMOS Inverter is shown below - when the CMOS inverter receives a LOW (0), the output will be a HIGH (1). When the Inverter receives a HIGH (1), it will output a LOW (0)

CMOS Inverter Truth Table	
Cell Inputs {0,1}	Cell Outputs {0,1} Y
0	1
1	0

Cell Schematic Diagram

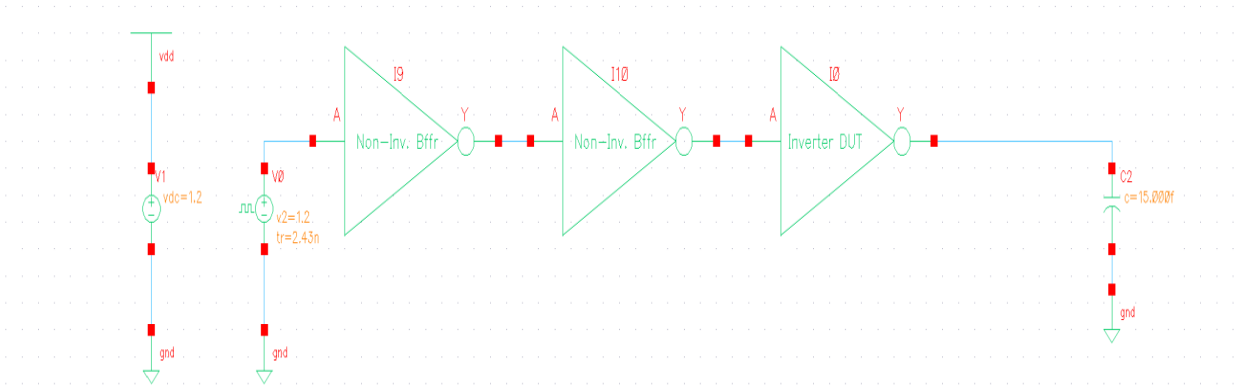

Figure 3: Schematic Diagram of DUT with Fanout of 0

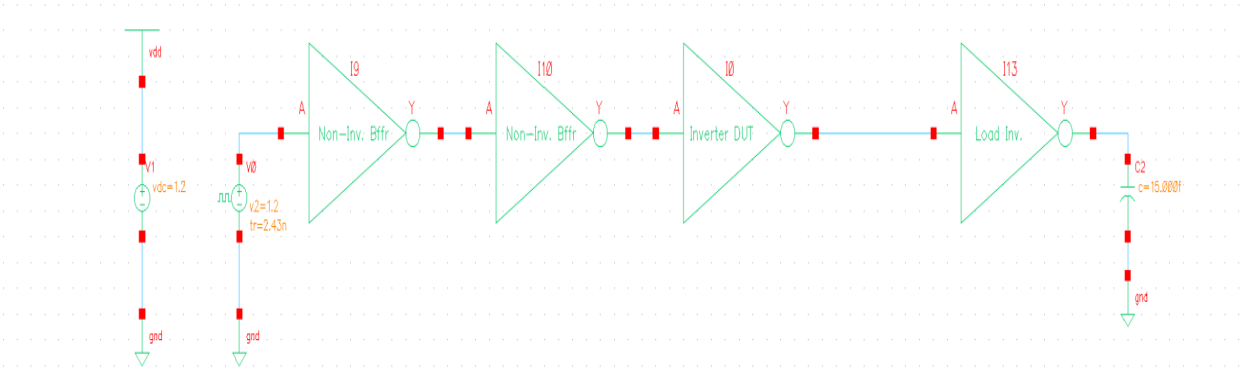

Figure 4: Schematic Diagram of DUT with Fanout of 1

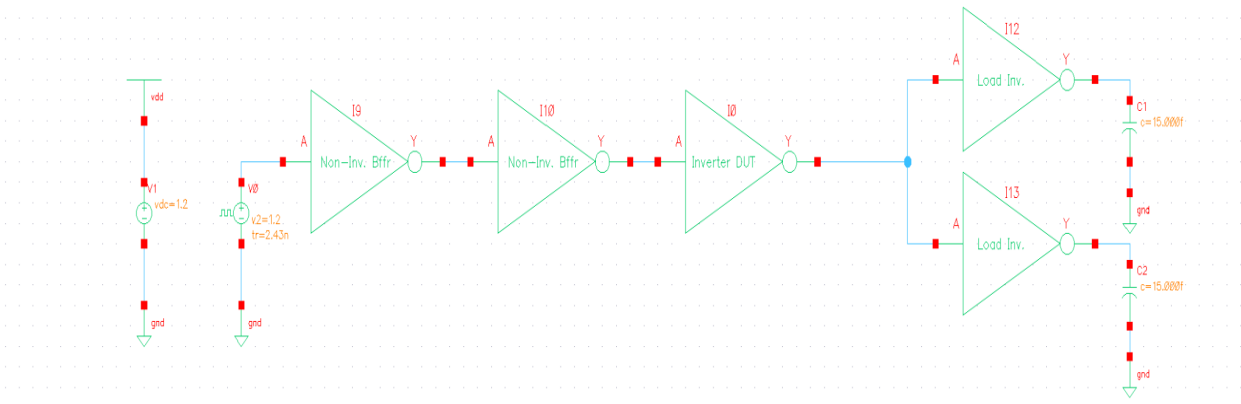

Figure 5: Schematic Diagram of DUT with Fanout of 2

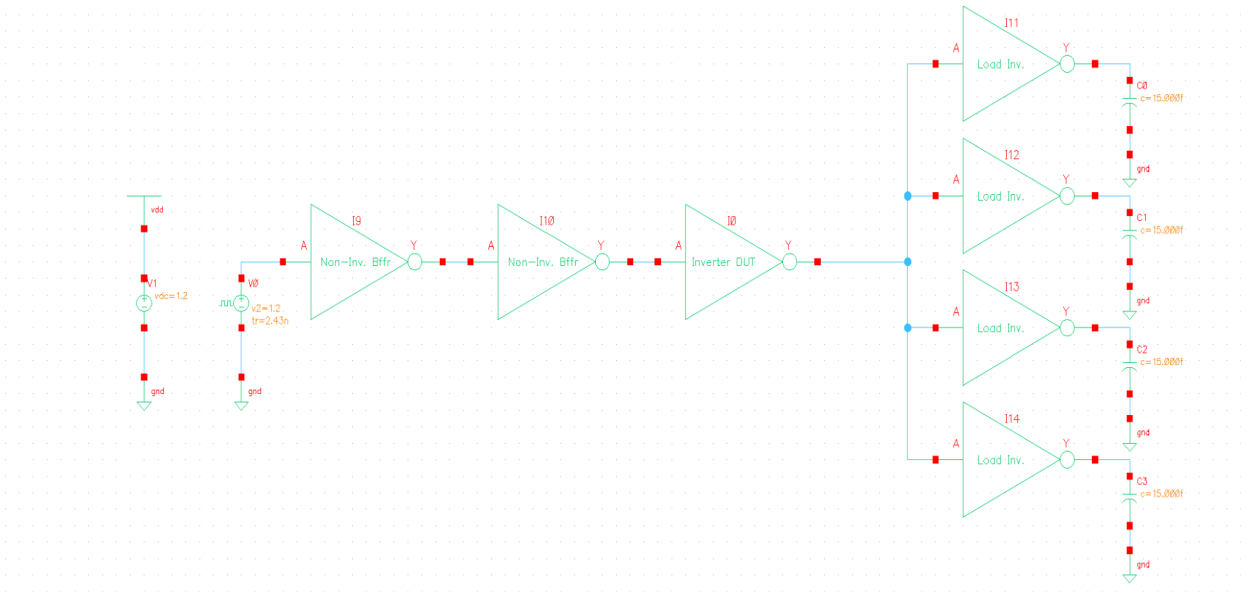

Figure 6: Schematic Diagram of DUT with Fanout of 4

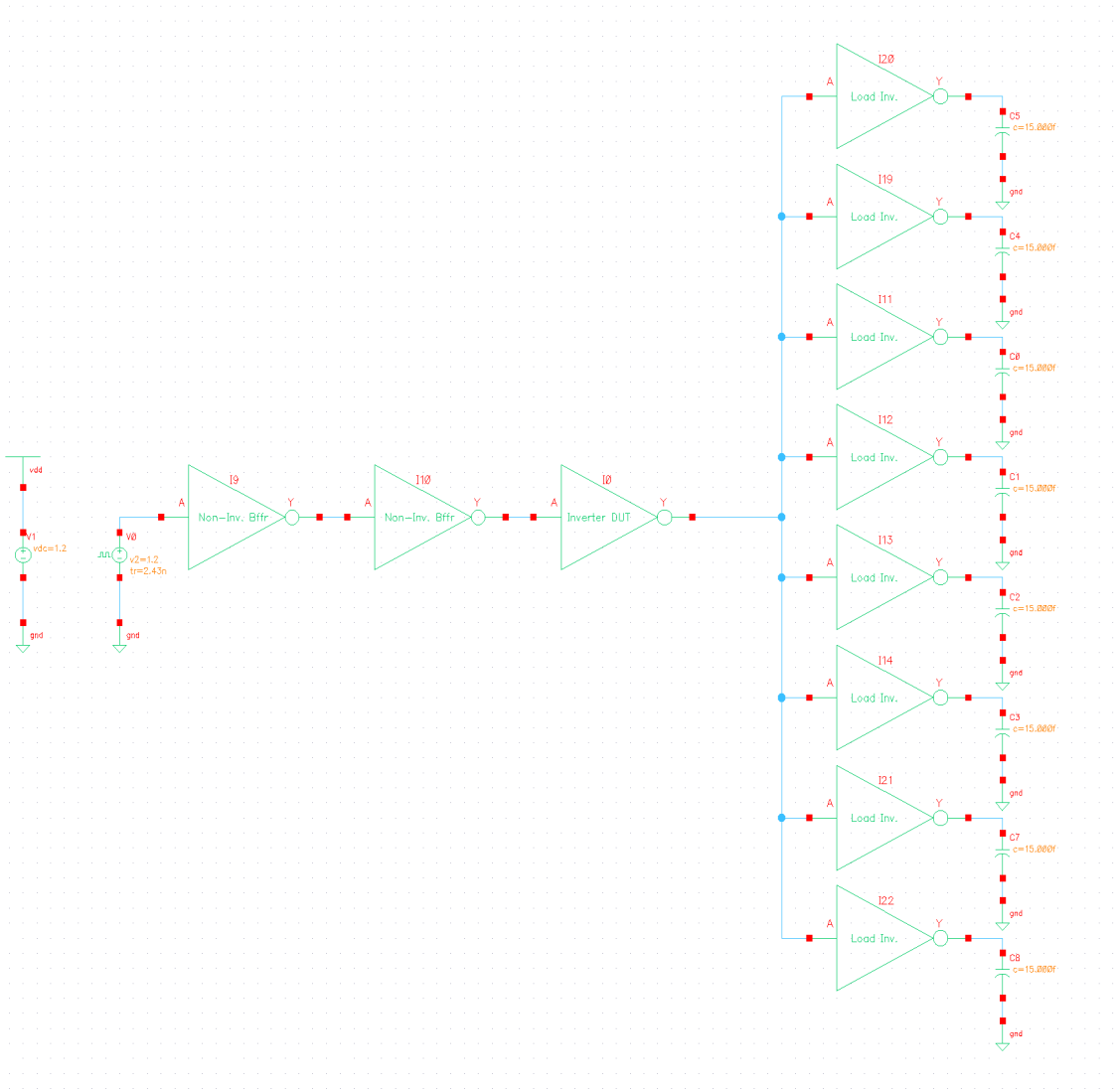

Figure 7: Schematic Diagram of DUT with Fanout of 8

Cell Layout Diagram and Dimensions

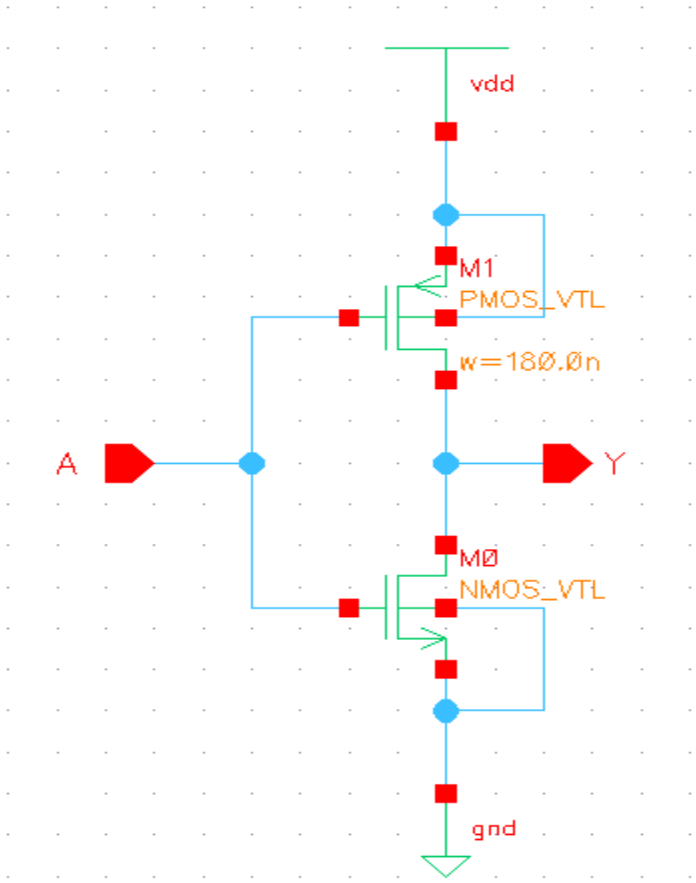

Figure 8: Layout diagram of DUT inverter

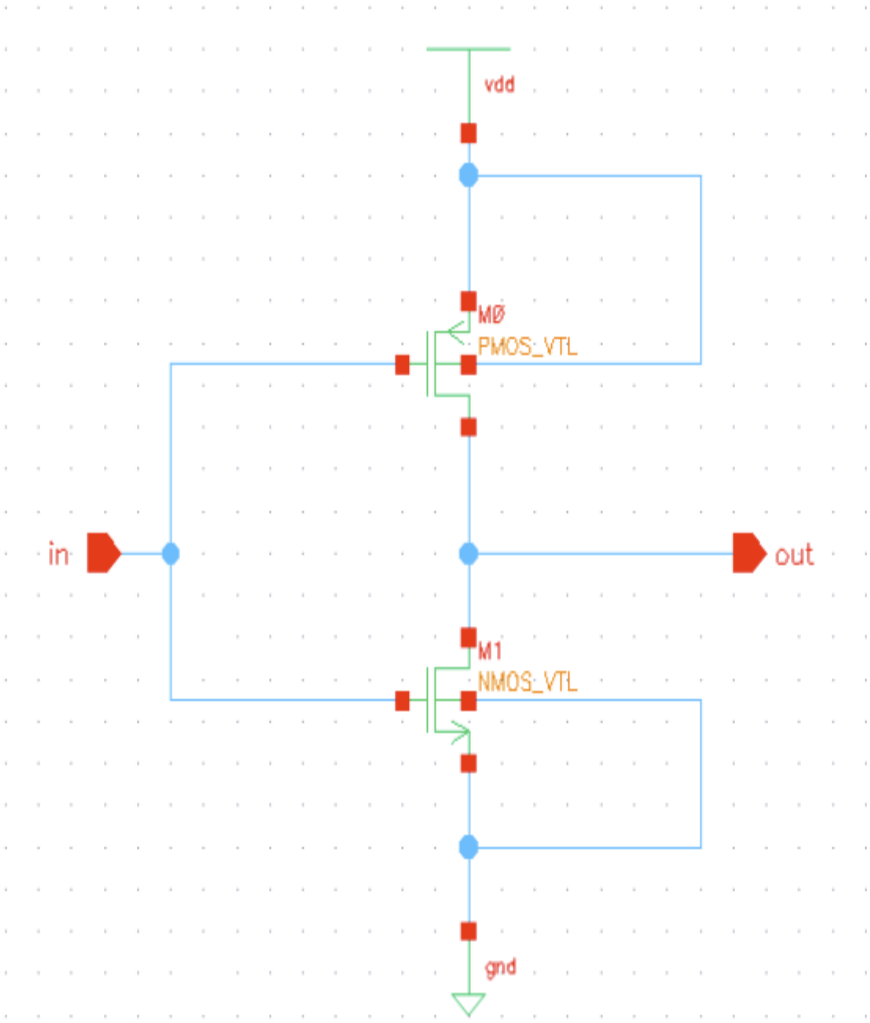

Figure 9: Layout diagram of inverter with minimum dimensions

Transistor Dimensions (DUT)		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS	50	90
PMOS	90	180

Transistor Dimensions (load and non inverting buffer)		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS	50	90
PMOS	50	90

Performance Analysis

FO4 Initial Simulation Results:

CMOS Inverter PMOS/NMOS Width Variation					
DUT		**Rise/Fall & Delay Times (ps)**			
Wp (nm)	Wn (nm)	T_R	T_F	T_{PLH}	T_{PHL}
90	90	34.92	19.44	13.81	35.87
90	135	35.52	17.93	8.84	37.51
135	90	27.12	19.94	15.1	28.43
180	90	24.21	20.68	16.112	24.4267

Experimental Values (RED = out of spec)

After thorough simulation, the team decided that having a PMOS size double of an NMOS provided the best results. There was a smaller delta between the Propagation Delays and a better Rise/Fall times.

Rise and Fall Times

Input X: Output Rise Time Data t_r (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	188.1	17.23	19.65	24.21	32.3

Stack Input Combination: ***Replace with Boolean Product***

Stack S, Input X: Output Fall Time Data t_f (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	117.4	15.84	17.33	20.68	25.54

Stack Input Combination: ***Replace with Boolean Product***

Propagation Delays

Data Worst Case Low to High Propagation Delay Data t_{plh} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	101.35	9.167	19.078	16.112	23.112

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	139.34	16.975	21.252	24.4267	32.351

Worse Case Input Combination: ***Replace with Boolean Product***

Conclusion:

We chose the PMOS and NMOS widths to both be 180nm and 90nm respectively. We made this choice because it gave simulation results for tr, tf, tplh, and tphl which fit within the given specifications better as seen in the 'Performance Analysis'. The specifications the team was looking for were closer rise/fall times and to have the least difference between TPLH and TPHL. This will contribute to better performance compared to the other width sizes.

Please answer the following question:

What are the roles and responsibilities of each member of your lab team? Who did what part of the lab? Please list the individual contribution to the lab.

Jesus worked on CMOS compound gate schematics, simulations and worked on the report.
Juan made the schematics and ran simulations for the CMOS inverter and made the report template.
Mehul ran the simulations for the CMOS inverter and worked on the report.

Transient Simulation Plots:

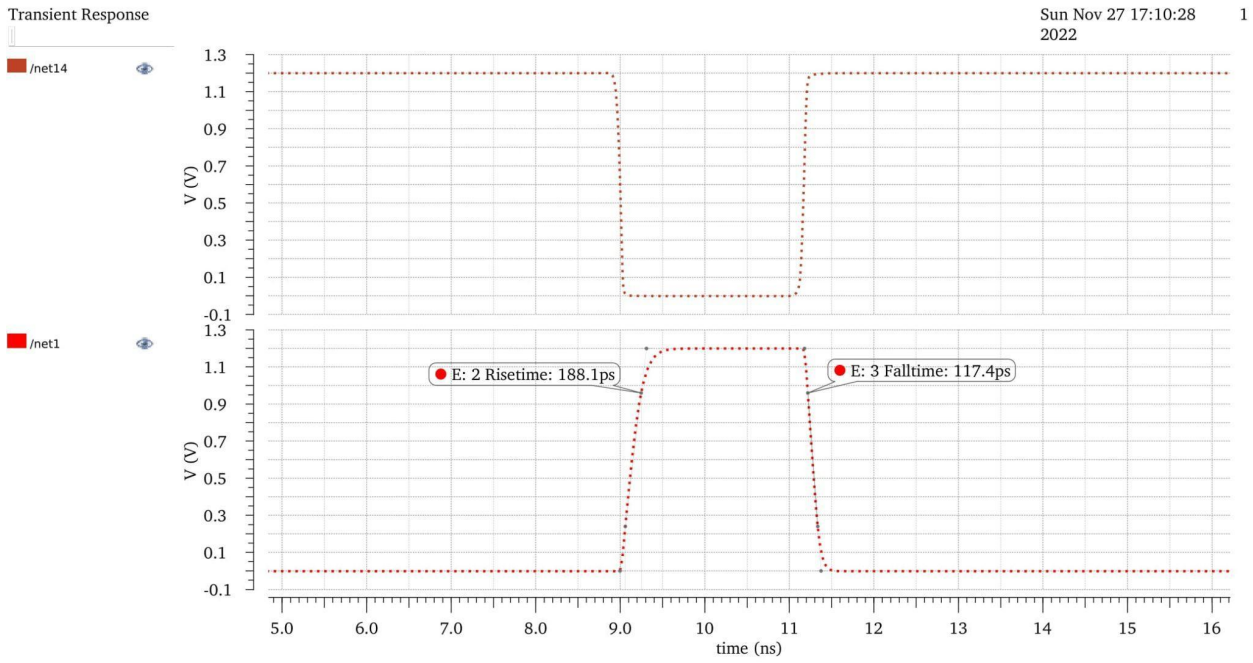

Figure 10: Rise/Fall time of Fanout 0

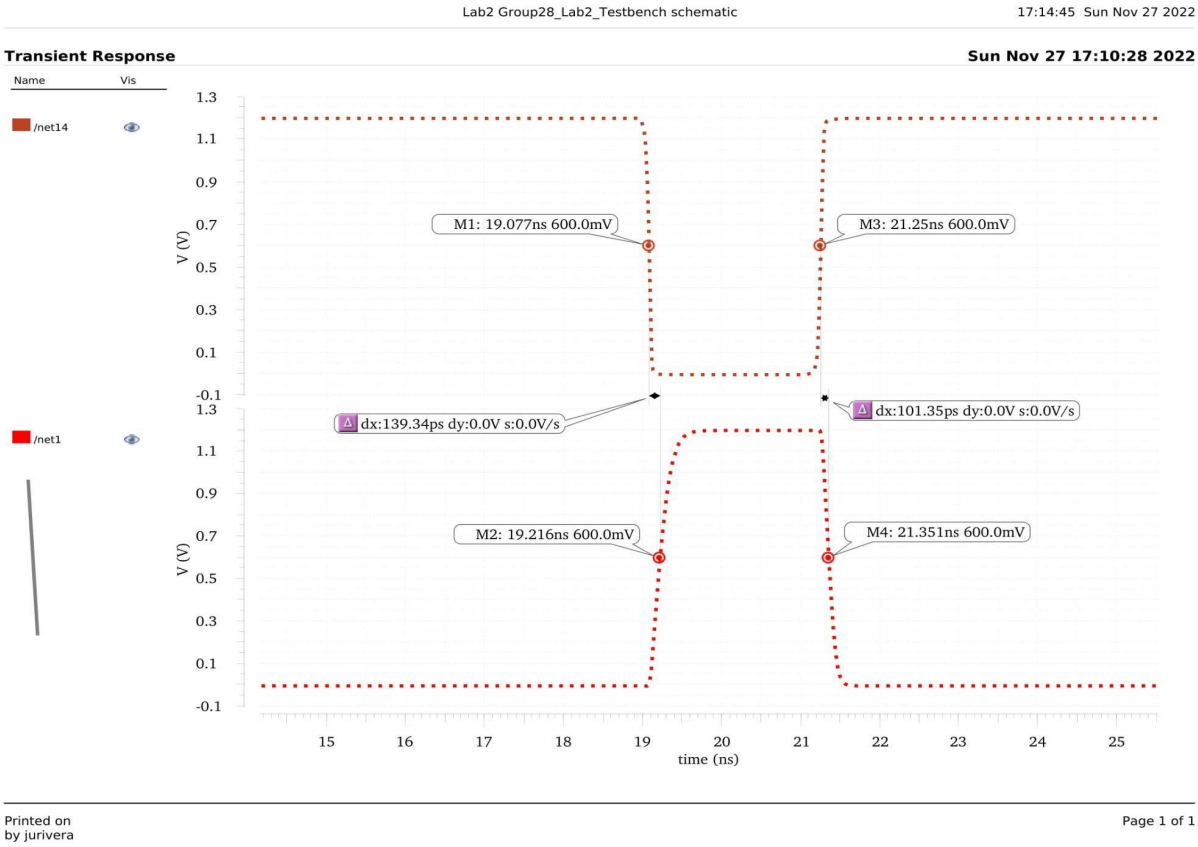

Figure 11:Propagation Delay of Fanout 0

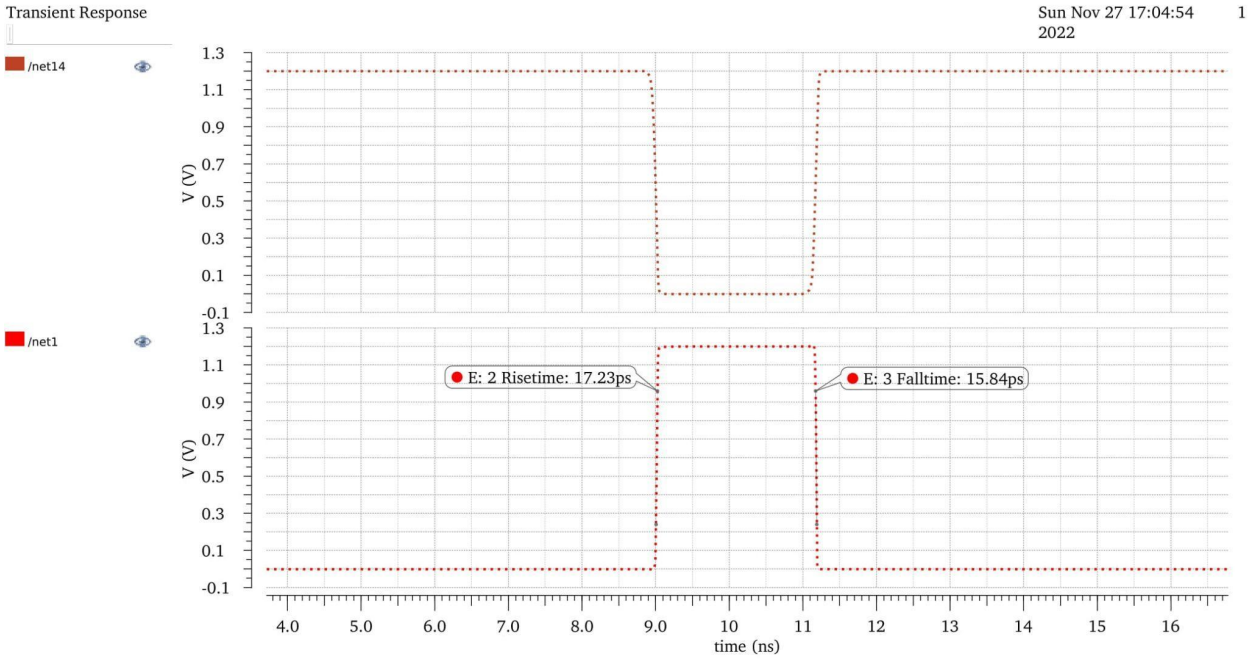

Figure 12: Rise/Fall time of Fanout 1

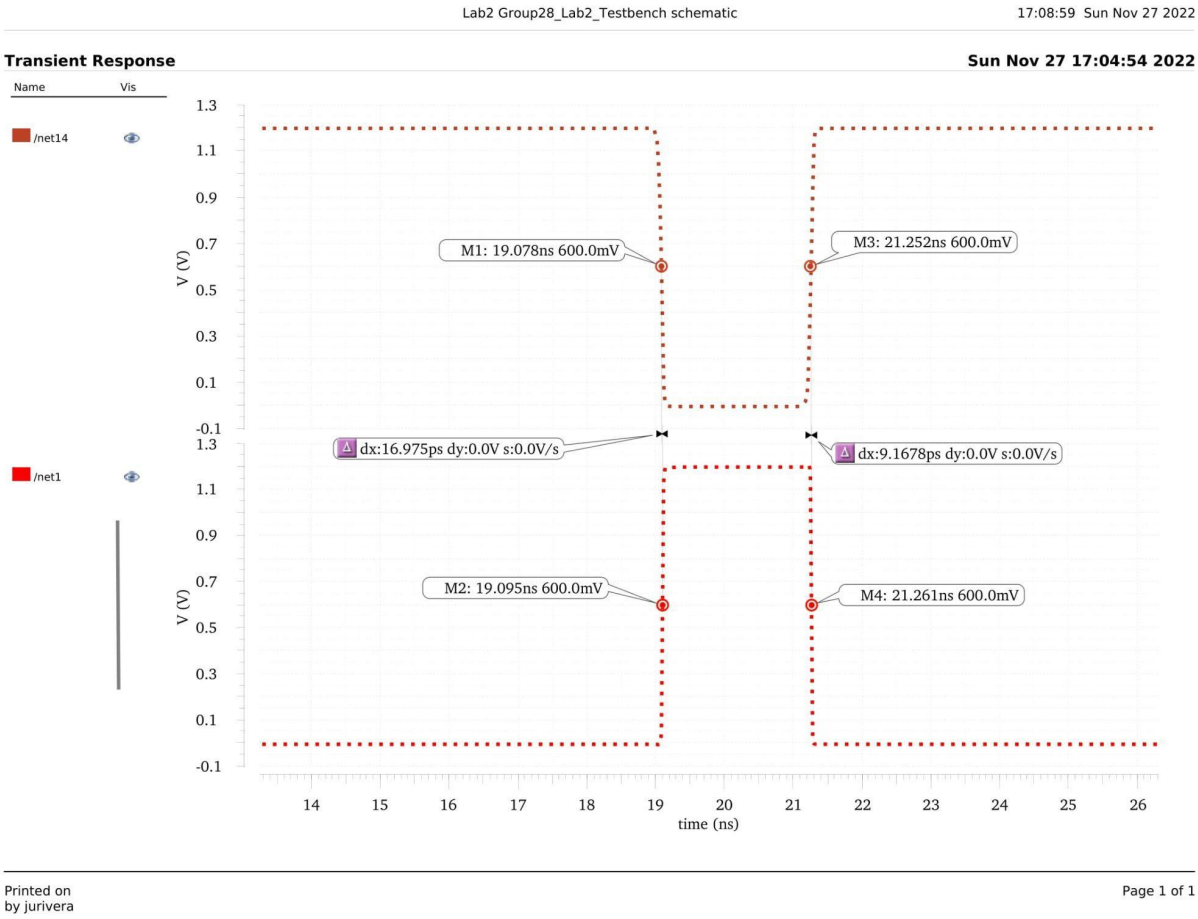

Figure 13:Propagation Delay of Fanout 1

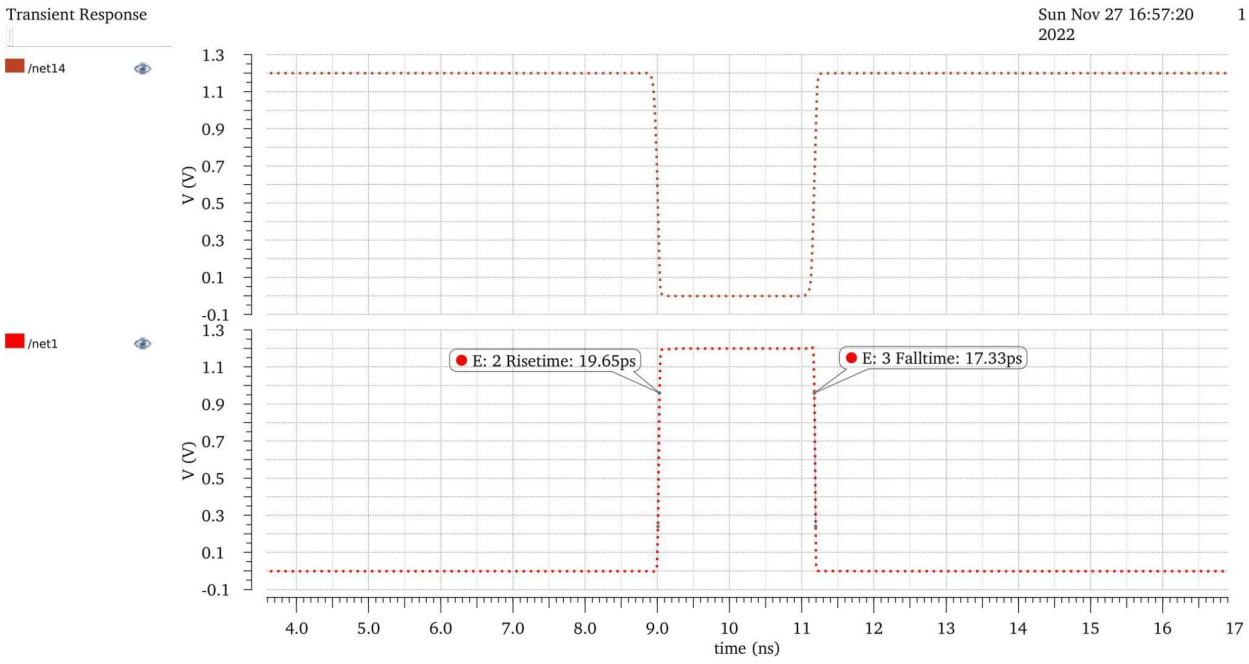

Figure 14: Rise/Fall time of Fanout 2

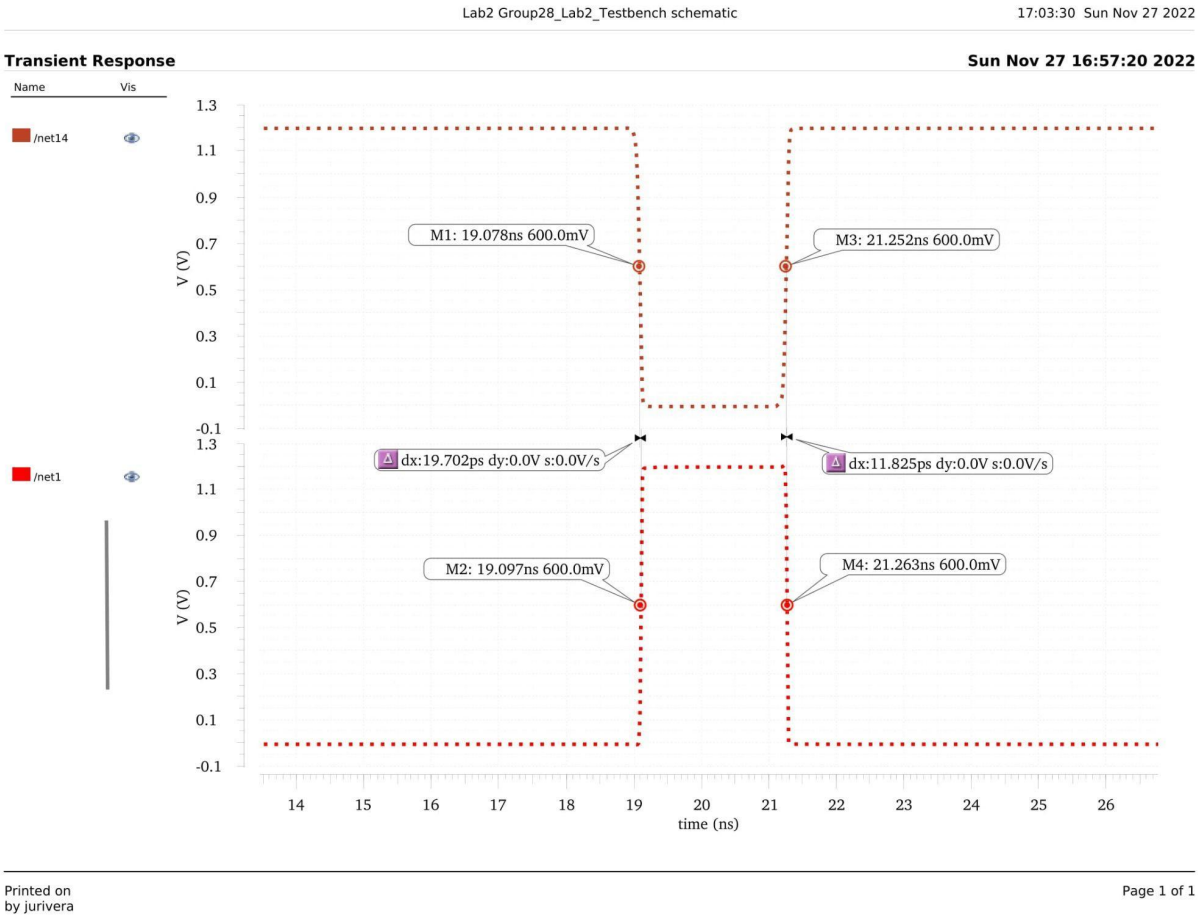

Figure 15:Propagation Delay of Fanout 2

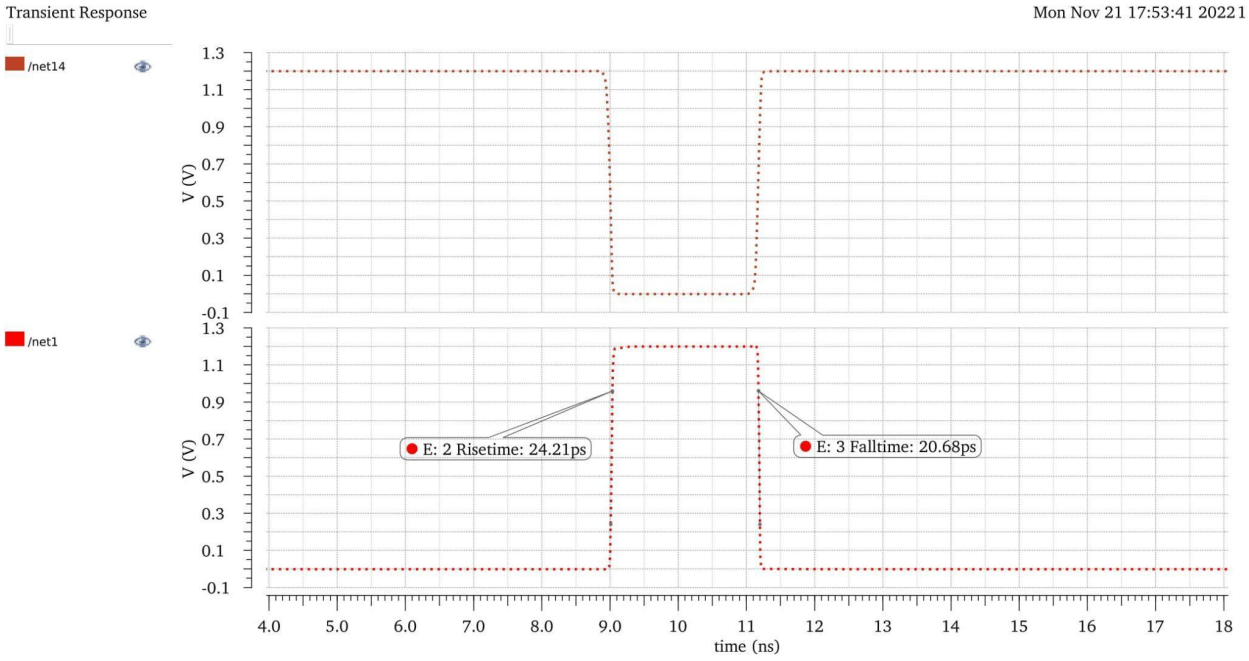

Figure 16: Rise/Fall time of Fanout 4

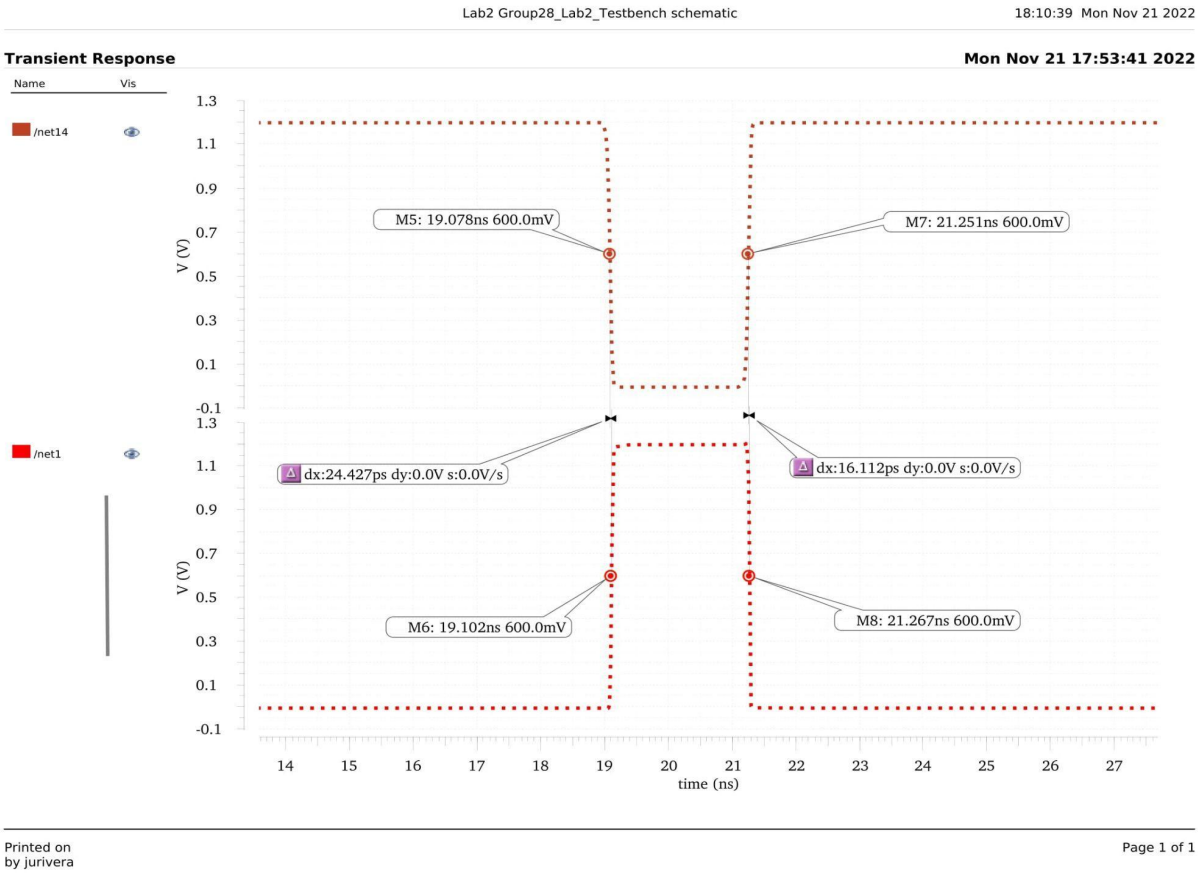

Figure 17:Propagation Delay of Fanout 4

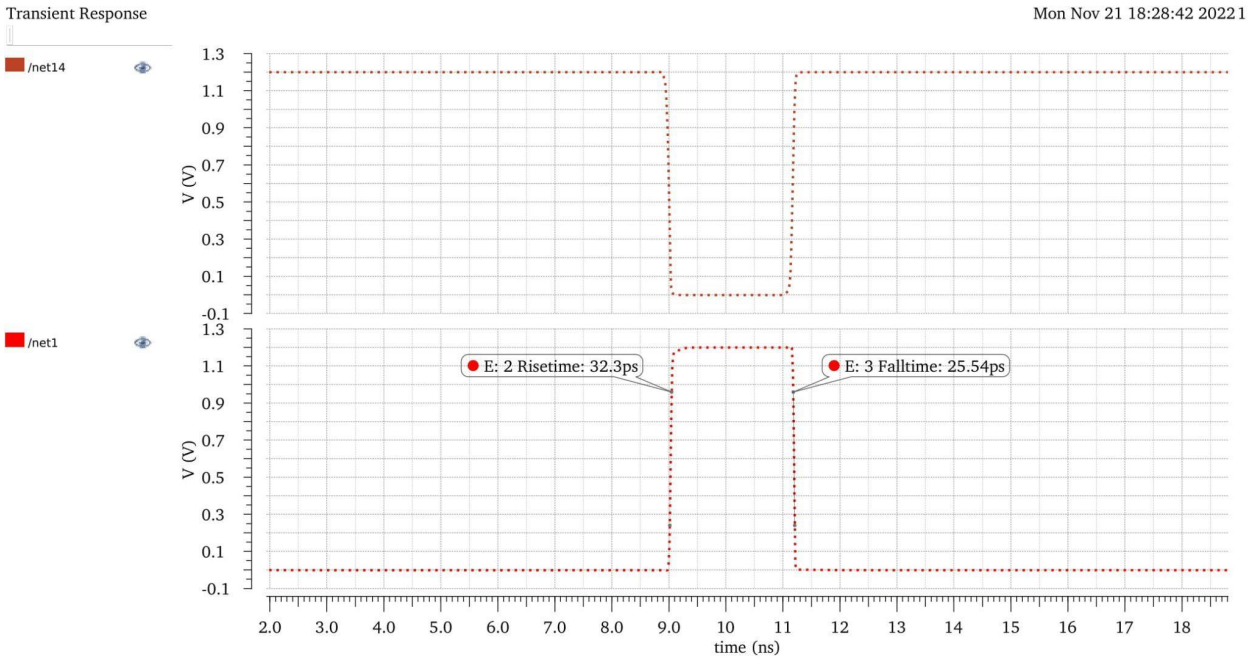

Figure 18: Rise/Fall time of Fanout 8

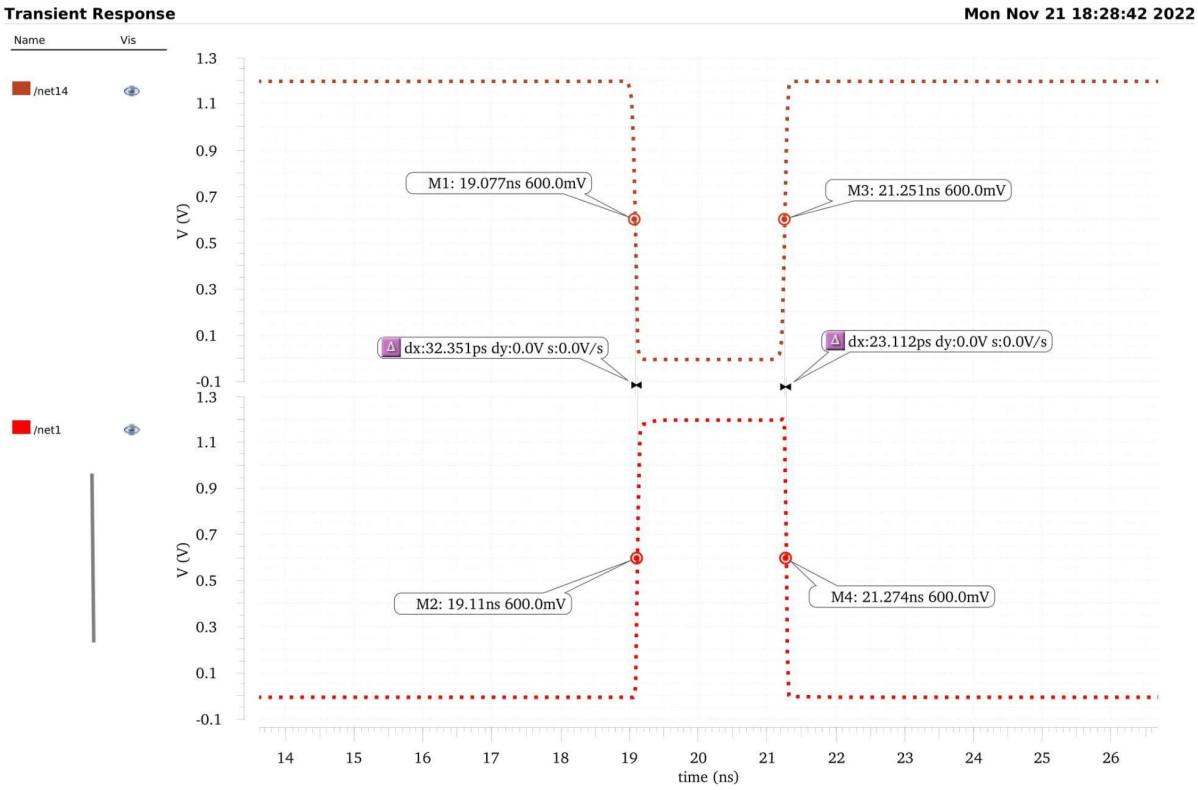

Figure 19:Propagation Delay of Fanout 8

Compound Gate

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12/02/2022

Introduction and Physical Properties

Cell Description

The 3 input NAND gate has three inputs and one output. The logic gate is constructed out of 3 PMOS in parallel and 3 NMOS in series. . The way that the gate functions is, if all the inputs were 1, which turns ON all the NMOS while turning OFF all the PMOS, the output will be 0. To get an output of 1, only one input has to be 0 in order to turn on one of the PMOS. The Boolean expression of the logic NAND gate is defined as the binary operation dot(.)

Cell Symbol

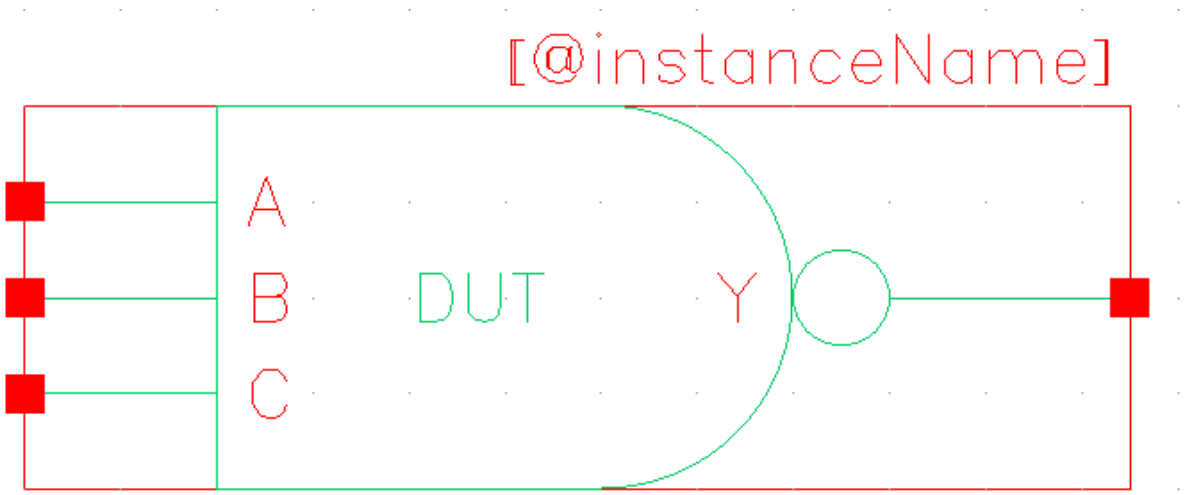

Figure 1: 3-input NAND gate .

The Output of the circuit is:

$$Y = \overline{A \cdot B \cdot (B \cdot C + D) \cdot C}$$

Reducing the equation for **NMOS Stack**:

$$\begin{aligned}
Y &= \overline{A \cdot B \cdot (B \cdot C + D) \cdot C} \\
Y &= \overline{A \cdot B \cdot C \cdot (B \cdot C + D)} \\
Y &= \overline{A \cdot B \cdot C \cdot (B \cdot C) + A \cdot B \cdot C \cdot D} \\
Y &= \overline{A \cdot B \cdot C + A \cdot B \cdot C \cdot D} \\
Y &= \overline{A \cdot B \cdot C \cdot (1 + D)} \\
Y &= \overline{A \cdot B \cdot C}
\end{aligned}$$

For **PMOS Stack** :
Reduced Equation:

$$Y = \bar{A} + \bar{B} + \bar{C}$$

So, the Compound Gate is a **3-input NAND gate.**

Cell Truth Table

CMOS Inverter Truth Table			
Cell Inputs {0,1}	Cell Inputs {0,1}	Cell Inputs {0,1}	Cell Outputs {0,1} Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Cell Schematic Diagram

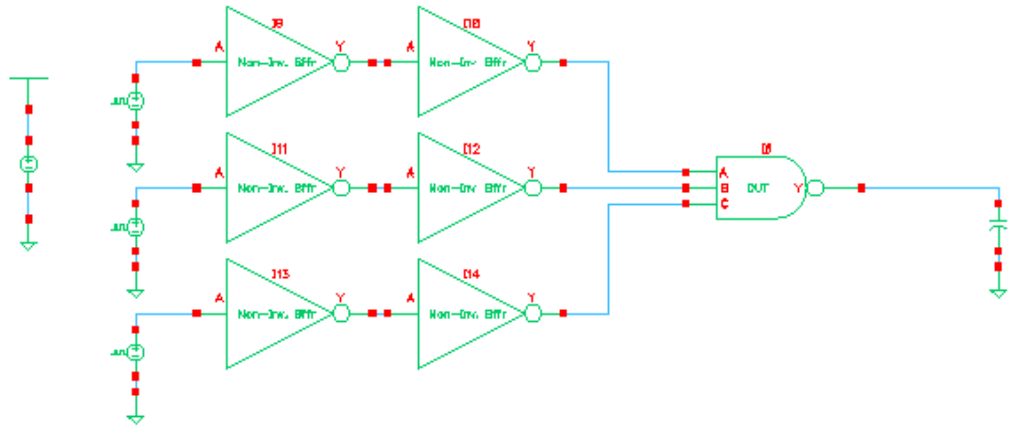

Figure 2 : Schematic diagram of compound gate for fanout 0

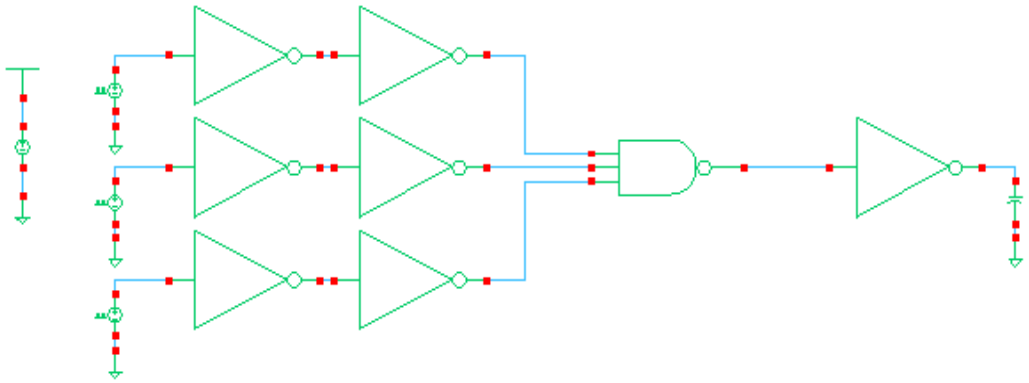

Figure 3 : Schematic diagram of compound gate for fanout 1

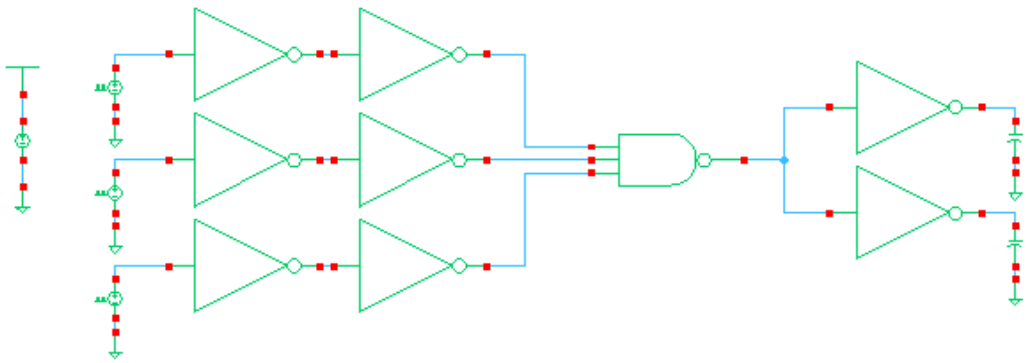

Figure 4 : Schematic diagram of compound gate for fanout 2

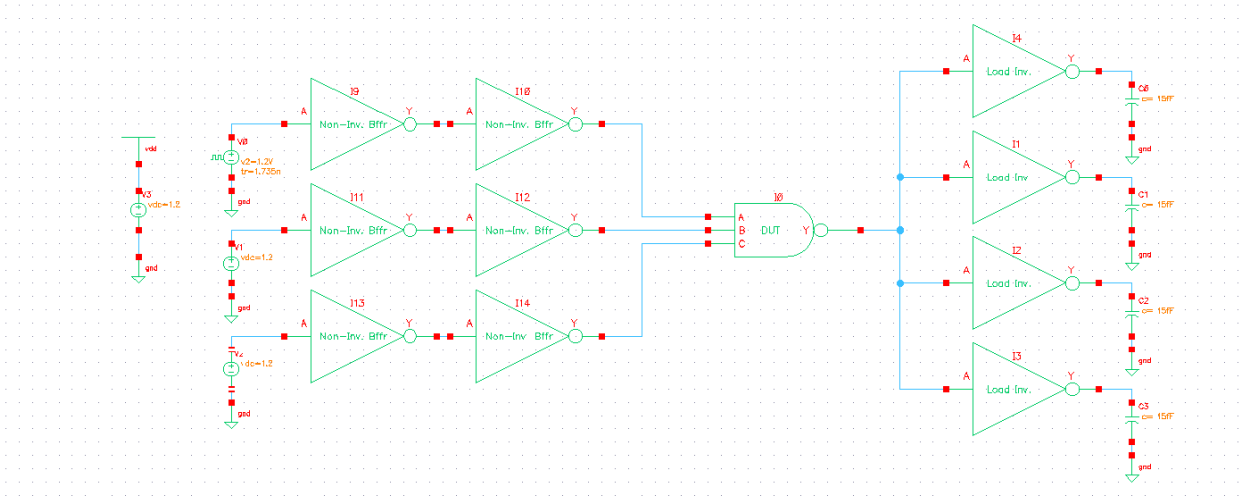

Figure 5 : Schematic diagram of compound gate for fanout 4 Input A varies BC

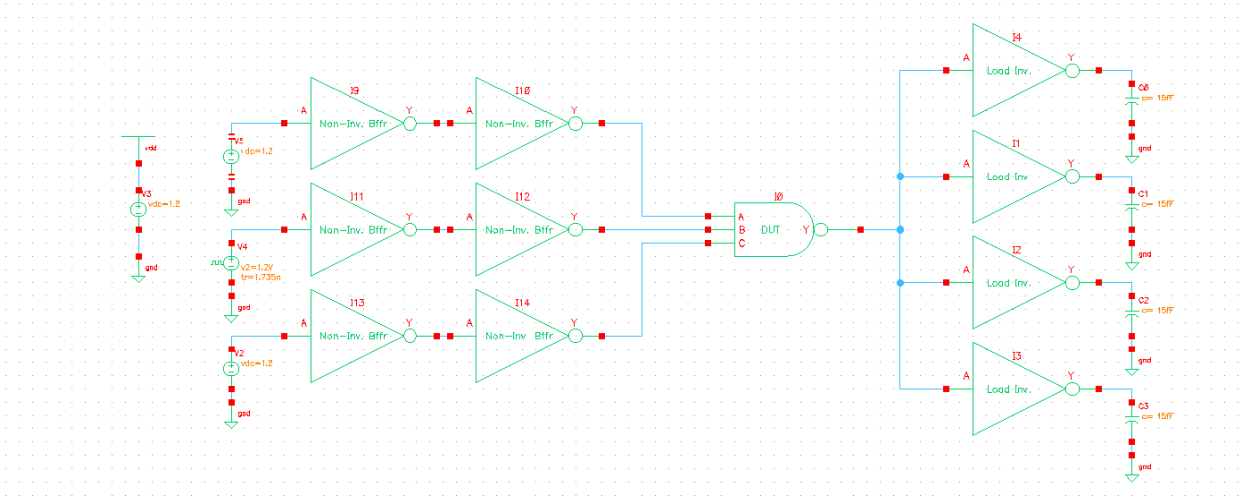

Figure 6 : Schematic diagram of compound gate for fanout 4 Input B varies AC

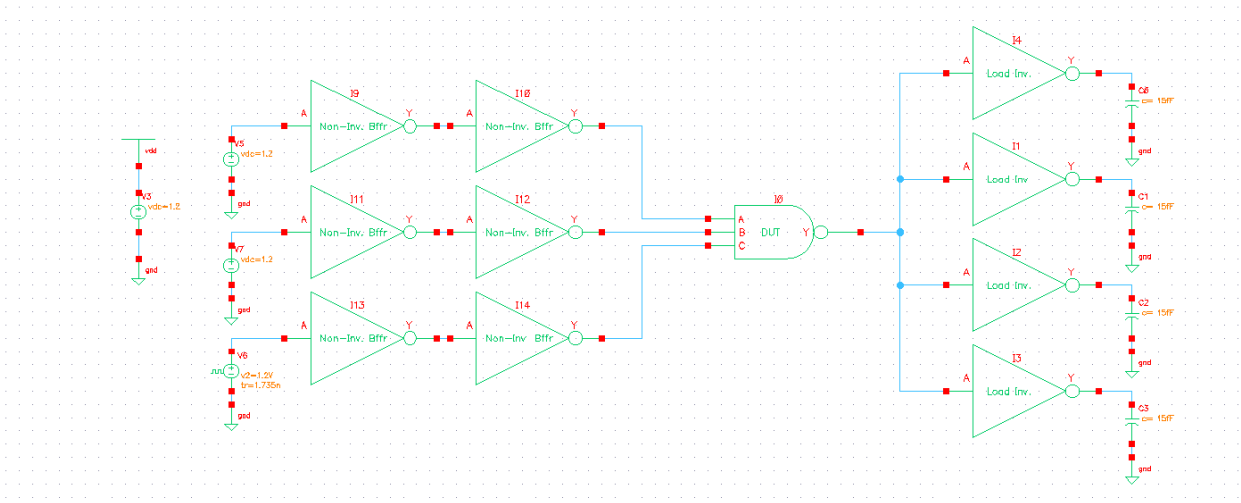

Figure 7 : Schematic diagram of compound gate for fanout 4 Input C varies AB

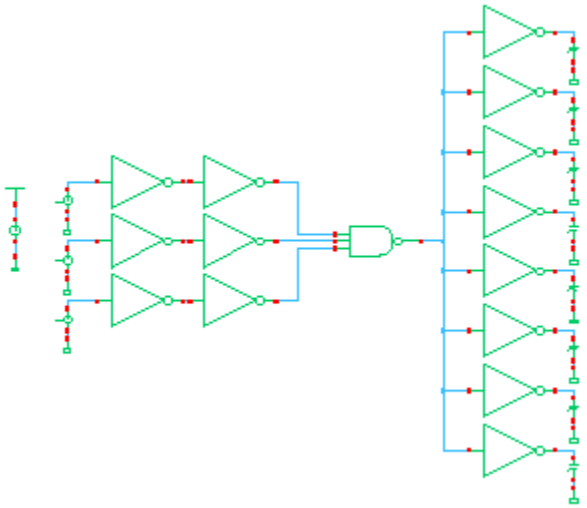

Figure 8 : Schematic diagram of compound gate for fanout 8

Cell Layout Diagram and Dimensions

Cell Layout Diagram:

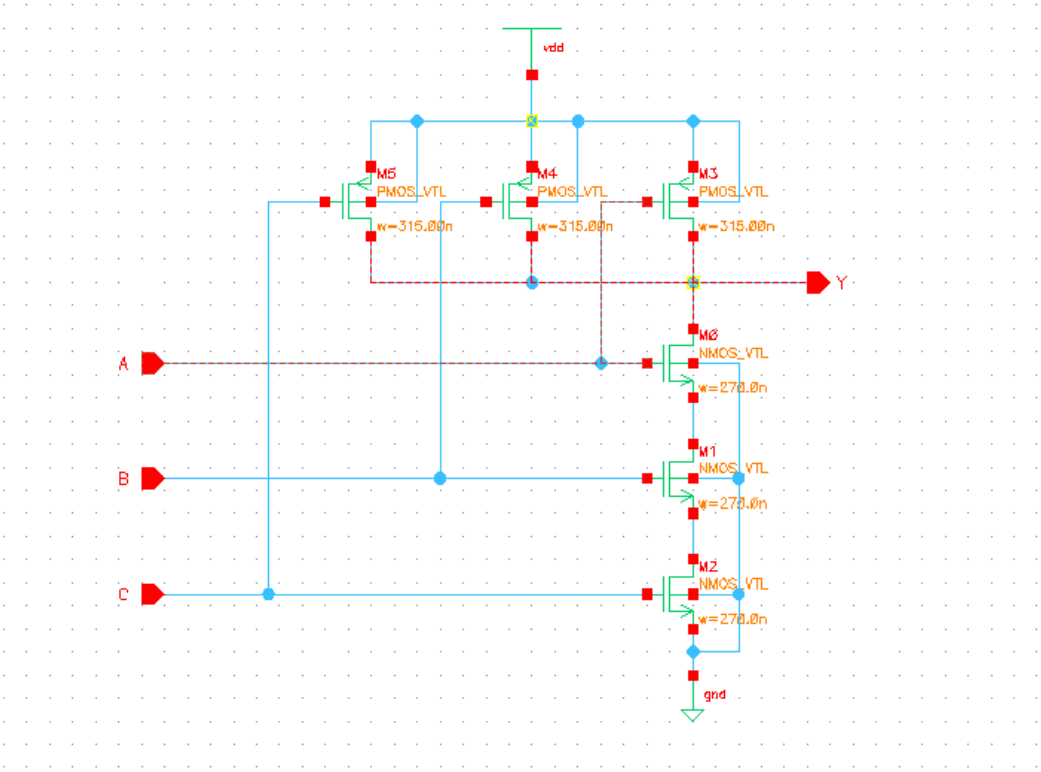

Figure 9 : Schematic diagram of DUT Transistor configuration for a NAND gate

Transistor Dimensions (DUT)		
Transistor Instance Number	Length (nm)	Width (nm)
PMOS	50	315
NMOS	50	270

Transistor Dimensions (Input Buffer and Output Load)		
Transistor Instance Number	Length (nm)	Width (nm)
PMOS	50	90
NMOS	50	90

Performance Analysis

Rise and Fall Times - Input A

Input X: Output Rise Time Data t_r (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	113.0	20.71	21.57	23.97	28.6

Stack Input Combination: ***Replace with Boolean Product***

Stack S, Input X: Output Fall Time Data t_f (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	98.59	19.47	20.5	22.68	26.78

Stack Input Combination: ***Replace with Boolean Product***

Propagation Delays - Input A

Data Worst Case Low to High Propagation Delay Data t_{plh} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	89.698	20.845	22.179	24.785	29.385

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	82.316	14.652	16.038	18.419	22.237

Worse Case Input Combination: ***Replace with Boolean Product***

Rise and Fall Times - Input B

Input X: Output Rise Time Data t_r (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	114.8	22.49	23.62	25.85	30.69

Stack Input Combination: ***Replace with Boolean Product***

Stack S, Input X: Output Fall Time Data t_f (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	97.98	16.51	17.62	20.06	24.35

Stack Input Combination: ***Replace with Boolean Product***

Propagation Delays - Input B

Data Worst Case Low to High Propagation Delay Data t_{plh} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	92.656	25.146	26.351	28.54	33.008

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	84.397	17.066	18.344	20.764	25.239

Worse Case Input Combination: ***Replace with Boolean Product***

Rise and Fall Times - Input C

Input X: Output Rise Time Data t_r (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	117.8	24.59	25.77	28.11	32.98

Stack Input Combination: ***Replace with Boolean Product***

Stack S, Input X: Output Fall Time Data t_f (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	98.52	15.07	16.21	18.47	23.14

Stack Input Combination: ***Replace with Boolean Product***

Propagation Delays - Input C

Data Worst Case Low to High Propagation Delay Data t_{plh} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	95.738	28.389	29.573	31.721	35.996

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	82.833	16.686	17.847	20.103	24.312

Worse Case Input Combination: ***Replace with Boolean Product***

Conclusion:

Initial DUT conditions were the following:

pMOS width - 180, L - 50
nMOS width - 270, L - 50

With these conditions the FO4 rise/fall time delays were out of spec because the bottom two inputs (B, C) were taking too long to transition states, namely from low to high. The current model is that since there is additional diffusion capacitance on the A,B inputs when C is transitioning and there is extra time needed to charge/discharge the added load capacitance.

This model was reinforced with the rise/fall and delay measurements. Consistently, input C had longer rise/fall and delay values than the other two inputs. This fits the Elmor model delay since there is added diffusion capacitance in its path to the output.

Adjusting the value of the width of the DUT model by increasing the width of the pMOS from 180 nm to 315 nm helped to bring the rise/fall and delay values into spec. This was observed regardless of input being driven.

The shortest delay observed was that of the FO1, we believe this is because of the ratio of diffusion capacitance at the load to the input of a driving inverter.

CMOS Inverter PMOS/NMOS Width Variation					
DUT (Input C)		**Rise/Fall & Delay Times (ps)**			
Wp (nm)	Wn (nm)	T_R	T_F	T_{PLH}	T_{PHL}
180	270	36.03	15.51	42.489	16.786
315	270	28.11	18.47	31.721	20.103

Experimental Values (RED = out of spec)

We can see that from the default width values the rise/fall and delay values are out of spec. Increasing in increments of 45 nm to find the final value resulted in all the spec being met.

Please answer the following question:
What are the roles and responsibilities of each member of your lab team? Who did what part of the lab? Please list the individual contribution to the lab.

Jesus worked on CMOS compound gate schematics, simulations and worked on the report.
Juan made the schematics and ran simulations for the CMOS inverter and made the report template.
Mehul ran the simulations for the CMOS inverter and worked on the report.

Transient Simulation Plots:

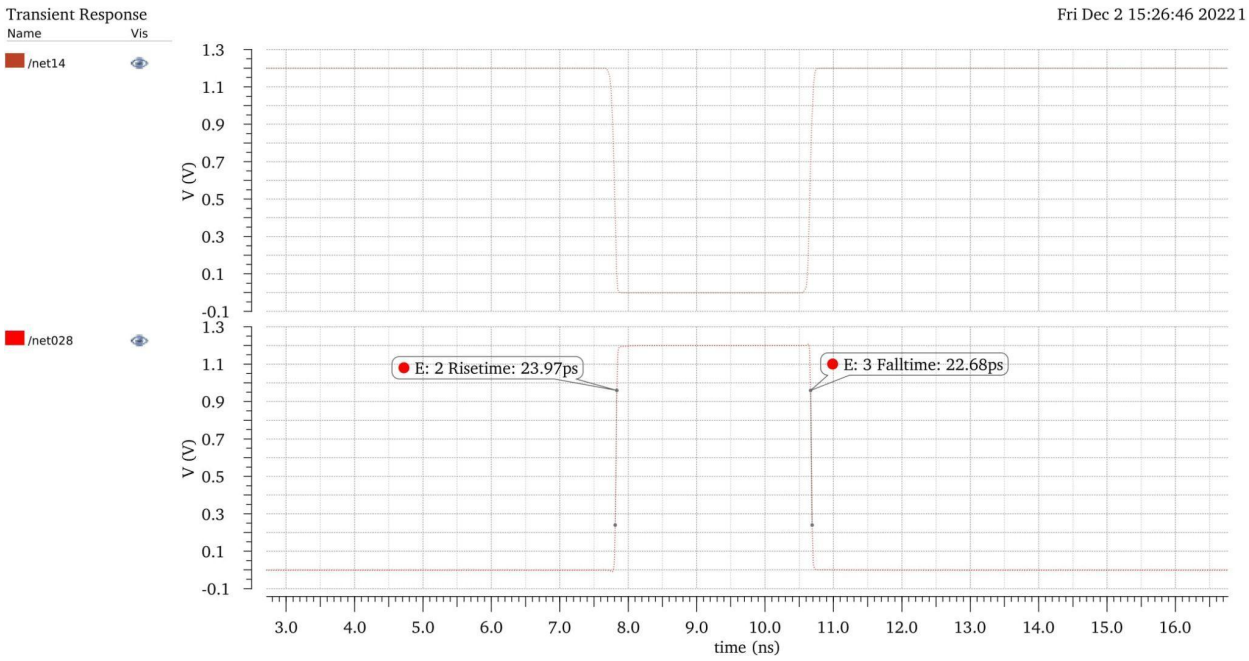

Figure 10: Input A Rise/Fall time of Fanout 4

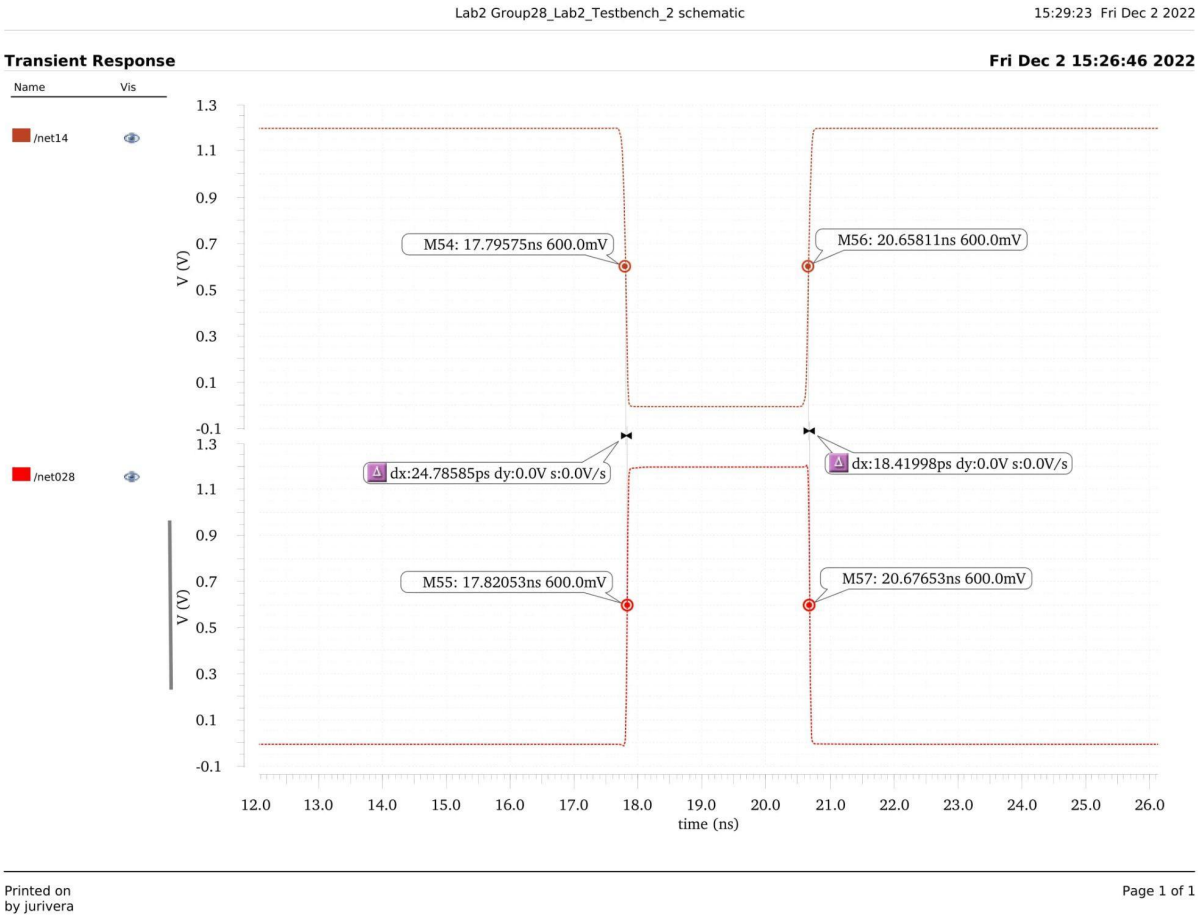

Figure 11: Input A Propagation Delay time of Fanout 4

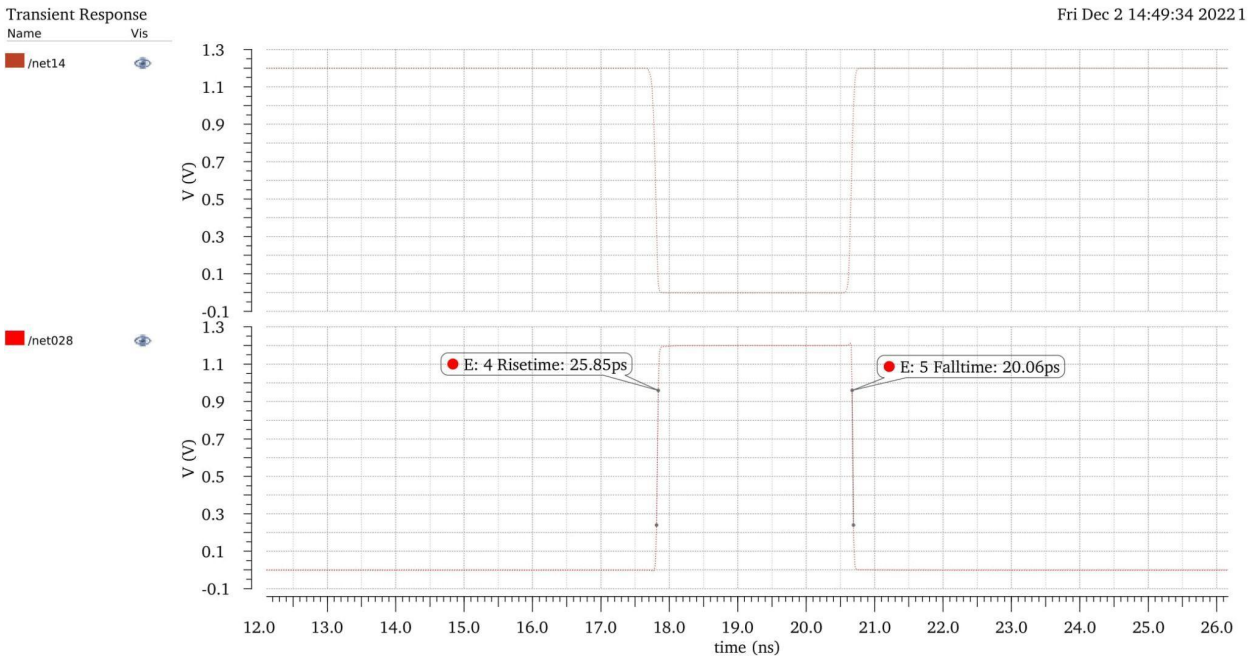

Figure 12: Input B Rise/Fall time of Fanout 4

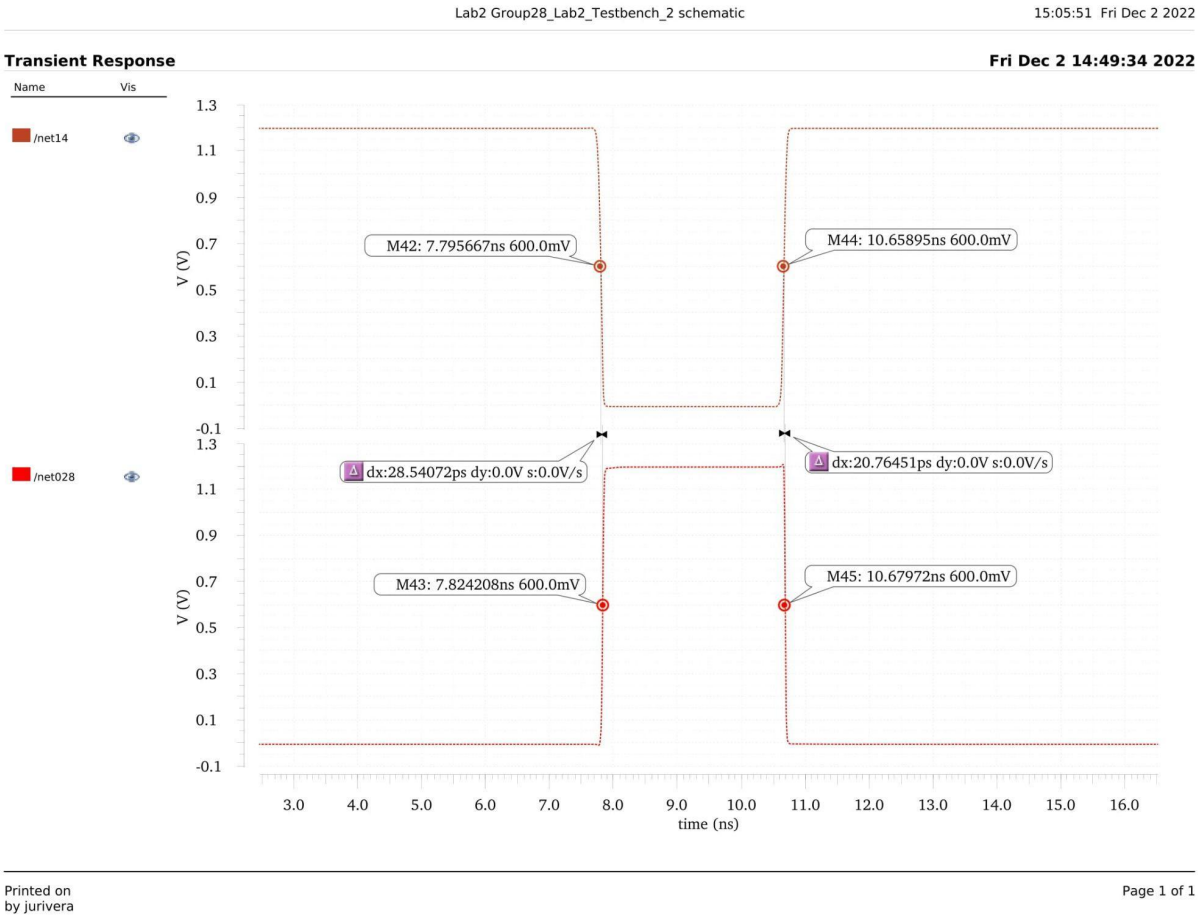

Figure 13: Input B Propagation Delay time of Fanout 4

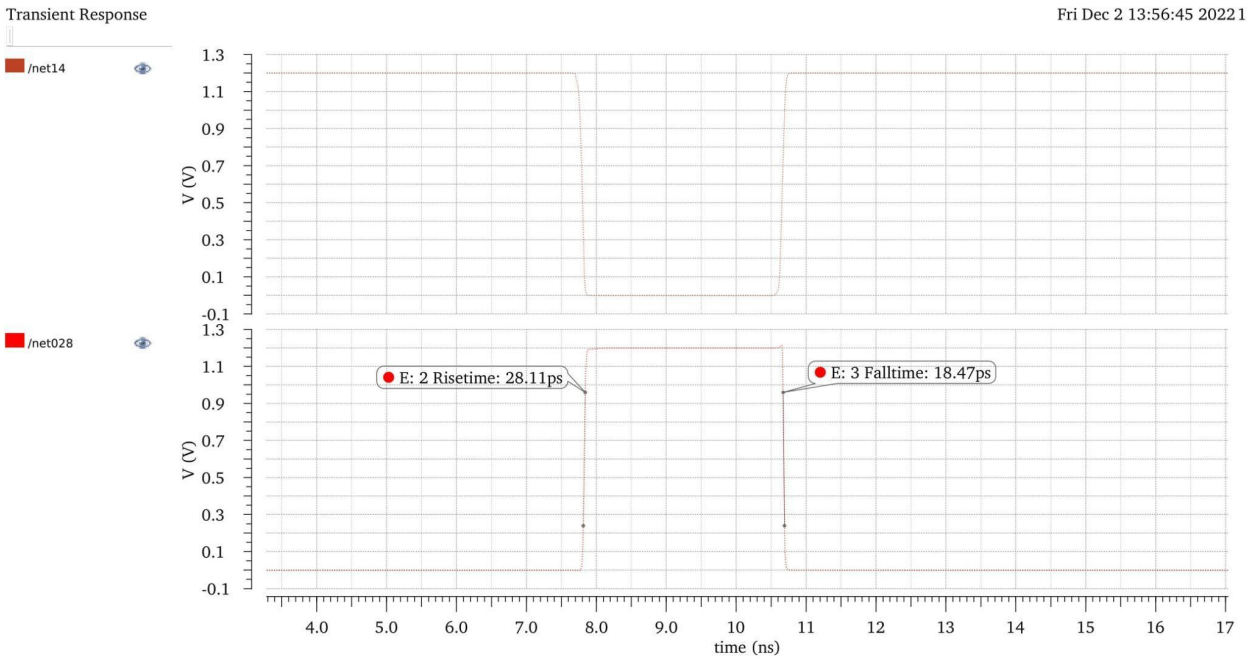

Figure 14: Input C Rise/Fall time of Fanout 4

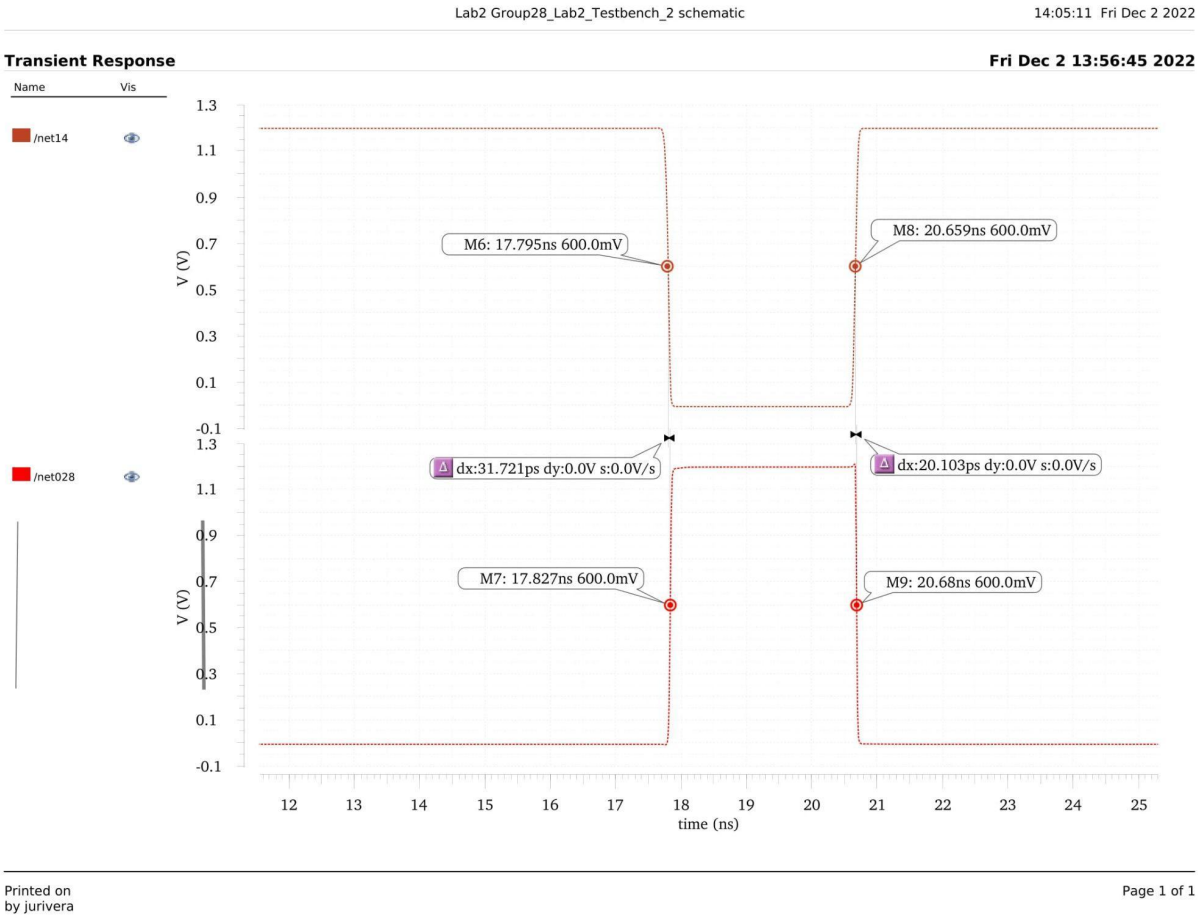

Figure 15: Input C Propagation Delay time of Fanout 4