In the name of God

Final project of analog electronics

Lecturer :

Dr. Fatemeh Akbar

Students :

Meysam Asadi 99101116

Mohammad Hossein Babaei 99101281

Date :

2024/6/10

The goal of this project is to design a MOS differential amplifier that meets the specified limits and includes the desired features.

$$V_{DD} = 1.8\ v\ , V_{SS} = 0v\ \ , A_{vd}\ , CMRR \geq 110\ db$$

The designed amplifier has two stages and a single ended output. The first stage is a folded Cascode structure and the second stage is a common source with an active load. To reach the specified CMRR a low voltage current source is used.

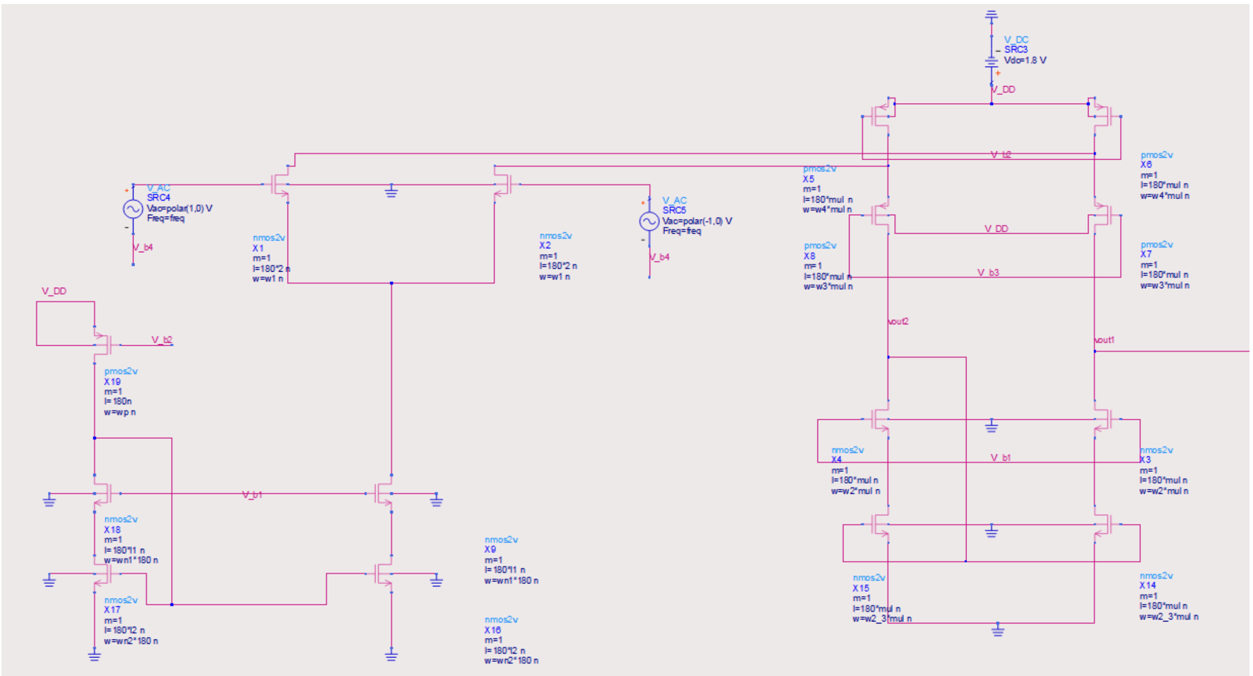


Figure 1: the structure of first stage

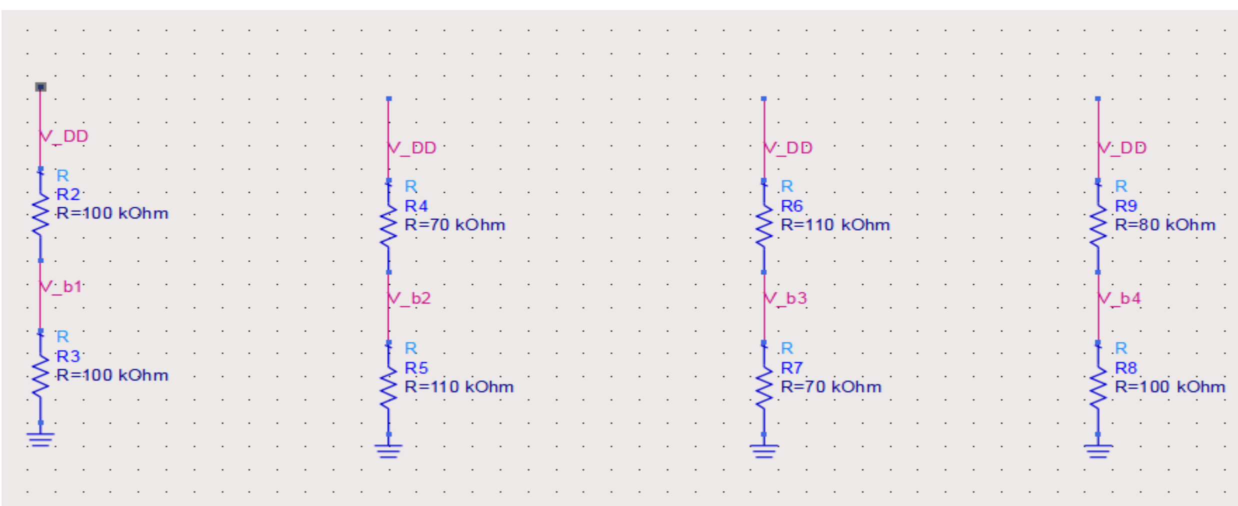


Figure 2: DC biases

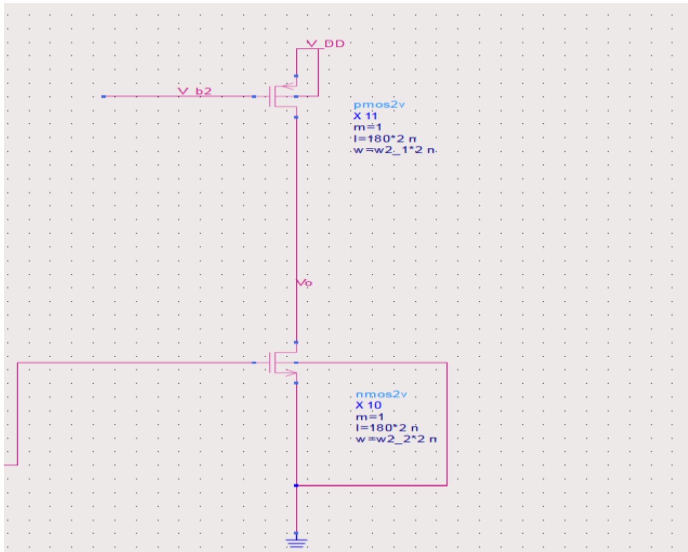


Figure 3: second stage

A_{vd}

Theoretical calculations:

$$A_{vd} = A_{vd1} * A_{vd2} = g_{m1}\ (r_{op}||r_{on})\ \ g_{m10}\ (r_{o11}||r_{o10})$$

$$g_{m1} = 2mmho\ , g_{m10} = 5mmho\ , rop \approx ron = 50M\Omega\ , r_{o11} \approx r_{o12} = 20k\Omega$$

$$A_{vd} \approx 128db$$

Simulation results:

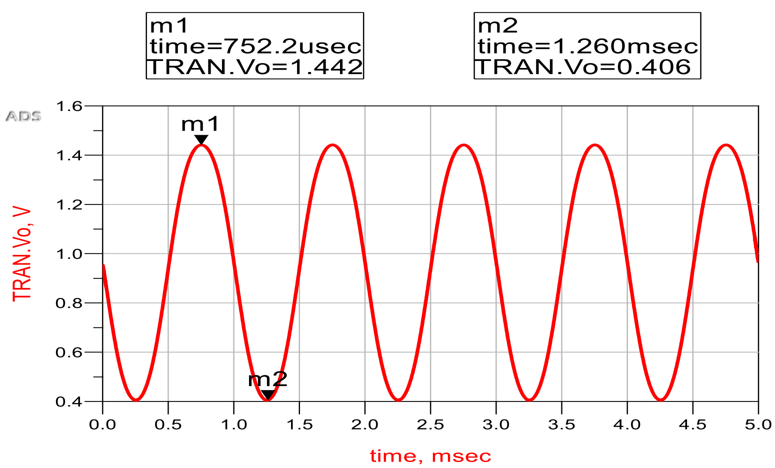


Figure 4: output voltage for an input of 1uV

$$A_{vd} \approx 114db$$

Power consumption

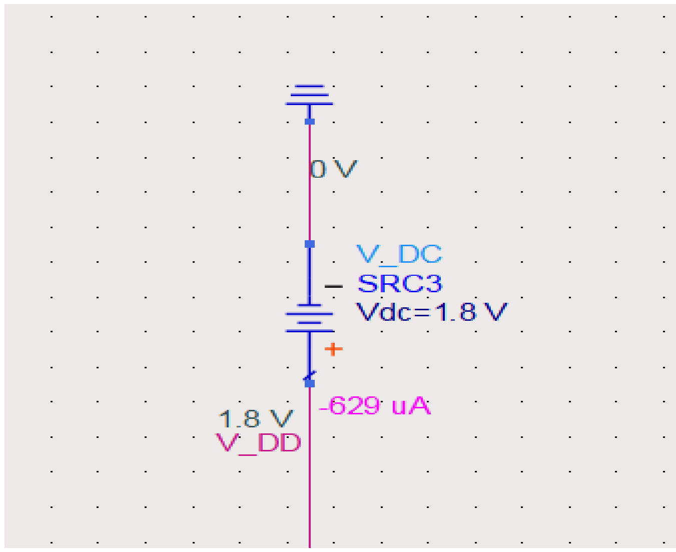
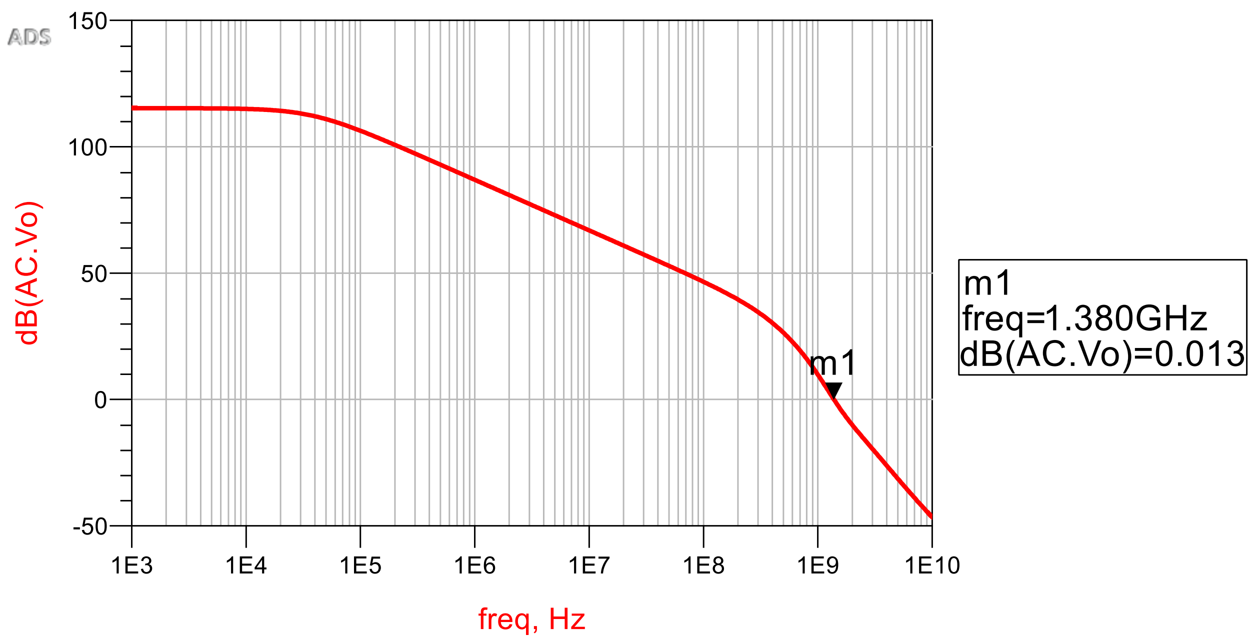


Figure 6: Power consumption

$$Power \approx 0.629 * 1.8 \approx 1.13mW$$

Phase margin

Frequency response before compensating:



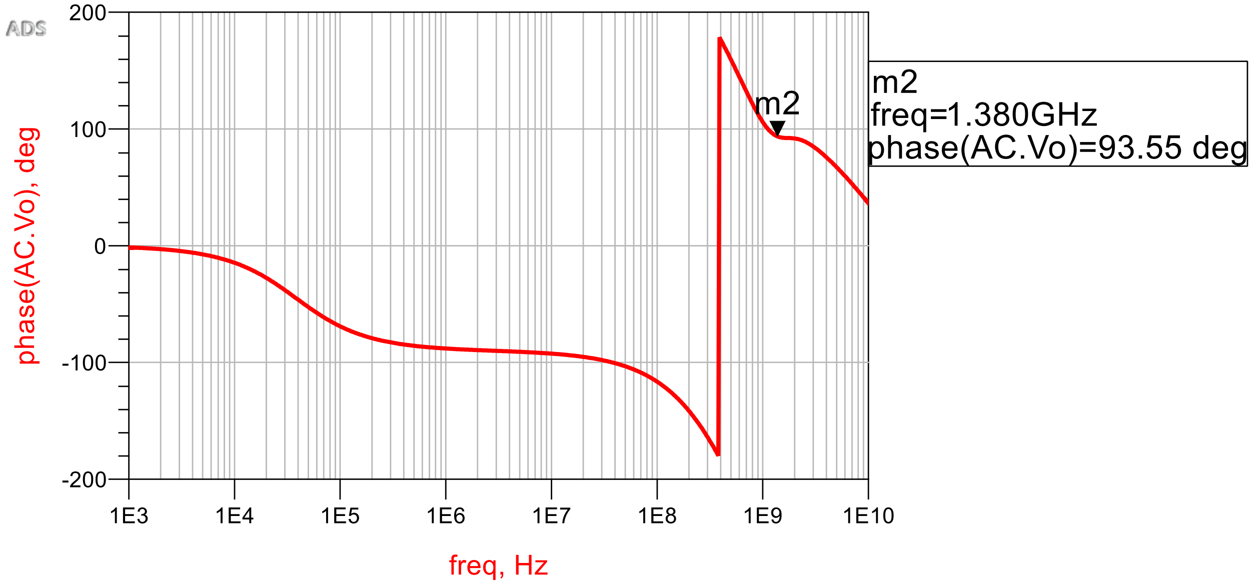


Figure 7: Open loop bode diagram

Above figure shows that when unity feedback is applied to the amplifier, the resulting buffer will be unstable at frequencies below f_u. Thus, the circuit needs to be compensated. Miller compensation method is used to get the desired phase margin.

Frequency response after compensating:

As mentioned in the previous part, buy choosing the right value for the capacitance and resistance we can get a phase margin above 45°.

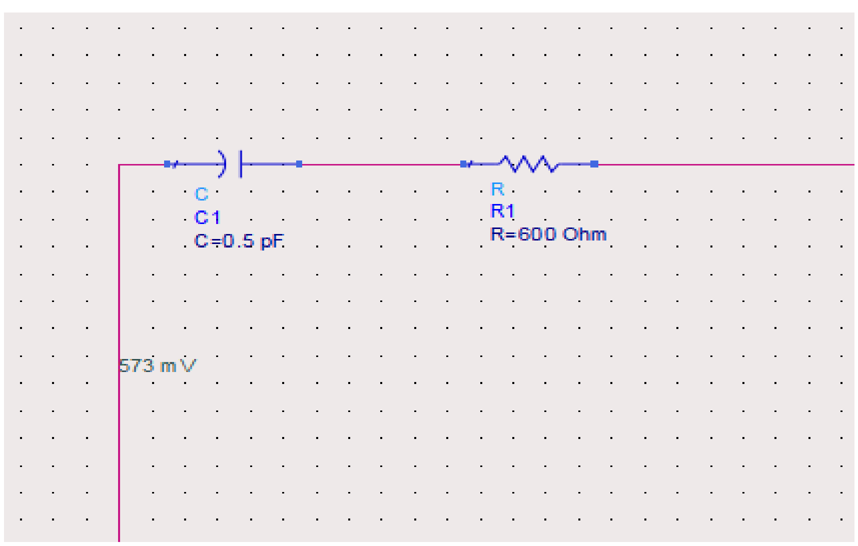


Figure 8: Compensation part (values are obtained by tuning)

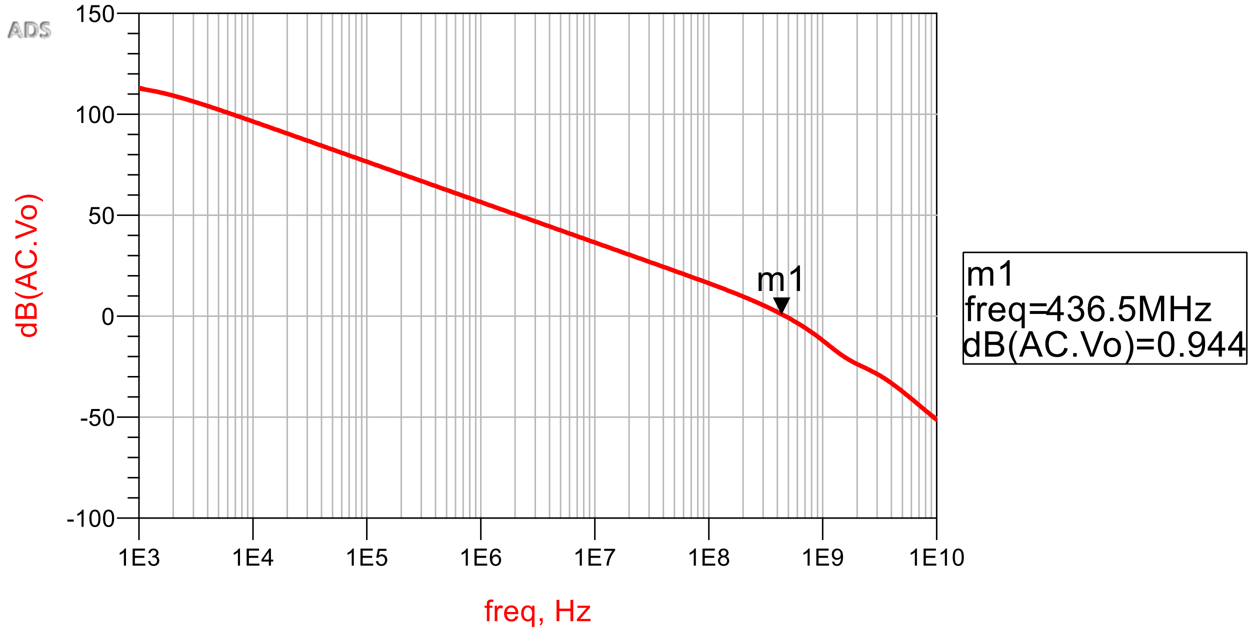


Figure 9: magnitude of frequency response ($f_u \approx 437\ MHz$)

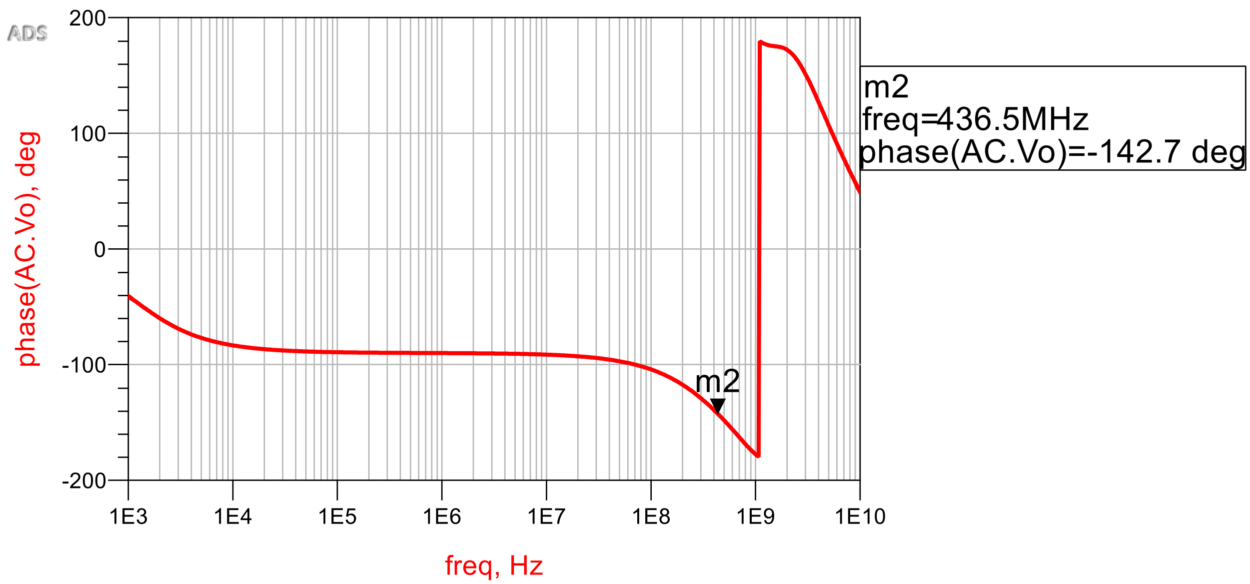


Figure 10: phase of frequency response ($phase\ margin \approx 47^{\circ}$)

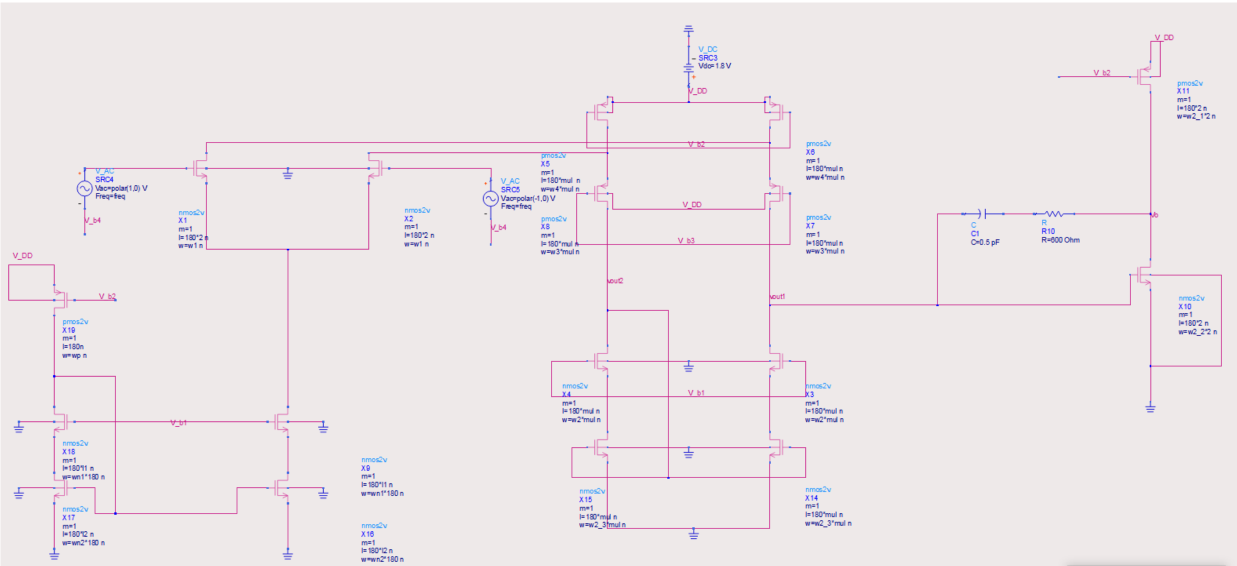


Figure 11: final schematic of the open loop circuit

Noise

The noise sources in this circuit are Flicker noise and channel noise of each MOS and thermal noise of resistors (R1, …, R8). To determine the equivalent input noise density, we first calculate the total output noise within a 1Hz bandwidth, and then divide this value by the gain at that frequency.

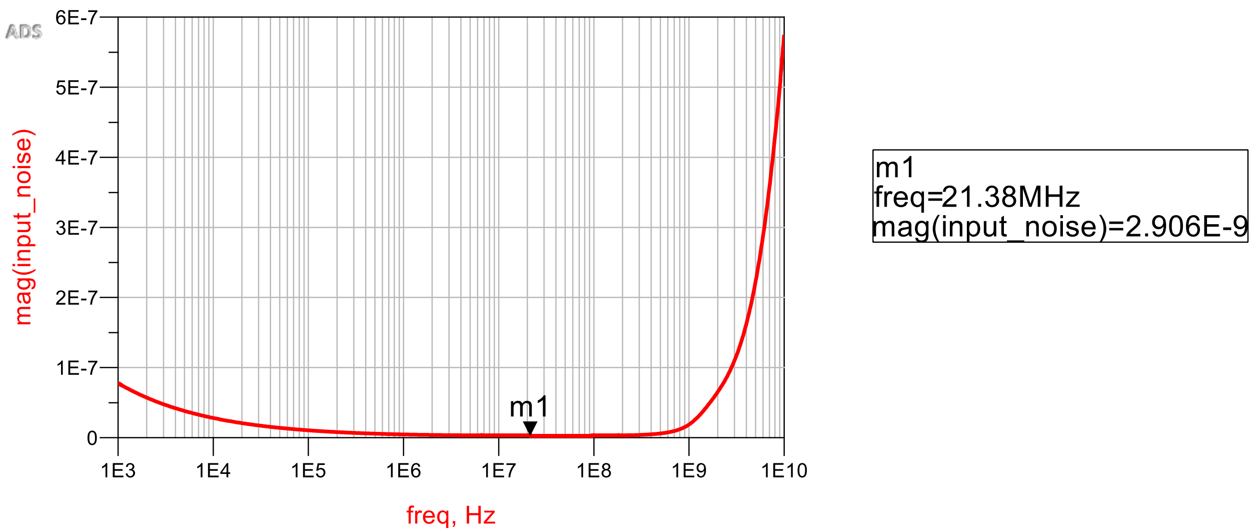


Figure 12: input noise density

As seen from the above figure, the total input noise density is below specified limit ($\frac{7nV}{\sqrt{Hz}}$).

P_P swing when unity feedback is applied

The bias of output is set at 0.9v to get the maximum output swing.

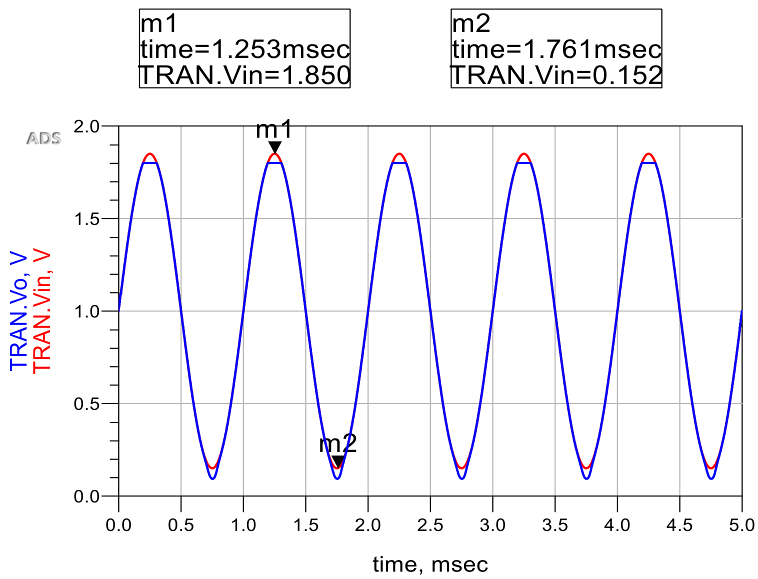


Figure 13: output volage when the input voltage is 1.7 v peak to peak.

Thus the output swing is less than 1.7v peak to peak.

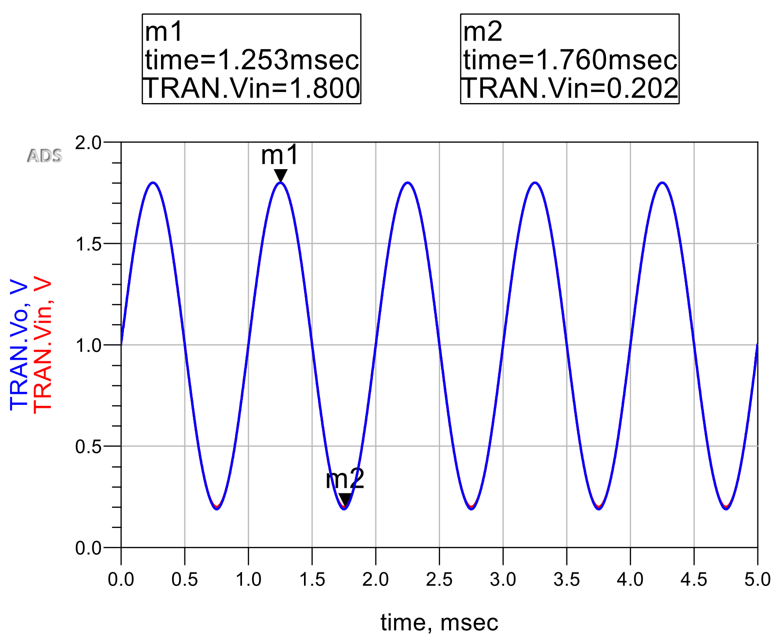


Figure 14: output volage when the input voltage is 1.6 v peak to peak.

As seen from the above figure, maximum output swing is 1.6v (peak to peak).

Bandwidth of the resulting Buffer

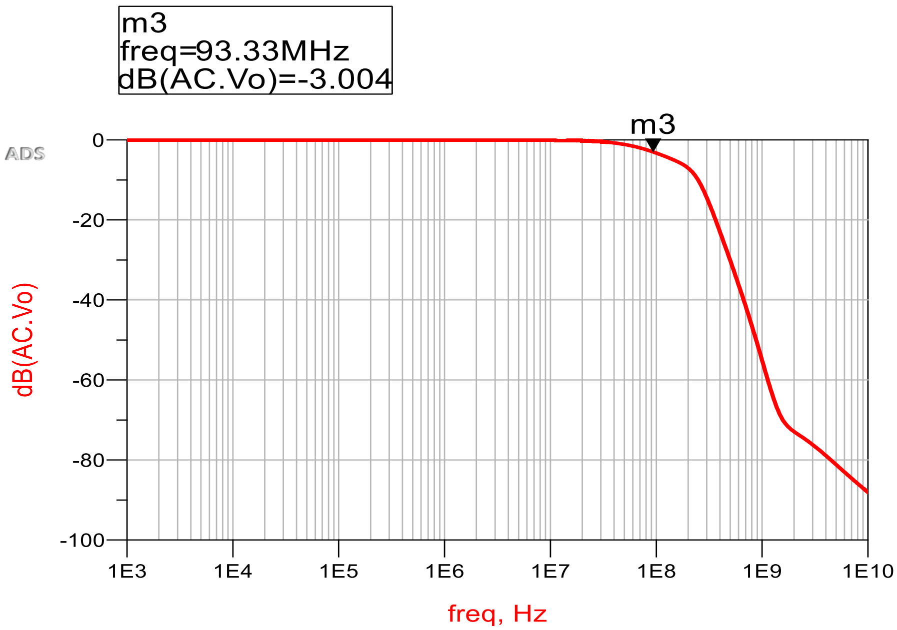


Figure 15: Frequency response of the buffer (BW≈93MHz)

Slew rate

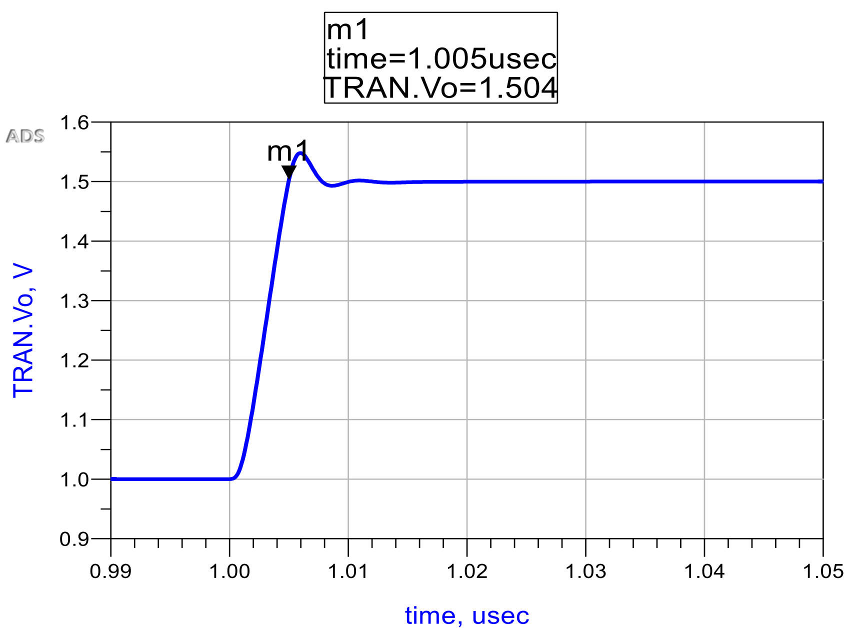


Figure 16: output voltage when a 0.5v step is applied to the input.

$$slew\ rate = \frac{0.5v}{5ns} = \boxed{100\ \frac{v}{\mu s}}$$

$settling\ time$: $14\ ns$

Noise

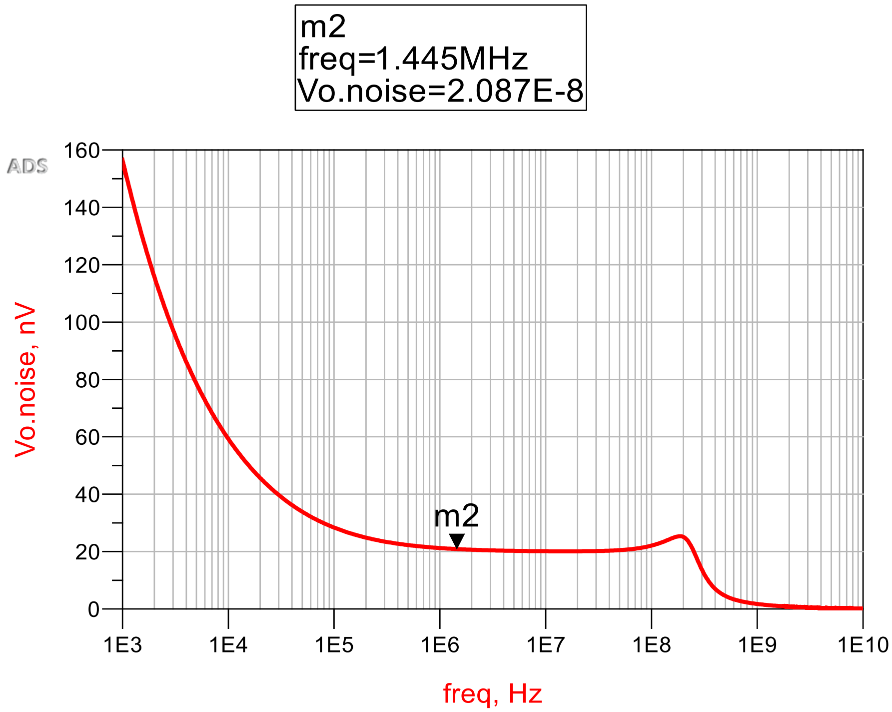


Figure 17: total output noise of the buffer.

Extra details about the amplifier

Size

MOS	W (×180 nm)	L (×180 nm)
M1,M2	300	2
M3,M4,M5,M6,M7,M8	50	3
M9, M18	50	2
M16.M17	50	1
M19	45	1
M10	100	2
M11	137	2
M14,M15	15	3

DC OP point

MOS	|Vgs| (mv)	|Vth| (mv)	|Vds| (mv)	I (uA)
M1,M2	603	563	979	56
M3,M4	581	571	254	40
M5,M6	700	465	384	96
M7,M8	716	580	842	40
M9	681	552	217	112

M18	677	553	354	112
M16	577	517	219	112
M17	577	517	223	112
M19	700	506	1220	112
M10	573	493	952	286
M11	700	474	848	286
M14	573	487	319	40