In the name of almighty

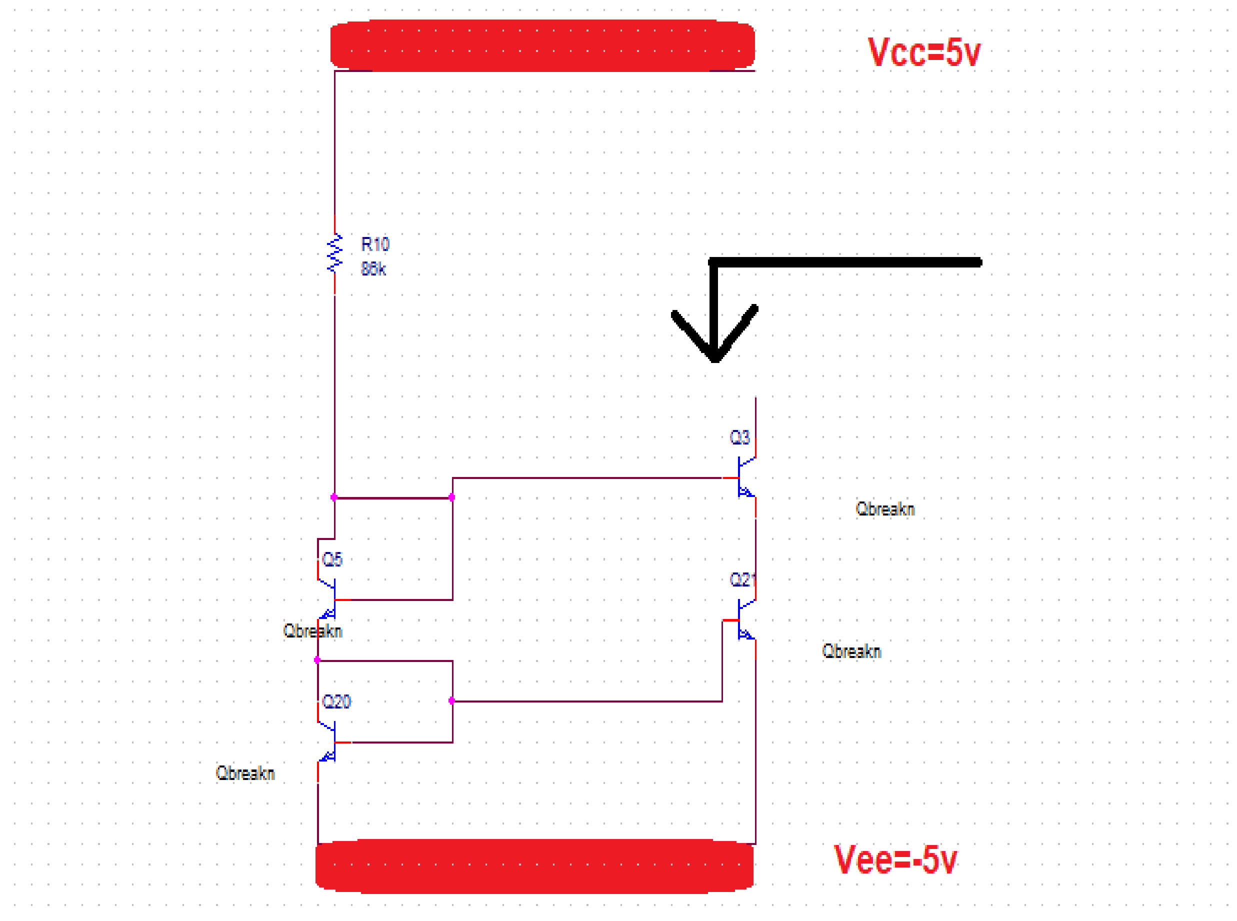
Meysam Asadi 99101116

Project

First Design

Designing a current source

Due to its high output impedance We will use the cascade stage in order to design our current source.

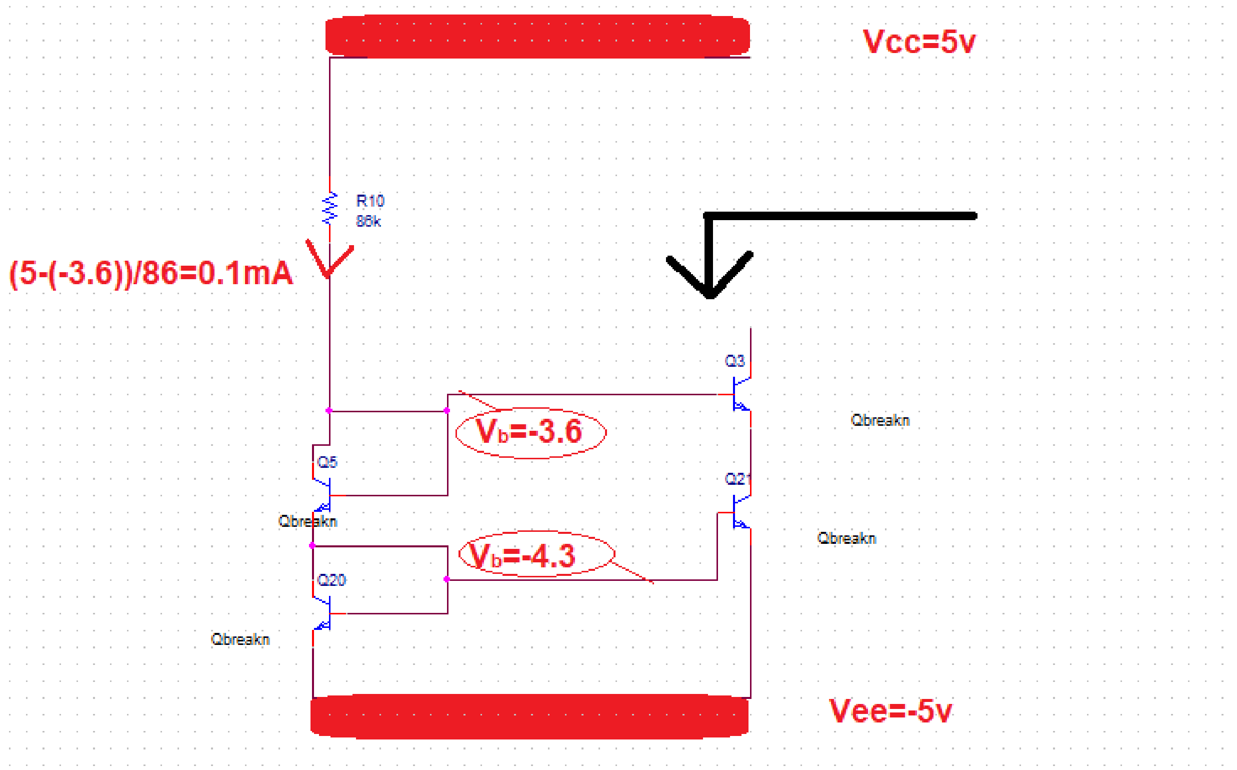


Let's compute the impedance seen from the output (according to cascode output impedance formula).

$$R_{out} \approx (1 + g_{m3}(r_{o2}||r_{\pi3}))\, r_{o3} + (r_{o2}||r_{\pi3})$$

Note that we can neglect the impedance seen from the base of Q3;

We have biased this stage to supply a current of 0.1mA ;



$$I_{Q5} \approx I_{Q20} \approx I_{Q3} \approx I_{Q2} \approx 0.1\ mA$$

$$g_{mQ5} \approx g_{mQ20} \approx g_{mQ3} \approx g_{mQ2} \approx 4m\mho$$

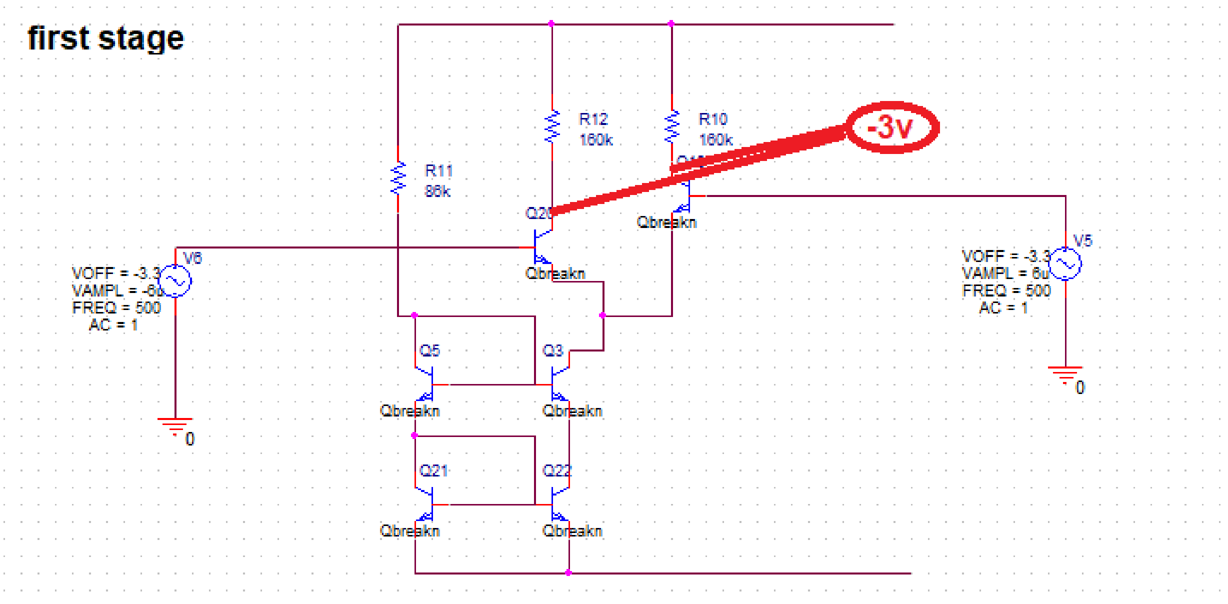
$$r_{\pi\ Q5} \approx r_{\pi\ Q20} \approx r_{\pi\ Q3} \approx r_{\pi\ Q2} \approx 25k\Omega$$

$$r_o \approx 1M\Omega$$

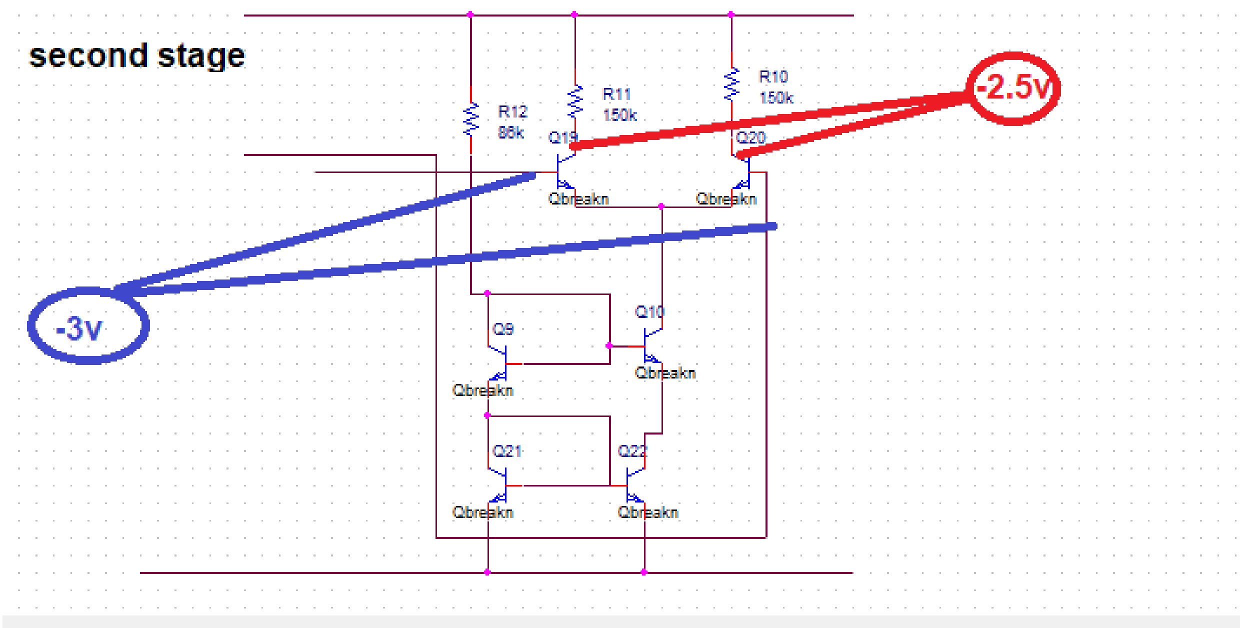
$$R_{out} \approx 100\ M\ \Omega$$

Amplifiying stages

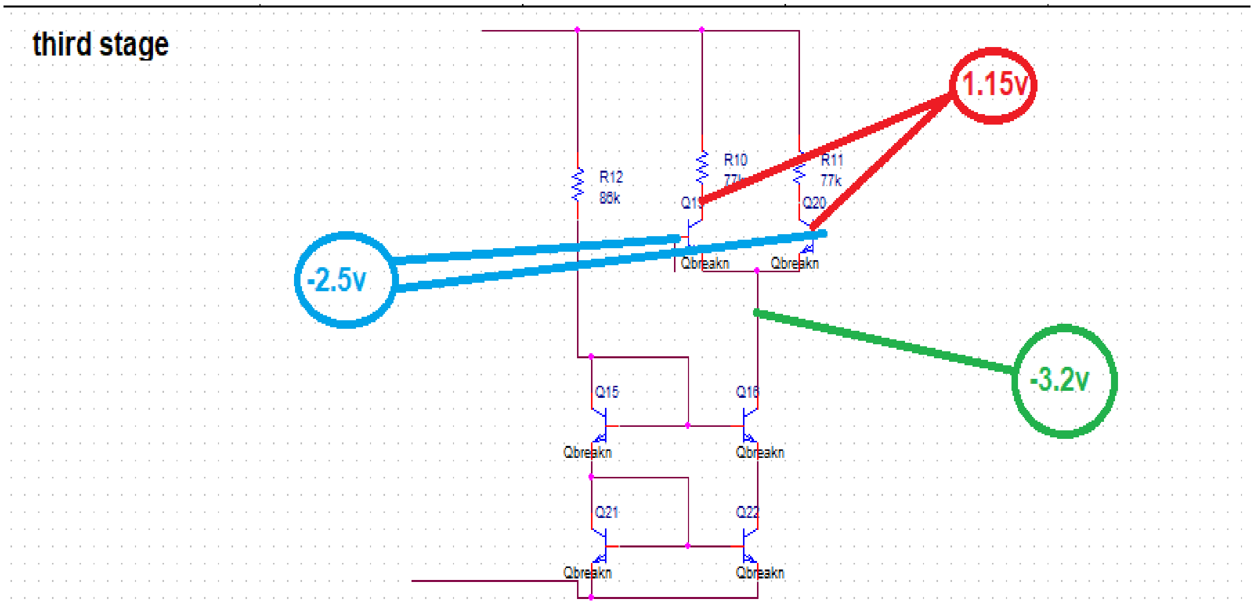
$$g_m\ of\ differential\ stages \approx 2m\mho$$



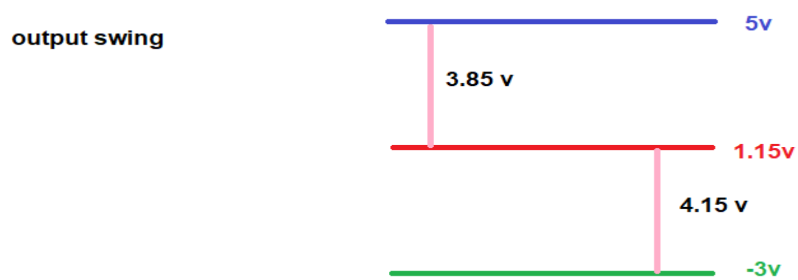
$$V_E = -4v\ ,V_C = -3v \rightarrow V_{CE} = 1v$$



$$V_E = -3.7v\ ,V_C = -2.5v \rightarrow V_{CE} = 1.2v$$



$$V_E = -3.2v\ , V_C = 1.15v \rightarrow V_{CE} = 4.35v$$

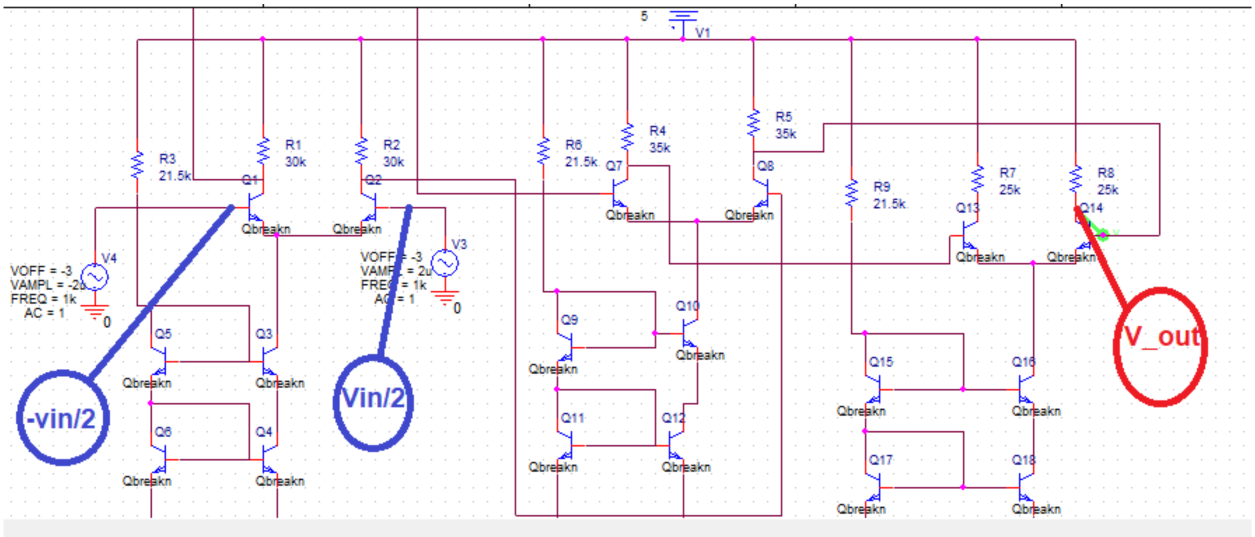


Gain of the first stage : $-g_m * (160k \parallel 50\ k) = -76$ → 50 kΩ is the R_{in} of next stage

Gain of the second stage : $-g_m * (150k \parallel 50\ k) = -75$ → 50 kΩ is the R_{in} of next stage

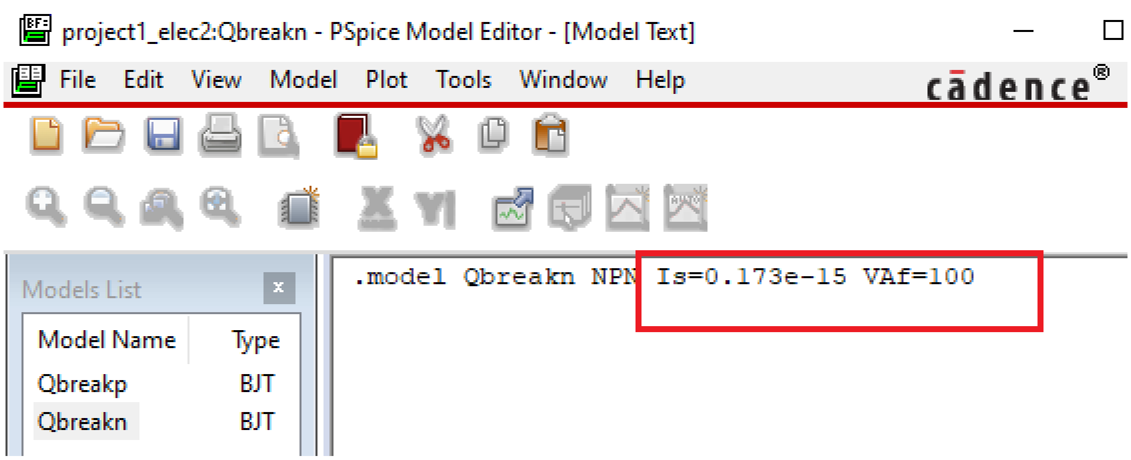
Gain of the third stage : $-g_m * 77\ k = -154$

● *note that we can ignore the Early effect because* r_o *is massive compred to* R_c



$$\text{Gain}=\frac{V_{out}}{V_{in}/_2} = -76 * 75 * 154 \approx -877{,}800$$

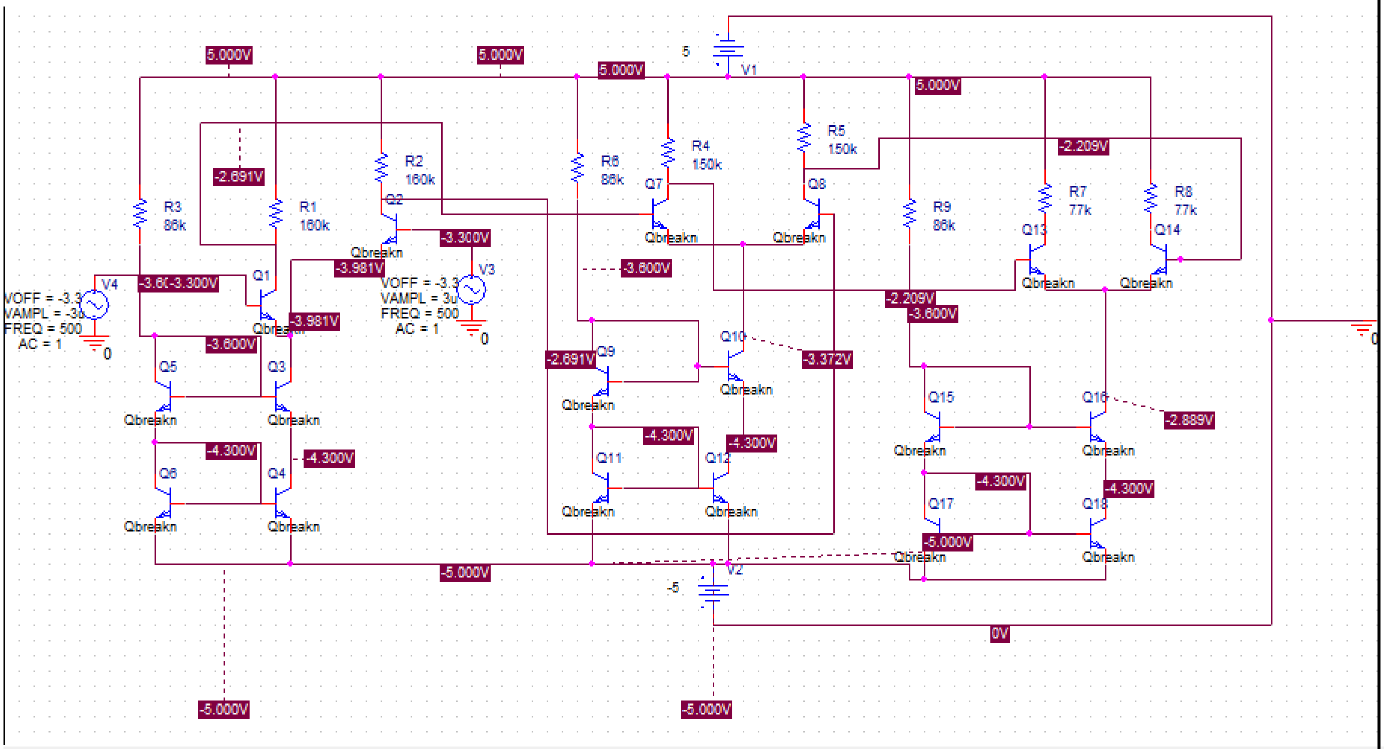
Pspice simulation results

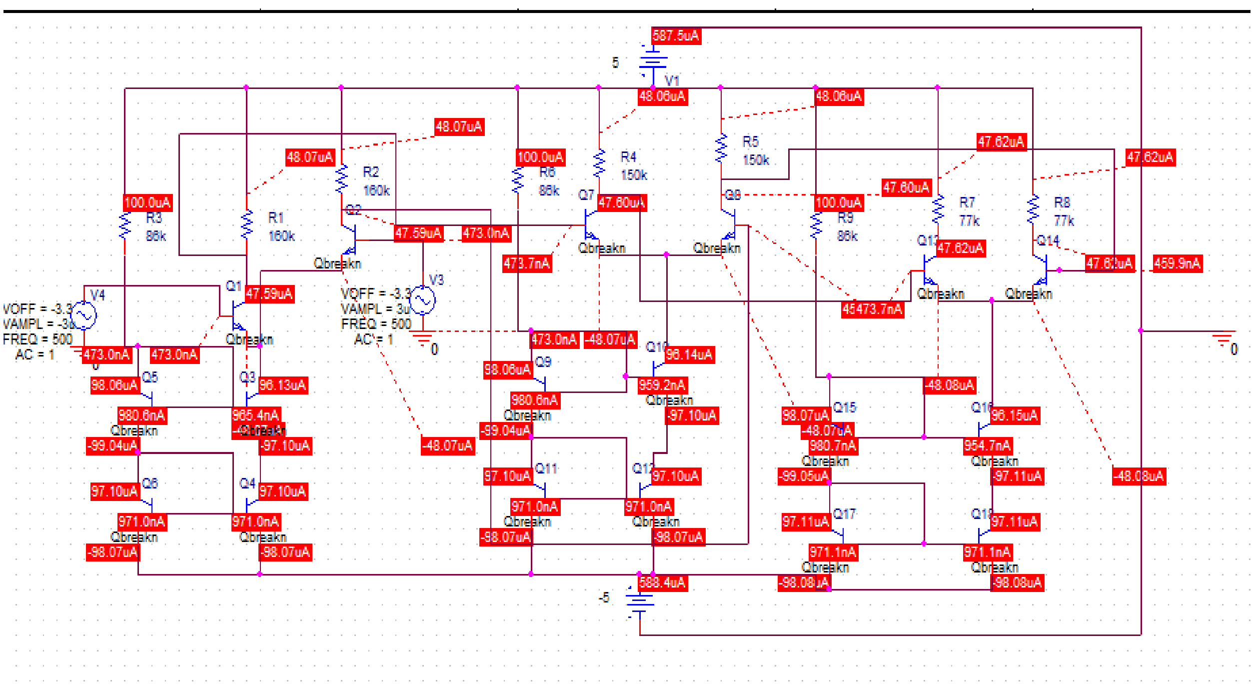


Pspice model of NPN transistor has been edited to ensure that

$$V_{BEon} \approx 0.7 \quad and \quad Early\ voltage \approx 100$$

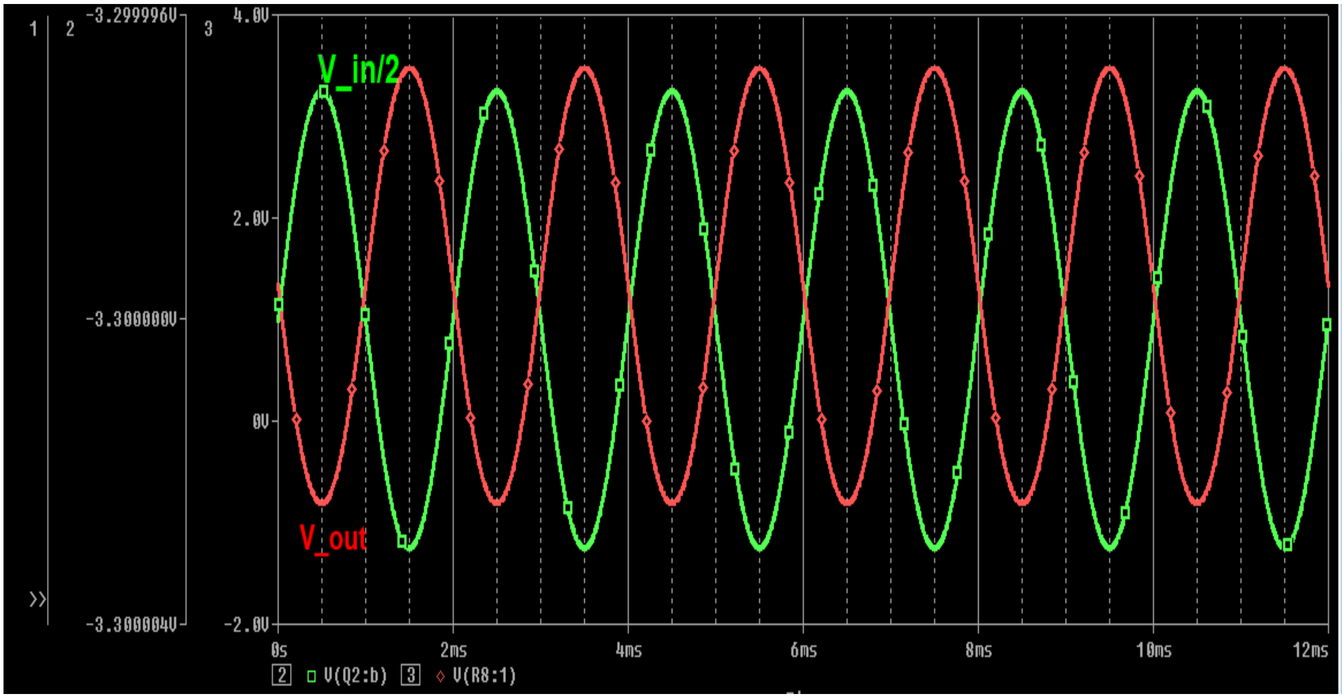
1)Bias points





the difference in voltages is because the bias currents are slightly different than what we have set (0.05mA) and this small difference is being multiplied by a big impedance which makes a considerable difference in the result;

1)Gain

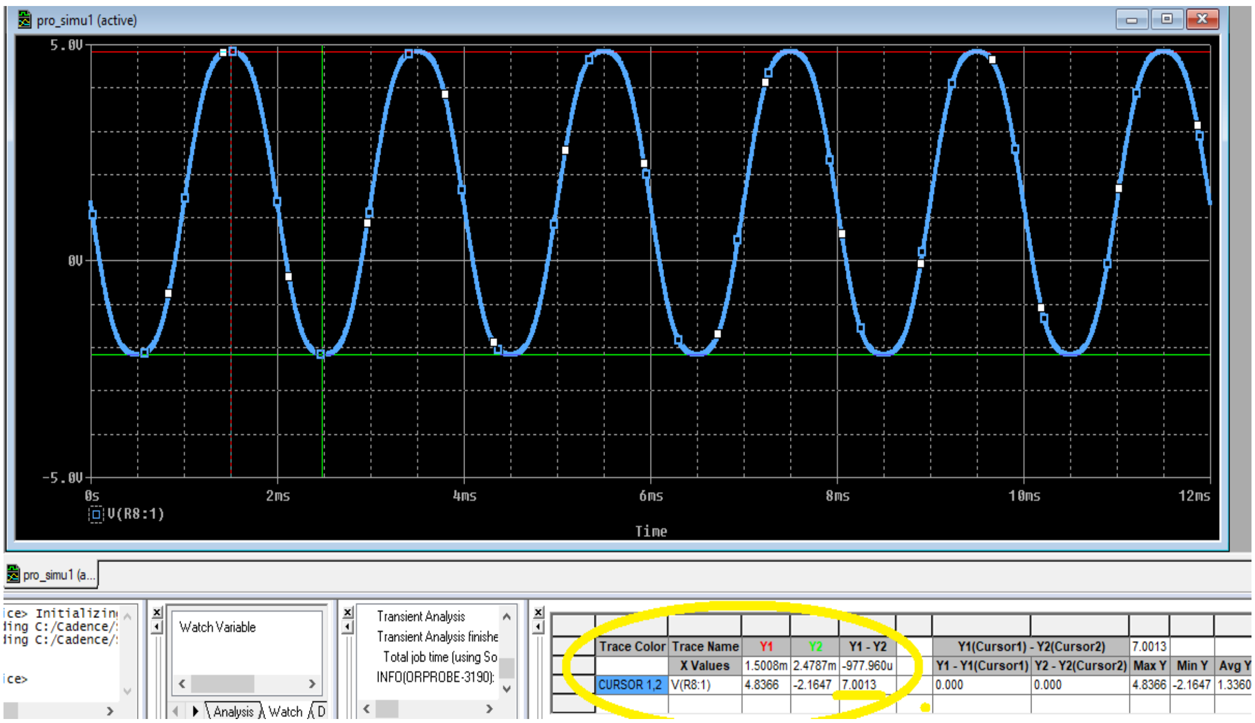


Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	1.4498m	483.404u	966.377u
CURSOR 1,2	V(Q2:b)	-3.3000	-3.3000	-5.9664u

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	2.5177m	1.5098m	1.0080m
CURSOR 1,2	V(R8:1)	-804.804m	3.4739	-4.2787

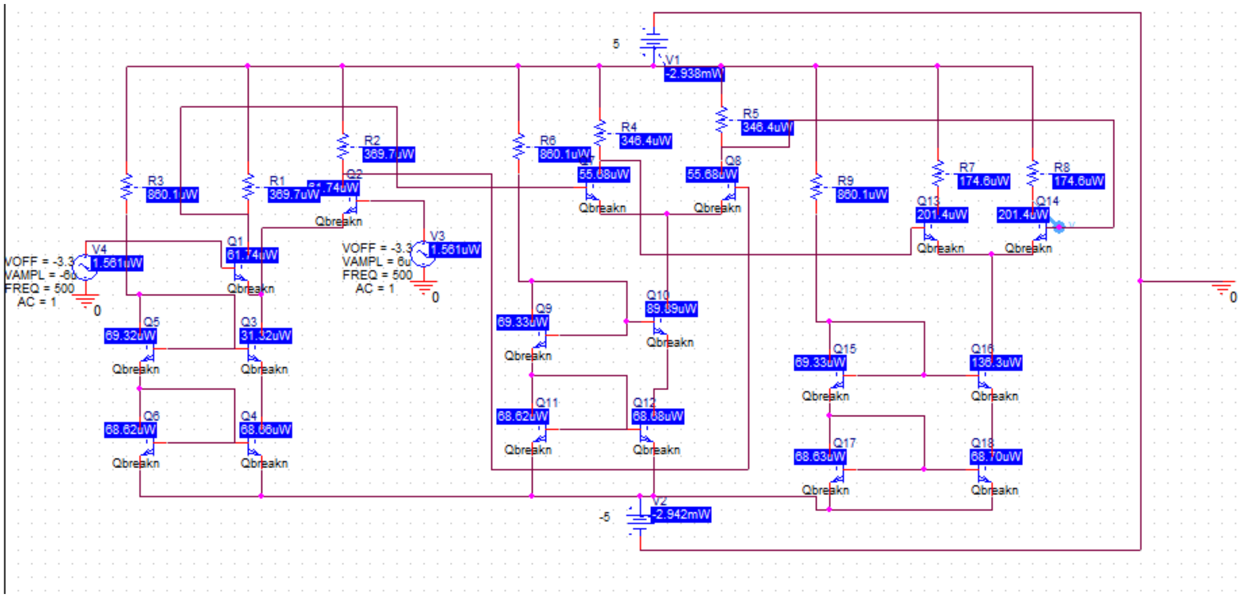
$$Gain = \frac{-4.2787}{5.966} \approx -720{,}000$$

1)Swing



Swing is +-3.5v

1)Power dissipation



Power dissipation =2.9*2mW

Comparing simulation result with theoretical result

Property	Theoretical	simulation
Power dissipation	6*0.1mA*10v=6mW	5.8mW
Differential Gain(V_out /(V_in/2))	-877800	-720000
Output Swing	$\pm 3.85v$	$\pm 3.5v$

CMMR

$$A_{v_{CM}} \approx \frac{-R_c}{2R_{EE}}$$

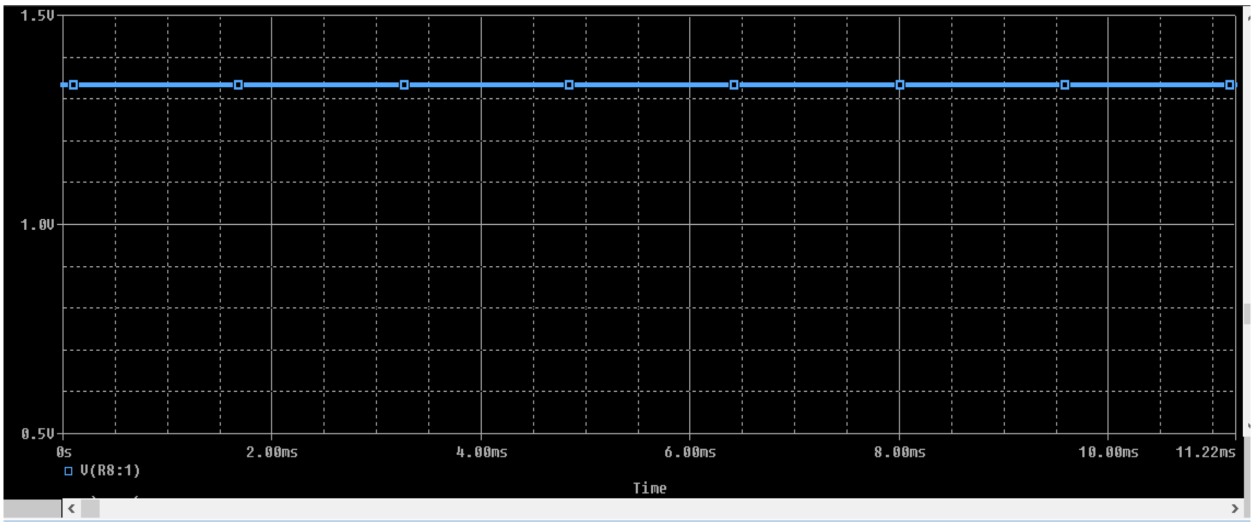
$$A_{v_{CM(stage1)}} \approx \frac{-(160k||50k)}{2 * 100M} \approx 0.2m$$

$$A_{v_{CM}(stage2)} \approx \frac{-(150k||50k)}{2 * 100M} \approx 0.2m$$

$$A_{v_{CM}(stage3)} \approx \frac{-77k}{2 * 100M} \approx 0.4m$$

$$A_{vCM}tot \approx 0.016n$$

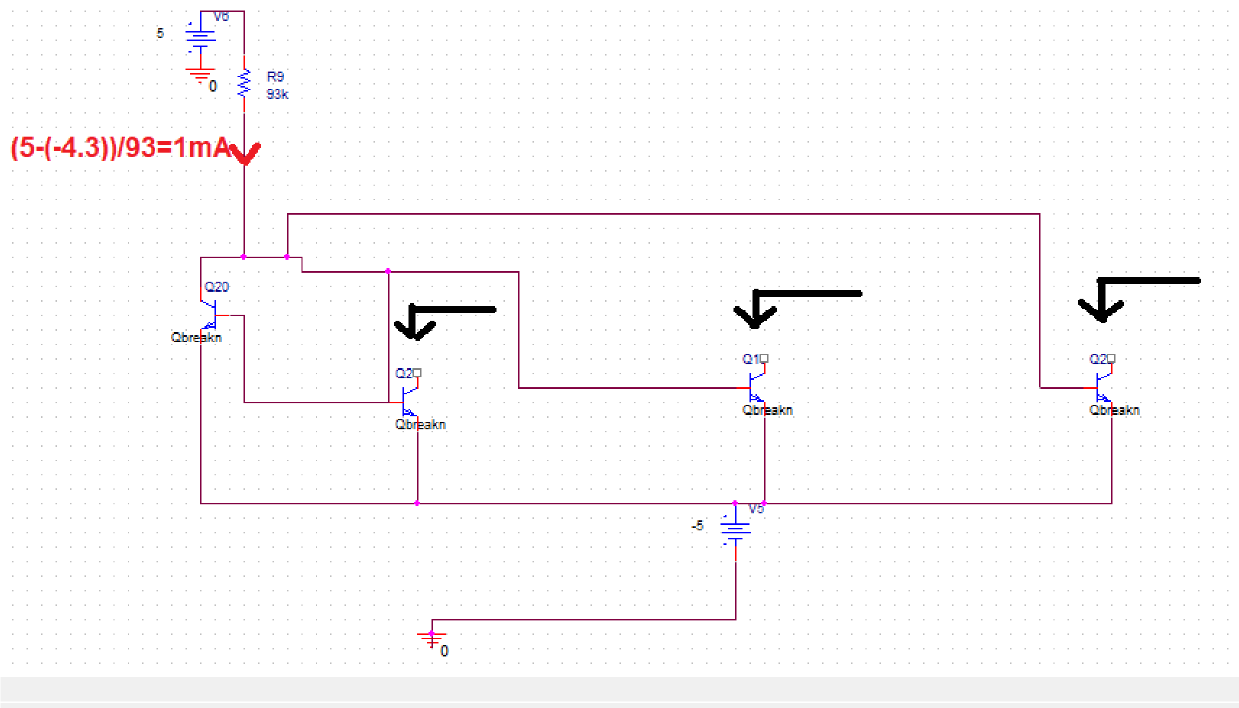
$$CMMR = -20 \log \left| \frac{A_{vCM}}{A_{vD}} \right| \approx 333$$



This shows that common mode is not being amplified

another Design

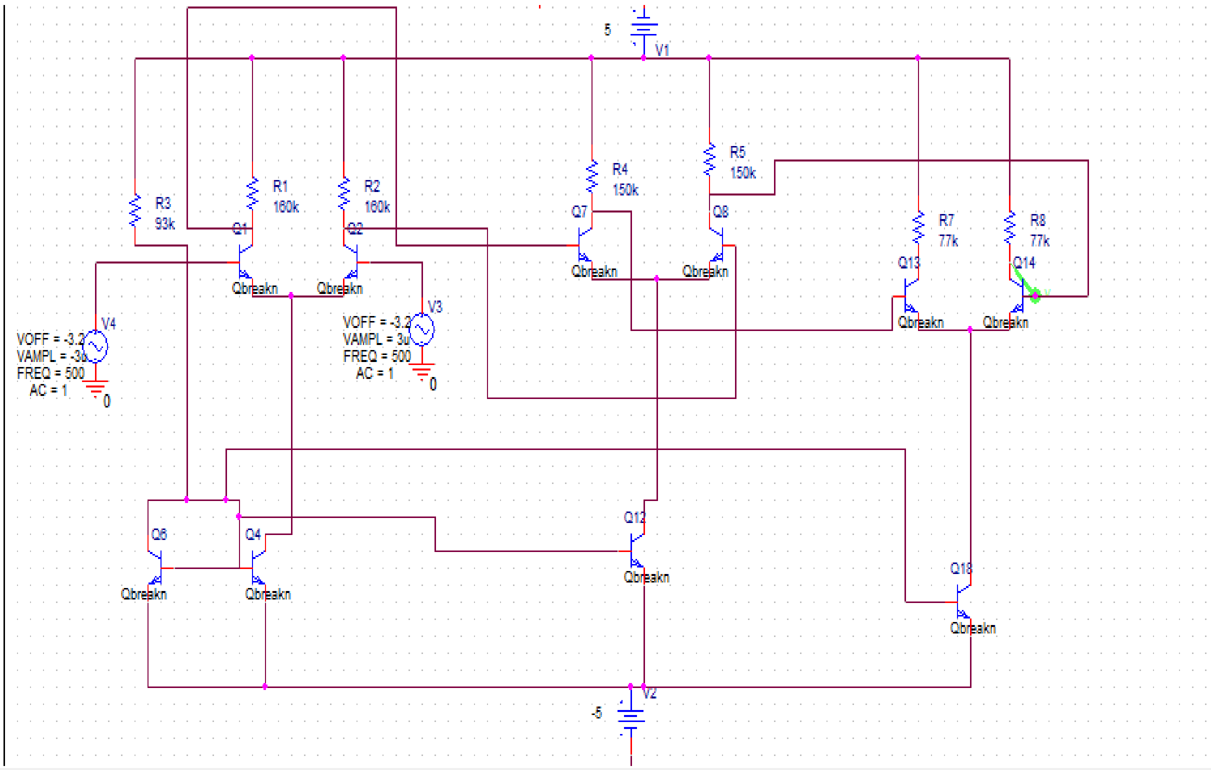
This design has less power dissipation because we have used current mirrors. Instead it has less impedance seen from the emitter of amplifying stages and that affects common mode gain;



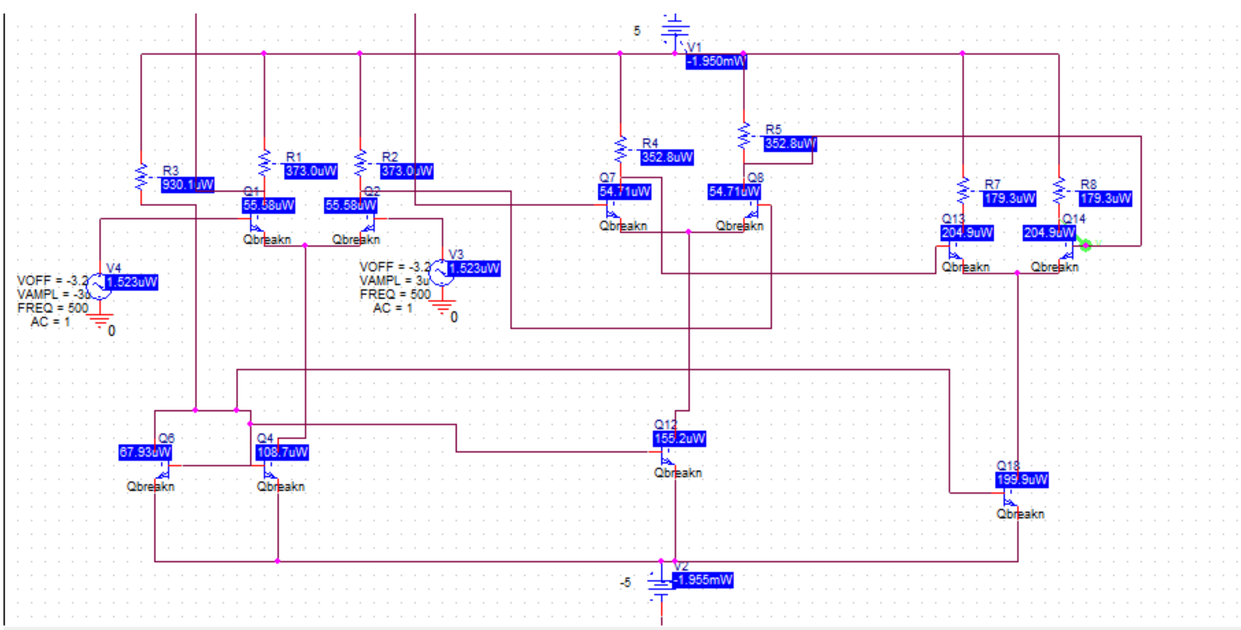
Impedance seen from each arrow is:

$$R_{out} \approx r_o = 1M\Omega$$

bias and gain and swing is the same as the first design



Power dissipation



The total power dissipation is <u>3.8 mW</u>

CMMR

$$A_{v_{CM}} \approx \frac{-R_c}{2R_{EE}}$$

$$A_{v_{CM(stage1)}} \approx \frac{-(160k||50k)}{2 * 1M} \approx 20m$$

$$A_{v_{CM(stage2)}} \approx \frac{-(150k||50k)}{2 * 100M} \approx 20m$$

$$A_{v_{CM(stage3)}} \approx \frac{-77k}{2 * 1M} \approx 40m$$

$$A_{vCM}tot \approx 16\mu$$

$$CMMR = -20\log\left|\frac{A_{vCM}}{A_{vD}}\right| \approx 213$$