
STM32
CubeMX

1. Description

1.1. Project

Project Name	micro-ROS
Board Name	B-L4S5I-IOT01A
Generated with:	STM32CubeMX 6.2.1
Date	05/20/2021

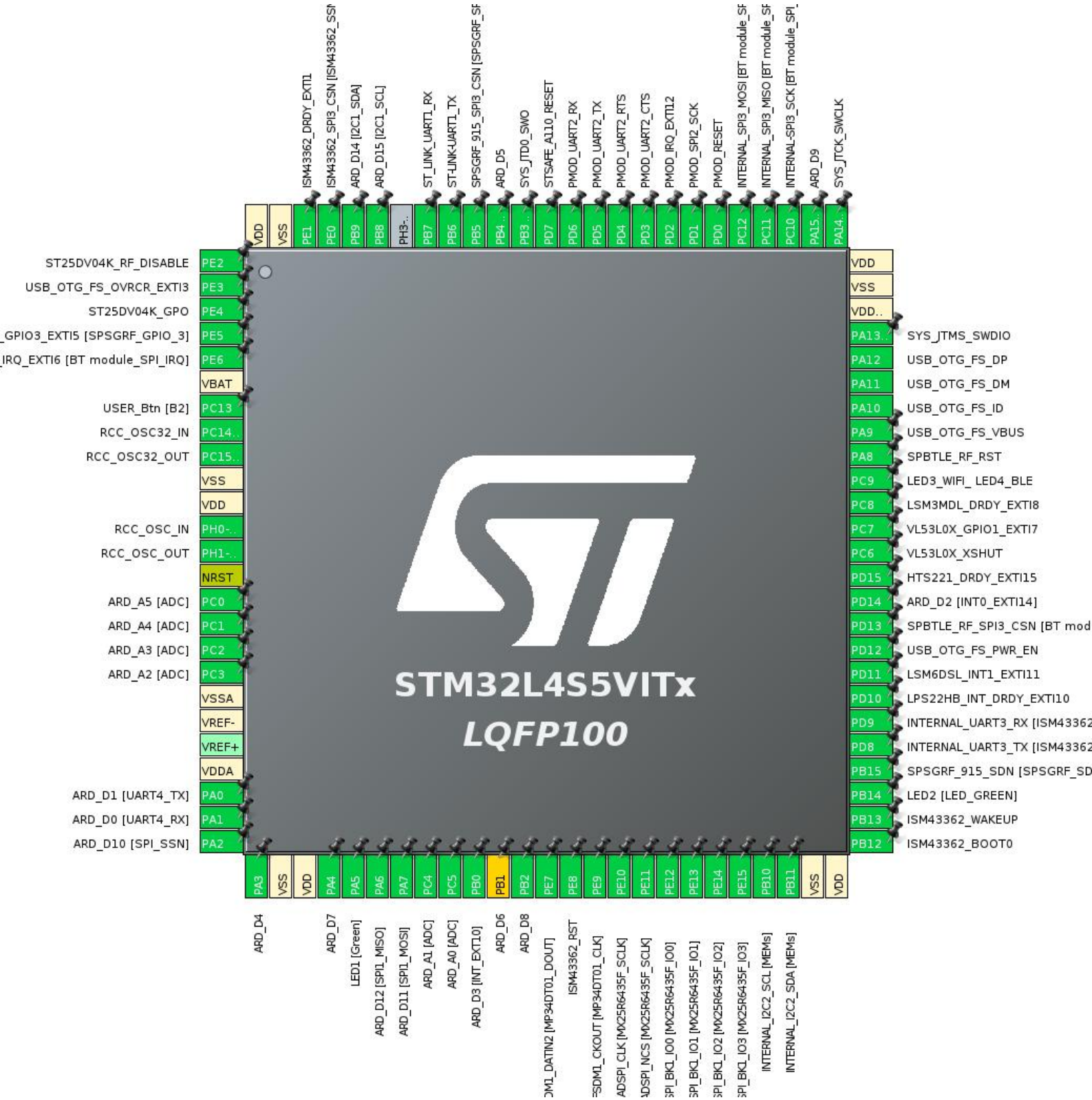
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4R5/S5
MCU name	STM32L4S5VITx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	ST25DV04K_RF_DISABLE
2	PE3	I/O	GPIO_EXTI3	USB_OTG_FS_OVRCR_EXTI3
3	PE4	I/O	GPIO_EXTI4	ST25DV04K_GPO
4	PE5	I/O	GPIO_EXTI5	SPSGRF_915_GPIO3_EXTI5 [SPSGRF_GPIO_3]
5	PE6	I/O	GPIO_EXTI6	SPBTLE_RF_IRQ_EXTI6 [BT module_SPI_IRQ]
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B2]
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC1_IN1	ARD_A5 [ADC]
16	PC1	I/O	ADC1_IN2	ARD_A4 [ADC]
17	PC2	I/O	ADC1_IN3	ARD_A3 [ADC]
18	PC3	I/O	ADC1_IN4	ARD_A2 [ADC]
19	VSSA	Power		
20	VREF-	Power		
22	VDDA	Power		
23	PA0	I/O	UART4_TX	ARD_D1 [UART4_TX]
24	PA1	I/O	UART4_RX	ARD_D0 [UART4_RX]
25	PA2 *	I/O	GPIO_Output	ARD_D10 [SPI_SSN]
26	PA3 *	I/O	GPIO_Output	ARD_D4
27	VSS	Power		
28	VDD	Power		
29	PA4 *	I/O	GPIO_Output	ARD_D7
30	PA5	I/O	SPI1_SCK	LED1 [Green]
31	PA6	I/O	SPI1_MISO	ARD_D12 [SPI1_MISO]
32	PA7	I/O	SPI1_MOSI	ARD_D11 [SPI1_MOSI]
33	PC4	I/O	ADC1_IN13	ARD_A1 [ADC]
34	PC5	I/O	ADC1_IN14	ARD_A0 [ADC]

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
35	PB0	I/O	GPIO_EXTI0	ARD_D3 [INT_EXT10]
36	PB1 **	I/O	TIM3_CH4	ARD_D6
37	PB2 *	I/O	GPIO_Output	ARD_D8
38	PE7	I/O	DFSDM1_DATIN2	DFSDM1_DATIN2 [MP34DT01_DOUT]
39	PE8 *	I/O	GPIO_Output	ISM43362_RST
40	PE9	I/O	DFSDM1_CKOUT	DFSDM1_CKOUT [MP34DT01_CLK]
41	PE10	I/O	OCTOSPIM_P1_CLK	QUADSPI_CLK [MX25R6435F_SCLK]
42	PE11	I/O	OCTOSPIM_P1_NCS	QUADSPI_NCS [MX25R6435F_SCLK]
43	PE12	I/O	OCTOSPIM_P1_IO0	OQUADSPI_BK1_IO0 [MX25R6435F_IO0]
44	PE13	I/O	OCTOSPIM_P1_IO1	QUADSPI_BK1_IO1 [MX25R6435F_IO1]
45	PE14	I/O	OCTOSPIM_P1_IO2	QUAD_SPI_BK1_IO2 [MX25R6435F_IO2]
46	PE15	I/O	OCTOSPIM_P1_IO3	QUAD_SPI_BK1_IO3 [MX25R6435F_IO3]
47	PB10	I/O	I2C2_SCL	INTERNAL_I2C2_SCL [MEMs]
48	PB11	I/O	I2C2_SDA	INTERNAL_I2C2_SDA [MEMs]
49	VSS	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	ISM43362_BOOT0
52	PB13 *	I/O	GPIO_Output	ISM43362_WAKEUP
53	PB14 *	I/O	GPIO_Output	LED2 [LED_GREEN]
54	PB15 *	I/O	GPIO_Output	SPSGRF_915_SDN [SPSGRF_SDN]
55	PD8	I/O	USART3_TX	INTERNAL_UART3_TX [ISM43362_RX]
56	PD9	I/O	USART3_RX	INTERNAL_UART3_RX [ISM43362_TX]
57	PD10	I/O	GPIO_EXTI10	LPS22HB_INT_DRDY_EXTI 10
58	PD11	I/O	GPIO_EXTI11	LSM6DSL_INT1_EXTI11
59	PD12	I/O	GPIO_EXTI12	USB_OTG_FS_PWR_EN
60	PD13 *	I/O	GPIO_Output	SPBTLE_RF_SPI3_CSN [BT module_SPI_CS]
61	PD14	I/O	GPIO_EXTI14	ARD_D2 [INT0_EXTI14]

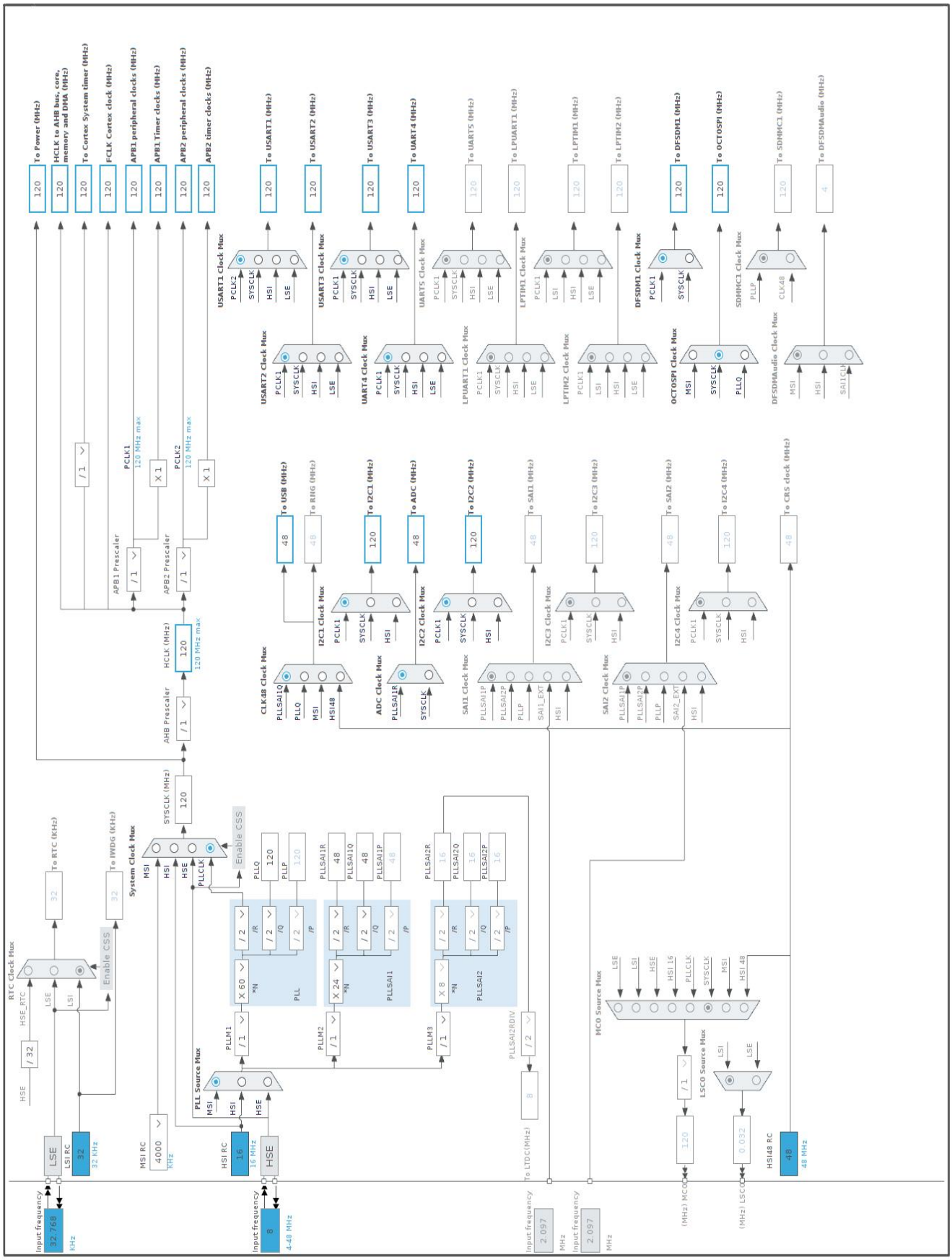
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
62	PD15	I/O	GPIO_EXTI15	HTS221_DRDY_EXTI15
63	PC6 *	I/O	GPIO_Output	VL53L0X_XSHUT
64	PC7	I/O	GPIO_EXTI7	VL53L0X_GPIO1_EXTI7
65	PC8	I/O	GPIO_EXTI8	LSM3MDL_DRDY_EXTI8
66	PC9 *	I/O	GPIO_Output	LED3_WIFI_ LED4_BLE
67	PA8 *	I/O	GPIO_Output	SPBTLE_RF_RST
68	PA9	I/O	USB_OTG_FS_VBUS	USB_OTG_FS_VBUS
69	PA10	I/O	USB_OTG_FS_ID	USB_OTG_FS_ID
70	PA11	I/O	USB_OTG_FS_DM	USB_OTG_FS_DM
71	PA12	I/O	USB_OTG_FS_DP	USB_OTG_FS_DP
72	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	SYS_JTMS_SWDIO
73	VDDUSB	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	SYS_JTCK_SWCLK
77	PA15 (JTDI) *	I/O	GPIO_Output	ARD_D9
78	PC10	I/O	SPI3_SCK	INTERNAL-SPI3_SCK [BT module_SPI_MOSI] [ISM43362_MOSI]
79	PC11	I/O	SPI3_MISO	INTERNAL_SPI3_MISO [BT module_SPI_MOSI] [ISM43362_MOSI]
80	PC12	I/O	SPI3_MOSI	INTERNAL_SPI3_MOSI [BT module_SPI_MOSI] [ISM43362_MOSI]
81	PD0 *	I/O	GPIO_Output	PMOD_RESET
82	PD1 *	I/O	GPIO_Output	PMOD_SPI2_SCK
83	PD2	I/O	GPIO_EXTI2	PMOD_IRQ_EXTI12
84	PD3	I/O	USART2_CTS	PMOD_UART2_CTS
85	PD4	I/O	USART2_RTS	PMOD_UART2_RTS
86	PD5	I/O	USART2_TX	PMOD_UART2_TX
87	PD6	I/O	USART2_RX	PMOD_UART2_RX
88	PD7 *	I/O	GPIO_Output	STSAFE_A110_RESET
89	PB3 (JTDO/TRACESWO)	I/O	SYS_JTDO-SWO	SYS_JTD0_SWO
90	PB4 (NJTRST) *	I/O	GPIO_Output	ARD_D5
91	PB5 *	I/O	GPIO_Output	SPSGRF_915_SPI3_CSN [SPSGRF_SPI_CS]
92	PB6	I/O	USART1_TX	ST-LINK-UART1_TX
93	PB7	I/O	USART1_RX	ST_LINK_UART1_RX
95	PB8	I/O	I2C1_SCL	ARD_D15 [I2C1_SCL]
96	PB9	I/O	I2C1_SDA	ARD_D14 [I2C1_SDA]

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
97	PE0 *	I/O	GPIO_Output	ISM43362_SPI3_CSN [ISM43362_SSN]
98	PE1	I/O	GPIO_EXTI1	ISM43362_DRDY_EXTI1
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	micro-ROS
Project Folder	/home/michael/repos/freertos_apps/microros_b_l4s5i_iot01a_extensions
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.0
Application Structure	Basic
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_DFSDM1_Init	DFSDM1
6	MX_I2C1_Init	I2C1
7	MX_I2C2_Init	I2C2
8	MX_OCTOSPI1_Init	OCTOSPI1
9	MX_SPI1_Init	SPI1
10	MX_SPI3_Init	SPI3
11	MX_UART4_Init	UART4

Rank	Function Name	Peripheral Instance Name
12	MX_USART1_UART_Init	USART1
13	MX_USART2_UART_Init	USART2
14	MX_USART3_UART_Init	USART3
15	MX_USB_OTG_FS_USB_Init	USB_OTG_FS

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4R5/S5
MCU	STM32L4S5VITx
Datasheet	DS12024_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

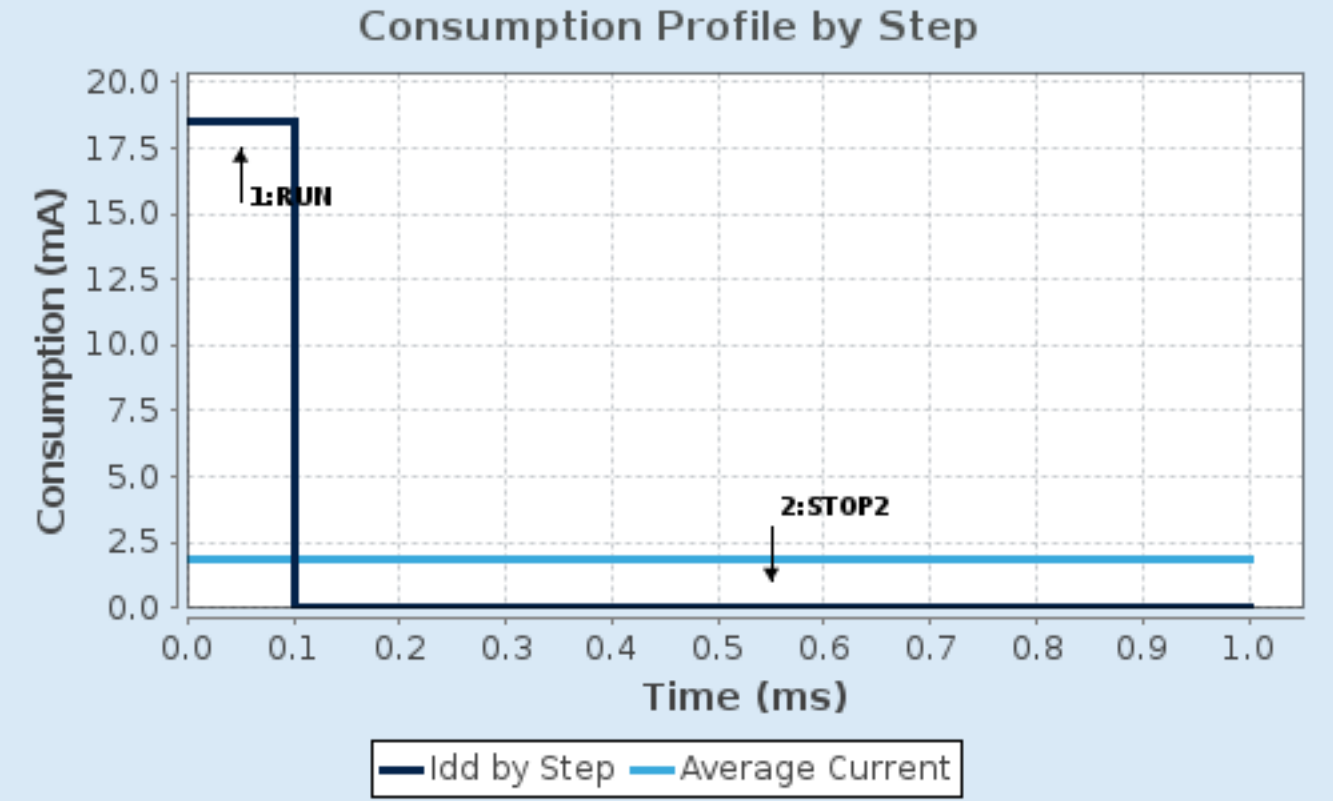
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH-SingleBank	n/a
CPU Frequency	120 MHz	0 Hz
Clock Configuration	HSE BYP PLL ART	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	18.5 mA	2.55 µA
Duration	0.1 ms	0.9 ms
DMIPS	150.0	0.0
Ta Max	102.67	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.85 mA
Battery Life	2 months, 15 days, 11 hours	Average DMIPS	150.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP2
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN13: IN13 Single-ended

IN14: IN14 Single-ended

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. DFSDM1

mode: PDM/SPI input from ch2 and internal clock

7.2.1. Filter 0:

regular channel selection:

regular channel selection	- None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

7.2.2. Filter 1:

regular channel selection:

regular channel selection	- None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

7.2.3. Filter 2:

regular channel selection:

regular channel selection	- None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable

Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

7.2.4. Filter 3:

regular channel selection:

regular channel selection	- None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

7.2.5. Output Clock:

Output Clock parameters:

Selection	Source for ouput clock is system clock
Divider	2

7.2.6. Channel 2:

Channel 2 parameters:

Type	SPI with rising edge
Spi Clock	Internal SPI clock
Offset	0
Right Bit Shift	**0x00 ***

Analog watchdog parameters:

Filter Order	FastSinc filter type
Oversampling	1

7.3. I2C1

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x307075B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. I2C2

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x307075B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled

Primary slave address	0

7.5. OCTOSPI1

Mode: Quad SPI

mode: Clock

Chip Select: Port1 NCS

Data [3:0]: Port1 IO[3:0]

7.5.1. Parameter Settings:

Generic:

Fifo Threshold	1
Dual Mode	Disable
Memory Type	**Macronix ***
Device Size	32
Chip Select High Time	1
Free Running Clock	Disable
Clock Mode	Low
Clock Prescaler	1
Sample Shifting	No Sample Shifting
Delay Hold Quarter Cycle	Disable
Chip Select Boundary	0
Delay Block Bypass	Disable

7.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
MSI Calibration Value	0

MSI Auto Calibration	Enabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1 boost

7.7. SPI1

Mode: Full-Duplex Master

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**60.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.8. SPI3

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**30.0 MBits/s ***
Clock Polarity (CPOL)	Low

Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.9. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM1

7.10. UART4

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.11. USART1

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.12. USART2

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit

Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.13. USART3

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable

DMA on RX Error	Enable
MSB First	Disable

7.14. USB_OTG_FS
Mode: OTG/Dual_Role_Device
Activate_VBUS: VBUS sensing

7.15. FREERTOS
Interface: CMSIS_V2
7.15.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**50000 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

7.15.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled

vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.15.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN1	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ARD_A5 [ADC]
	PC1	ADC1_IN2	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ARD_A4 [ADC]
	PC2	ADC1_IN3	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ARD_A3 [ADC]
	PC3	ADC1_IN4	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ARD_A2 [ADC]
	PC4	ADC1_IN13	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ARD_A1 [ADC]
	PC5	ADC1_IN14	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ARD_A0 [ADC]
DFSDM1	PE7	DFSDM1_DATIN2	Alternate Function Push Pull	No pull-up and no pull-down	Low	DFSDM1_DATIN2 [MP34DT01_DOUT]
	PE9	DFSDM1_CKOUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	DFSDM1_CKOUT [MP34DT01_CLK]
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	ARD_D15 [I2C1_SCL]
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	ARD_D14 [I2C1_SDA]
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	INTERNAL_I2C2_SCL [MEMs]
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	INTERNAL_I2C2_SDA [MEMs]
OCTOSPI1	PE10	OCTOSPIM_P1_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	QUADSPI_CLK [MX25R6435F_SCLK]
	PE11	OCTOSPIM_P1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	QUADSPI_NCS [MX25R6435F_SCLK]
	PE12	OCTOSPIM_P1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OQUADSPI_BK1_IO0 [MX25R6435F_IO0]
	PE13	OCTOSPIM_P1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	QUADSPI_BK1_IO1 [MX25R6435F_IO1]
	PE14	OCTOSPIM_P1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	QUAD_SPI_BK1_IO2 [MX25R6435F_IO2]
	PE15	OCTOSPIM_P1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	QUAD_SPI_BK1_IO3 [MX25R6435F_IO3]
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	LED1 [Green]
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARD_D12 [SPI1_MISO]
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARD_D11 [SPI1_MOSI]
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	INTERNAL-SPI3_SCK [BT module_SPI_MOSI] [ISM43362_MOSI]
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	INTERNAL_SPI3_MISO [BT module_SPI_MOSI] [ISM43362_MOSI]
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	INTERNAL_SPI3_MOSI [BT module_SPI_MOSI] [ISM43362_MOSI]
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	SYS_JTMS_SWDIO
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	SYS_JTCK_SWCLK
	PB3 (JTDO/TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	SYS_JTD0_SWO
UART4	PA0	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARD_D1 [UART4_TX]
	PA1	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARD_D0 [UART4_RX]
USART1	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ST-LINK-UART1_TX
	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ST_LINK_UART1_RX
USART2	PD3	USART2_CTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	PMOD_UART2_CTS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PD4	USART2_RTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	PMOD_UART2_RTS
	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	PMOD_UART2_TX
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	PMOD_UART2_RX
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	INTERNAL_UART3_TX [ISM43362_RX]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	INTERNAL_UART3_RX [ISM43362_TX]
USB_OTG_FS	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	USB_OTG_FS_VBUS
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USB_OTG_FS_ID
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USB_OTG_FS_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USB_OTG_FS_DP
Single Mapped Signals	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D6
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ST25DV04K_RF_DISABLE
	PE3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_OTG_FS_OVRCR_EXTI3
	PE4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ST25DV04K_GPO
	PE5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SPSGRF_915_GPIO3_EXTI5 [SPSGRF_GPIO_3]
	PE6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SPBTLE_RF_IRQ_EXTI6 [BT module_SPI_IRQ]
	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B2]
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARD_D10 [SPI_SSN]
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARD_D4
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARD_D7
	PB0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ARD_D3 [INT_EXT10]
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARD_D8
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ISM43362_RST

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ISM43362_BOOT0
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ISM43362_WAKEUP
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2 [LED_GREEN]
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPSGRF_915_SDN [SPSGRF_SDN]
	PD10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	LPS22HB_INT_DRDY_EXTI10
	PD11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	LSM6DSL_INT1_EXTI11
	PD12	GPIO_EXTI12	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_OTG_FS_PWR_EN
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPBTLE_RF_SPI3_CSN [BT module_SPI_CS]
	PD14	GPIO_EXTI14	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ARD_D2 [INT0_EXTI14]
	PD15	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	HTS221_DRDY_EXTI15
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VL53L0X_XSHUT
	PC7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	VL53L0X_GPIO1_EXTI7
	PC8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	LSM3MDL_DRDY_EXTI8
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3_WIFI_ LED4_BLE
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPBTLE_RF_RST
	PA15 (JTDI)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARD_D9
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PMOD_RESET
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PMOD_SPI2_SCK
	PD2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	PMOD_IRQ_EXTI12
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STSAFE_A110_RESET
	PB4 (NJTRST)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARD_D5
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPSGRF_915_SPI3_CSN [SPSGRF_SPI_CS]
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ISM43362_SPI3_CSN [ISM43362_SSN]
	PE1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ISM43362_DRDY_EXTI1

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel1	Peripheral To Memory	**Very High ***
USART1_TX	DMA1_Channel2	Memory To Peripheral	**Very High ***

USART1_RX: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 channel1 global interrupt	true	5	0
DMA1 channel2 global interrupt	true	5	0
EXTI line[9:5] interrupts	true	5	0
TIM1 update interrupt and TIM16 global interrupt	true	0	0
USART1 global interrupt	true	5	0
USART2 global interrupt	true	5	0
USART3 global interrupt	true	5	0
EXTI line[15:10] interrupts	true	5	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
EXTI line1 interrupt	unused		
EXTI line2 interrupt	unused		
EXTI line3 interrupt	unused		
EXTI line4 interrupt	unused		
ADC1 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
DFSDM1 filter3 global interrupt	unused		
SPI3 global interrupt	unused		
UART4 global interrupt	unused		
DFSDM1 filter0 global interrupt	unused		
DFSDM1 filter1 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
DFSDM1 filter2 global interrupt	unused		
OCTOSPI1 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

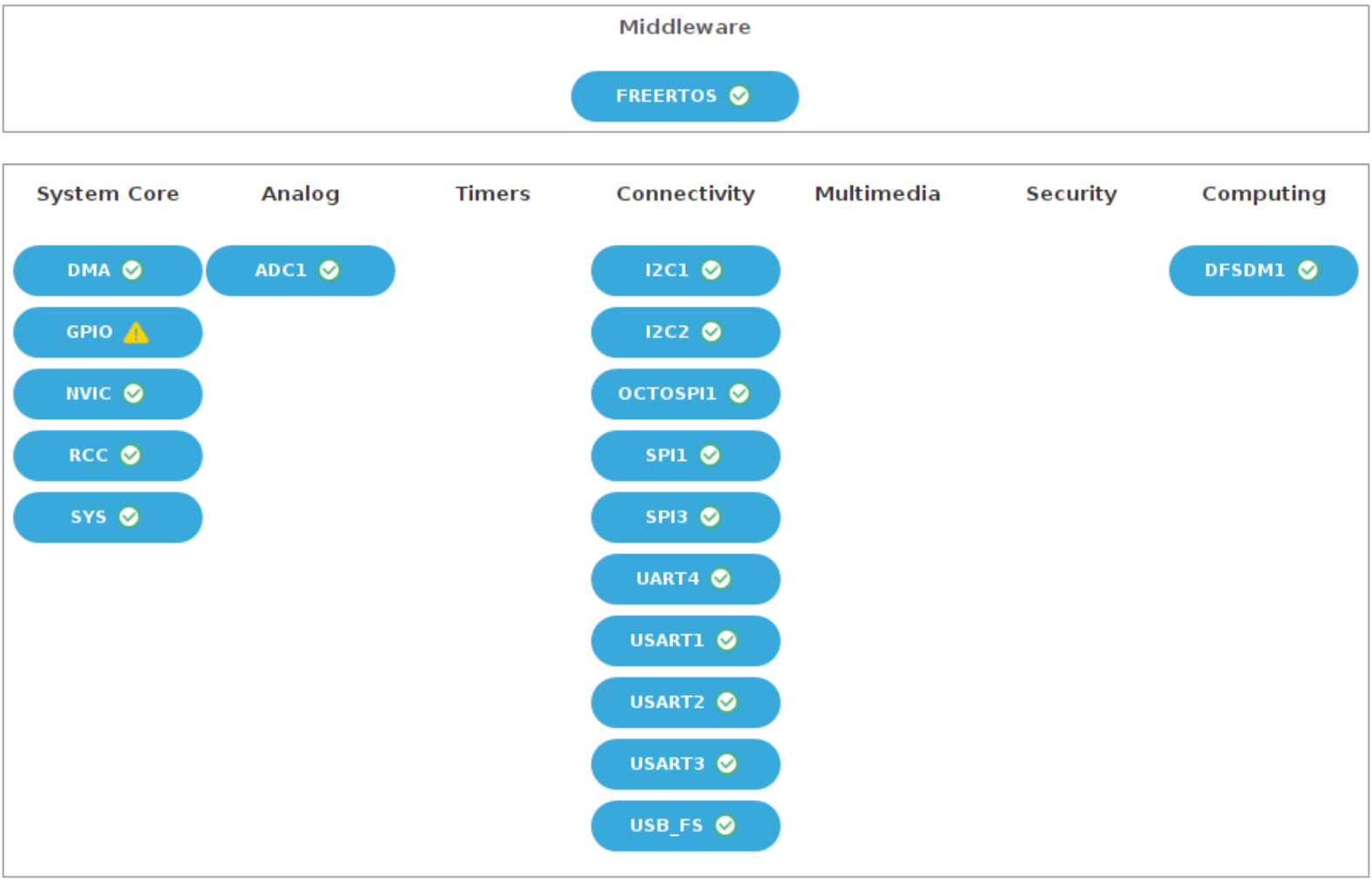
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true
TIM1 update interrupt and TIM16 global interrupt	false	true	true
USART1 global interrupt	false	true	true
USART2 global interrupt	false	true	true
USART3 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00366449.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00310109.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00371862.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00156964.pdf
Application note	http://www.st.com/resource/en/application_note/DM00150423.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209748.pdf

Application note	http://www.st.com/resource/en/application_note/DM00125306.pdf
Application note	http://www.st.com/resource/en/application_note/DM00141025.pdf
Application note	http://www.st.com/resource/en/application_note/DM00144612.pdf
Application note	http://www.st.com/resource/en/application_note/DM00148033.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209768.pdf
Application note	http://www.st.com/resource/en/application_note/DM00216518.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00269143.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00260952.pdf
Application note	http://www.st.com/resource/en/application_note/DM00263732.pdf
Application note	http://www.st.com/resource/en/application_note/DM00269146.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00338361.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00311483.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00367673.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00407776.pdf
Application note	http://www.st.com/resource/en/application_note/DM00407777.pdf
Application note	http://www.st.com/resource/en/application_note/DM00371863.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00445657.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209772.pdf
Application note	http://www.st.com/resource/en/application_note/DM00476869.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660597.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf