

Design Project 1

ENSC 350-1261

Group #: G30

Member 1: Mike Nguyen

SID: 301545780

Member 2: Mitchel Jennings

SID: 301563397

Member 3: Brayden Yip

SID: 301601372

**Project Submitted in Partial Fulfillment of the
Requirements for ENSC 350
Towards a Bachelor Degree in Engineering Science**

Spring 2026

Table of Contents

Section Title	Page
1. Objectives	
2. Specifications	
2.1 DUT — Adder Entity	
2.2 Verification — Testbench Specification	
3. General Tasks	
3.1 Design Project Setup	
3.2 Baseline Device	
3.3 Design Candidates	
3.4 Testbench Design	
3.5 Iterative Experiments (Synthesis & Simulation)	
4. Analysis of Results	
4.1 Analysis of Cost	
5. Appendices (Placeholders)	

1. Objectives

1.1 Main Objectives

Type: Text

Purpose: State the main objectives of DP1 at a high level.

Links to previous content: Opens the report; frames scope for specs and tasks.

- Placeholder: objective bullets (manager/engineer facing).
- Placeholder: what success looks like for DP1 stage.

1.2 Sub-Objectives

Type: Bullet list

Purpose: List measurable sub-objectives guiding implementation + verification + documentation.

Links to previous content: Expands from main objectives into actionable aims.

- Placeholder: verification-driven approach.
- Placeholder: baseline vs advanced candidate comparison goals.

2. Specifications

2.1 DUT — Adder Entity Requirements *Type: Text + (optional) small interface box*

Purpose: Define the DUT interface and key functional requirements.

Links to previous content: Depends on objectives; constrains all design candidates.

- Placeholder: N-bit combinational adder, Cin/Cout, Ovfl.
- Placeholder: assumptions/constraints (e.g., N power of 2).

2.2 Verification — Testbench Specification

Type: Text + bullets

Purpose: Specify test vector format, checking requirements, and transcript expectations.

Links to previous content: Links DUT spec to verification approach used later.

- Placeholder: vector file format line = {A,B,Cin,S,Cout,Ovfl}.
- Placeholder: pass/fail reporting format and measurement index.

3. General Tasks

3.1 Design Project Setup

Type: Flowchart placeholder + bullets

Purpose: Describe folder hierarchy + tool project setup plan.

Links to previous content: Connects specs to actual workflow and reproducibility.

- Placeholder: directory tree diagram (DP1 structure).
- Placeholder: ModelSim/Questa project setup (DP1.mpf).
- Placeholder: Quartus project setup (DP1.qpf).

3.2 Baseline Device

Type: Diagram placeholder + bullets

Purpose: Outline baseline ripple adder plan and why it is used for normalization.

Links to previous content: Builds on setup; establishes reference for later comparisons.

- Placeholder: architecture naming (Baseline vs FastRipple).
- Placeholder: what “baseline cost/perf” metrics will be recorded.

3.3 Design Candidates

Type: Table placeholder + bullets

Purpose: Outline the chosen additional topology(ies) and naming convention.

Links to previous content: Extends baseline into comparison candidates.

- Placeholder: candidate list (topology/implementation pairs).
- Placeholder: target FPGA devices and why.
- Placeholder: naming scheme (Arch + FPGA + candidate ID).

3.4 Testbench Design*Type: Flowchart placeholder + bullets***Purpose:** Outline testbench structure, file I/O, timing parameters, and reporting.**Links to previous content:** Connects verification spec to implementation plan.

- Placeholder: process diagram (stimulus, check, report).
- Placeholder: constants (file name, PreStimTime, PostStimTime).
- Placeholder: wave window organization plan (dividers, formats).

3.5 Iterative Experiments (Synthesis & Simulation) *Type: Procedure outline + bullets***Purpose:** Show intended repeatable experiment flow using scripts and captured outputs.**Links to previous content:** Builds on setup+testbench to produce evidence for analysis section.

- Placeholder: synthesis run checklist per candidate.
- Placeholder: simulation script checklist (compile, run, transcript).
- Placeholder: artifacts to save (transcripts, summary snippets).

4. Analysis of Results

4.1 Analysis of Cost

Type: Table placeholder + bullets

Purpose: Define how cost will be predicted/measured and compared across candidates.

Links to previous content: Consumes results from iterative experiments; leads to conclusions later.

- Placeholder: predicted vs actual resource estimates (Cyclone IV LEs).
- Placeholder: Arria II ALM-to-LE conversion factor plan.
- Placeholder: normalized comparison table structure.

5. Appendices (Placeholders)

A. Figures List Placeholder

Type: List placeholder

Purpose: Reserve space for figure numbering + captions used in DP1.1+.

Links to previous content: References figures used in sections 3–4.

B. Tables List Placeholder

Type: List placeholder

Purpose: Reserve space for tables (candidate summary, cost comparison, etc.).

Links to previous content: References tables introduced in sections 3–4.

C. File Naming / Directory Map Placeholder

Type: Table placeholder

Purpose: Reserve space for a “where each file goes” mapping table (if needed later).

Links to previous content: Links to reproducibility and documentation requirements.