DP1.0 Summary Report Outline

Group: G30 **Term:** Spring 2026
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1. Project Overview & Objectives *Type: Text*
Purpose: Briefly inform the Engineering Manager what DP1 is and what DP1.0 delivers.
Links to previous content: Opening section; sets context for status, plan, risks, and next steps.

- Project scope: 64-bit adder design candidates + verification + synthesis cost comparison.
- DP1.0 deliverable focus: organization, filing structure, report outlines, activity logging setup.
- Manager-facing emphasis: readiness to execute DP1.1 efficiently (repeatable workflow).

2. Current Status (DP1.0) *Type: Text + Bullets*
Purpose: Summarize progress vs. plan for DP1.0 tasks.
Links to previous content: Builds on overview; tells "what is done" and "what remains".

- Filing hierarchy created (DP1 root + required subfolders).
- Report outline structures defined for Summary + Project Report.
- Activity logs initiated for each group member (DP1.0 worksheet entries started).
- Toolchain prep planned/started (Quartus + ModelSim/Questa project setup).

3. Technical Plan (Design Candidates) *Type: Bulleted Plan*
Purpose: Outline intended design candidates/topologies without implementation detail.
Links to previous content: Follows status; transitions into how work will be executed.

- Baseline: 64-bit ripple adder (reference for normalization).
- Additional candidate(s): conditional-sum / carry-select style topology (and others if chosen).
- Naming convention: architecture + FPGA target identifier.
- Target devices: Cyclone IV (LE/LUT baseline) and Arria II (ALM comparison).

4. Verification & Experiment Plan *Type: Bulleted Plan*
Purpose: Describe planned verification workflow (test vectors, testbenches, scripts, transcripts).
Links to previous content: Builds on technical plan; explains how correctness will be ensured.

- Shared test vector file format for all DUTs (A,B,Cin,S,Cout,Ovfl).
- Two testbenches (one per topology) reading vectors from file.
- Scripts to compile, run sims, and capture transcripts for traceability.
- Waveform organization approach (dividers, formats, saved wave scripts).

5. Cost Analysis Plan *Type: Bulleted Plan*
Purpose: Show how cost will be estimated and compared across candidates/devices.
Links to previous content: Follows verification plan; transitions to synthesis + metrics.

- Cost metric: Cyclone IV 4-input LUTs / LEs for baseline comparisons.
- Predicted vs. actual resource tables per design candidate.

- Arria II ALM-to-LE conversion factor estimate and justification.
- Normalized comparison table (baseline as reference).

6. Risks, Constraints, Mitigation *Type: Bullets*
Purpose: Identify likely blockers and how the team will reduce schedule/quality risk.
Links to previous content: Reflects on the plan; helps manager anticipate issues.

- Toolchain setup friction (versions, project settings) → mitigate via checklist + scripts.
- Verification completeness risk → mitigate via structured vector strategy + transcripts.
- Schedule risk (advanced topology debug) → mitigate via incremental bring-up (baseline first).

7. Next Steps (DP1.1) *Type: Bulleted Milestones*
Purpose: List immediate next actions and expected artifacts for DP1.1.
Links to previous content: Final section; closes the outline with forward plan.

- Implement baseline ripple adder (Baseline + FastRipple architectures).
- Implement selected advanced topology (e.g., conditional-sum).
- Build testbenches + generate/validate test vector files.
- Run synthesis + simulations; collect Quartus summaries + ModelSim transcripts.
- Expand outline into full Summary + Report documents.