1. Description

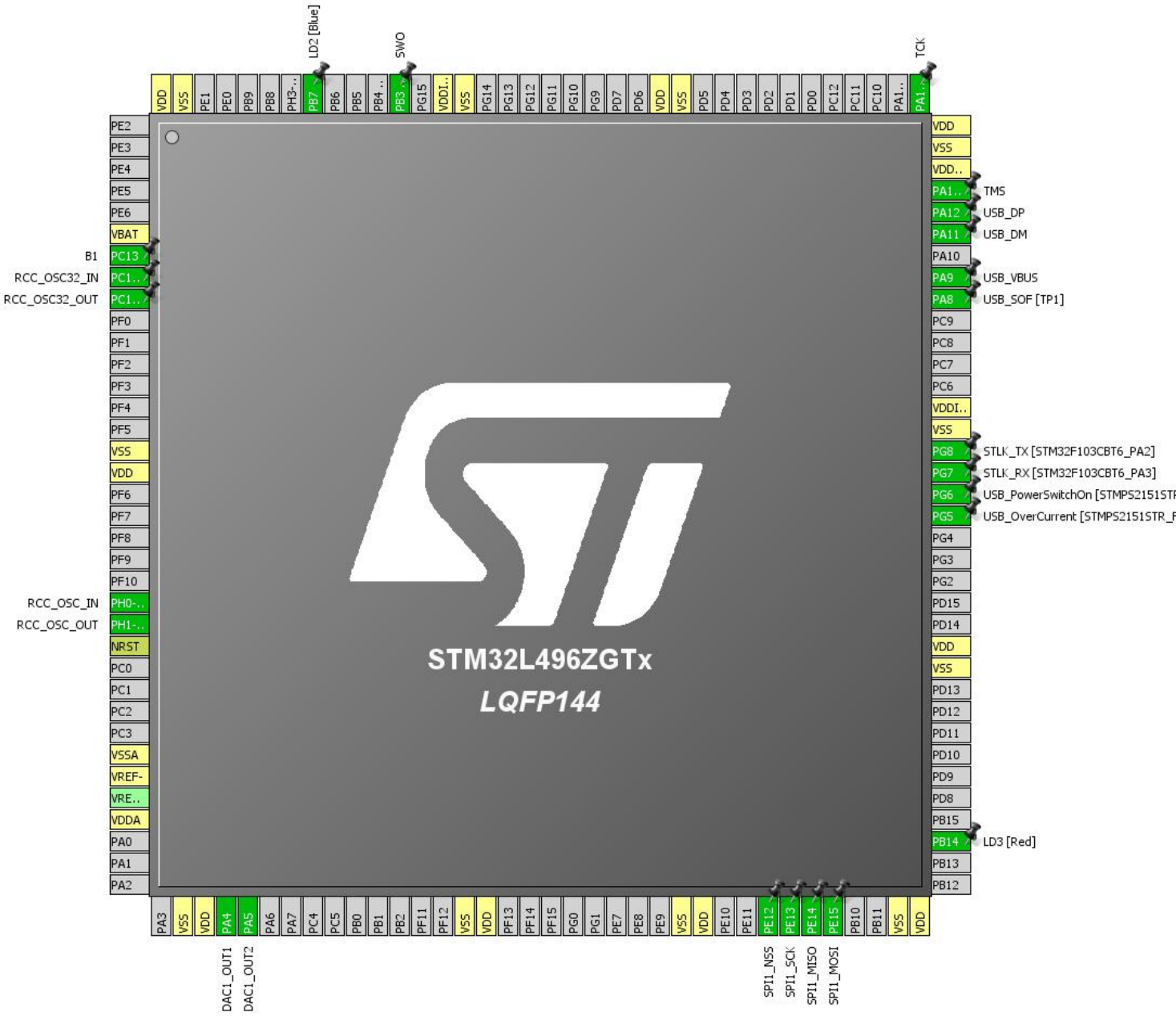
1.1. Project

Project Name	L496Midi
Board Name	NUCLEO-L496ZG
Generated with:	STM32CubeMX 4.25.0
Date	05/06/2018

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L496ZGTx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



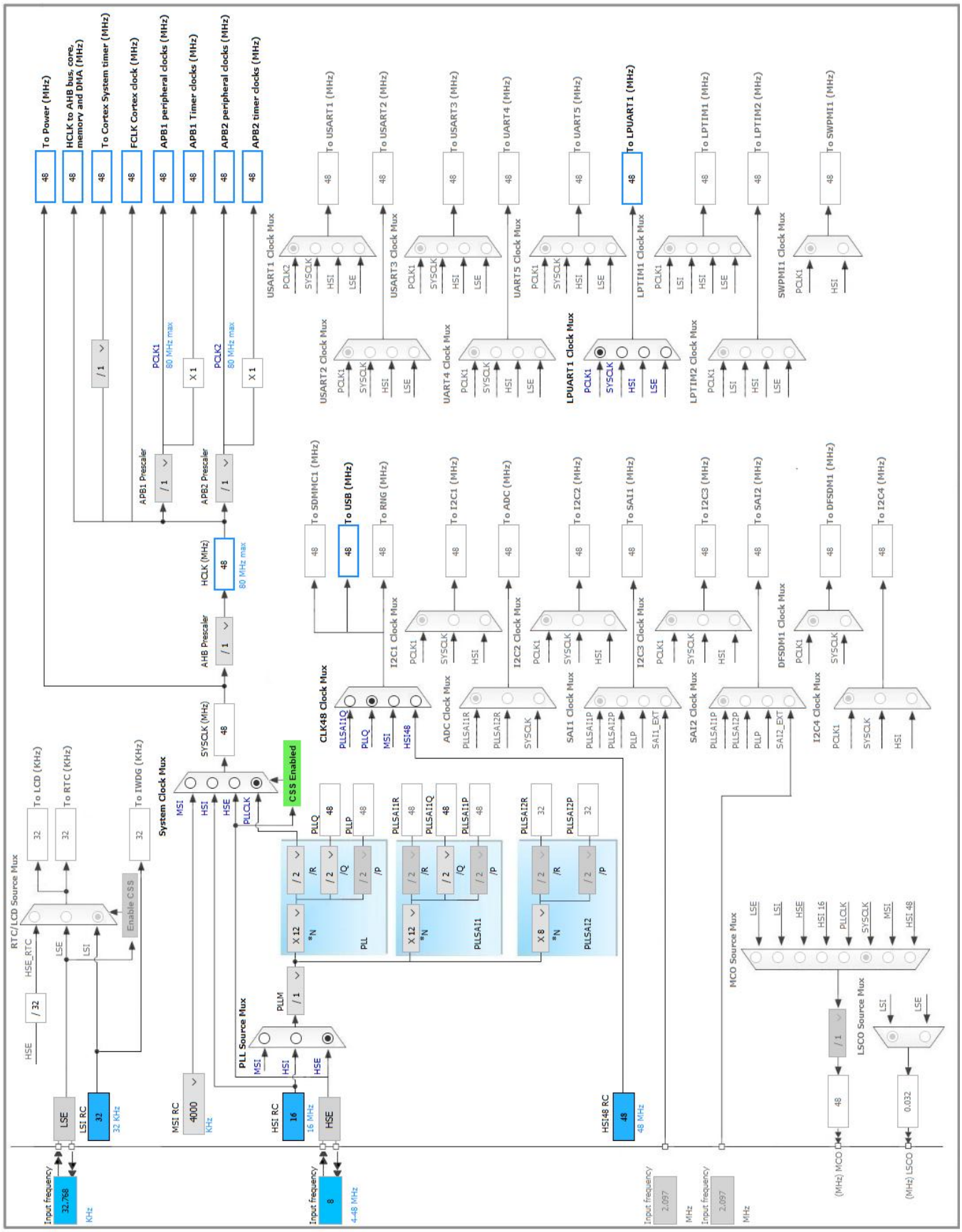
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	B1
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VSSA	Power		
31	VREF-	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC1_OUT1	
41	PA5	I/O	DAC1_OUT2	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
65	PE12	I/O	SPI1_NSS	
66	PE13	I/O	SPI1_SCK	
67	PE14	I/O	SPI1_MISO	
68	PE15	I/O	SPI1_MOSI	
71	VSS	Power		
72	VDD	Power		
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
83	VSS	Power		
84	VDD	Power		
90	PG5 *	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7	I/O	LPUART1_TX	STLK_RX [STM32F103CBT6_PA3]

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
93	PG8	I/O	LPUART1_RX	STLK_TX [STM32F103CBT6_PA2]
94	VSS	Power		
95	VDDIO2	Power		
100	PA8	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9	I/O	USB_OTG_FS_VBUS	USB_VBUS
103	PA11	I/O	USB_OTG_FS_DM	USB_DM
104	PA12	I/O	USB_OTG_FS_DP	USB_DP
105	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDDIO2	Power		
133	PB3 (JTDO/TRACESWO)	I/O	SYS_JTDO-SWO	SWO
137	PB7 *	I/O	GPIO_Output	LD2 [Blue]
143	VSS	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. DAC1

OUT1 mode: Connected to external pin only
OUT2 mode: Connected to external pin only

5.1.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

5.2. LPUART1

Mode: Asynchronous

5.2.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	**9 Bits (including Parity) ***
Parity	**Even ***
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable

Advanced Features:

Auto Baudrate Mode	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable

Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

5.4. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***

First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**12.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware

5.5. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

5.6. USB_OTG_FS

Mode: Device_Only

Activate_VBUS: VBUS sensing

mode: Activate_SOF

5.6.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	Enabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Enabled
Signal start of frame	Enabled

5.7. USB_DEVICE

Class For FS IP: Audio Device Class

5.7.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	**3: All messages and internal debug messages are shown ***
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USBD_AUDIO_FREQ (Audio sample frequency rate)	22100

5.7.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Audio Class
SERIALNUMBER_STRING (Serial number)	00000000001A
CONFIGURATION_STRING (Configuration Identifier)	AUDIO Config
INTERFACE_STRING (Interface Identifier)	AUDIO Interface

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
LPUART1	PG7	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	STLK_RX [STM32F103CBT6_PA3]
	PG8	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	STLK_TX [STM32F103CBT6_PA2]
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PE12	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE13	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE14	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE15	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PB3 (JTDO/TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	USB_SOF [TP1]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	USB_VBUS
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USB_DP
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B1
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]

6.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_RX	DMA1_Channel2	Peripheral To Memory	**High ***
SPI1_TX	DMA1_Channel3	Memory To Peripheral	**High ***
LPUART_TX	DMA2_Channel6	Memory To Peripheral	Low
DAC_CH1	DMA2_Channel4	Memory To Peripheral	Low
DAC_CH2	DMA1_Channel4	Memory To Peripheral	Low

SPI1_RX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI1_TX: DMA1_Channel3 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

LPUART_TX: DMA2_Channel6 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

DAC_CH1: DMA2_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***

Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

DAC_CH2: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA2 channel4 global interrupt	true	0	0
USB OTG FS global interrupt	true	0	0
DMA2 channel6 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
SPI1 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	unused		
LPUART1 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L496ZGTx
Datasheet	029173_Rev2

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	L496Midi
Project Folder	C:\Users\mariu\Documents\STM32 Projects\L496Midi
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_L4 V1.11.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report