CS 272: Lab 5

Due: Wednesday, November 22, 2017

Name: _____ _____ **/ 10 pts.**

The purpose of this lab is to use 4000 series CMOS digital logic to implement an arbitrary logic function. This lab will not use a microcontroller, but does show how digital logic circuit blocks can be cascaded to build larger digital logic circuits. CS 370 will pick up with this concept to build entire processors.

1. (*10 points*)

The circuit that you must build for this lab can be described by the truth table below. It is up to you to determine which logic gates should be used, and how they should be arranged in order to implement the correct functionality. Note that our lab stockpile has AND, OR, and NOT (inverter) logic chips. You may want to stick to using just those circuits, although you can build other logic functions (for example, XOR) using AND, OR, and NOT as building blocks. You can safely use sum-of-products to derive the circuit, however if you think that you have a more efficient implementation, you are free to implement the function however you wish. Show your work (the digital logic circuit diagram) below.

Work:

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

The following table lists all of the digital logic chips that we have in the lab. Notice that the AND and OR chips are functions of two single bit inputs. If you have any logic gates that require three or four single bit inputs, then you will need to cascade the output of a gate to the input of another gate. For example, if you need an OR3, then you could OR2 two of the inputs, and the output of that OR2 can be fed to the input of a second OR2 (along with the third input).

Note that the last two chips listed in the table have configurable functionality. You can use either of these chips if you wish, but it is not required for this lab. You can read the datasheet to understand

Part Number	Type	Datasheet URL
4081	AND2	`http://www.ti.com/lit/ds/symlink/cd4073b.pdf`
4071	OR2	`http://www.ti.com/lit/ds/symlink/cd4071b.pdf`
4049	NOT	`http://www.ti.com/lit/ds/symlink/cd4049ub.pdf`
4019	AND/OR	`http://www.ti.com/lit/ds/symlink/cd4019b.pdf`
4048	Multifunction	`http://www.ti.com/lit/ds/symlink/cd4048b.pdf`

how to configure these chips.

You should implement the circuit that you designed above. You can look at the datasheets for the various parts to see their pin assignments. You will probably need two breadboards. Remember that there are multiple gates on a single chip – for example, the 4081 has four AND2 gates that are independent of each other. You should use all gates on one chip before you use a second (if needed). Because these chips are CMOS logic, you can cascade without having to worry about limiting current through a resistor between logic gates. You should supply all of these circuits with a 9V battery.

The input (A, B, and C) for these chips should come from a set of DIP switches. The DIP switch is a SPST switch, just like our push-buttons, with the exception that they are not momentary. Instead, they are toggle – you move the switch in one direction to turn the switch on, and it will stay in that position until you move the switch in the other direction. Since these are similar to our SPST push-buttons, you will similarly need to use either a pull-up or pull-down resistor *for each switch* – you cannot share a pull-up or pull-down among all switches, unfortunately. The DIP switches that we have in the lab have 8 switches, but we only need to use three of the switches for this lab. You can leave the other five switches unconnected.

The output of this lab is a single bit, Z. To make this easier to visualize, you can tie the output to an LED (whatever color, your choice). Please be sure to use a current limiting resistor. The output of the final stage will be 9V, so you should can use a 1kΩ resistor to limit current.

Demonstrate that the circuit matches the above truth table for all values of A, B, and C. Instructor signature: _____

Submit this worksheet with your circuit schematic for grading.