

# Jetson TX1/TX2 Developer Kit Carrier Board

## Supports Jetson TX1/TX2/TX2i

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P2597 I2C Port Assignments

Slave Device	BUS:Device address
INA3221 (Power measurement)	I2C Gen 2 : 7h42
INA3221 (Power measurement)	I2C Gen 2 : 7h43
TCA9539 (GPIO Expander)	I2C Gen 2 : 7h74
TCA9539 (GPIO Expander)	I2C Gen 2 : 7h77
BOARDID EEPROM	I2C Gen 3 : 757h

P2180 I2C Port Assignments

Slave Device	BUS:Device address
TMP451 (Thermal)	I2C Gen 1 : 7h4C
ADS1015 (ACA detection)	I2C Gen 2 : 7h4A
INA226 (Power measurement)	I2C Gen 2 : 7h46
INA3221 (Power measurement)	I2C Gen 2 : 7h40

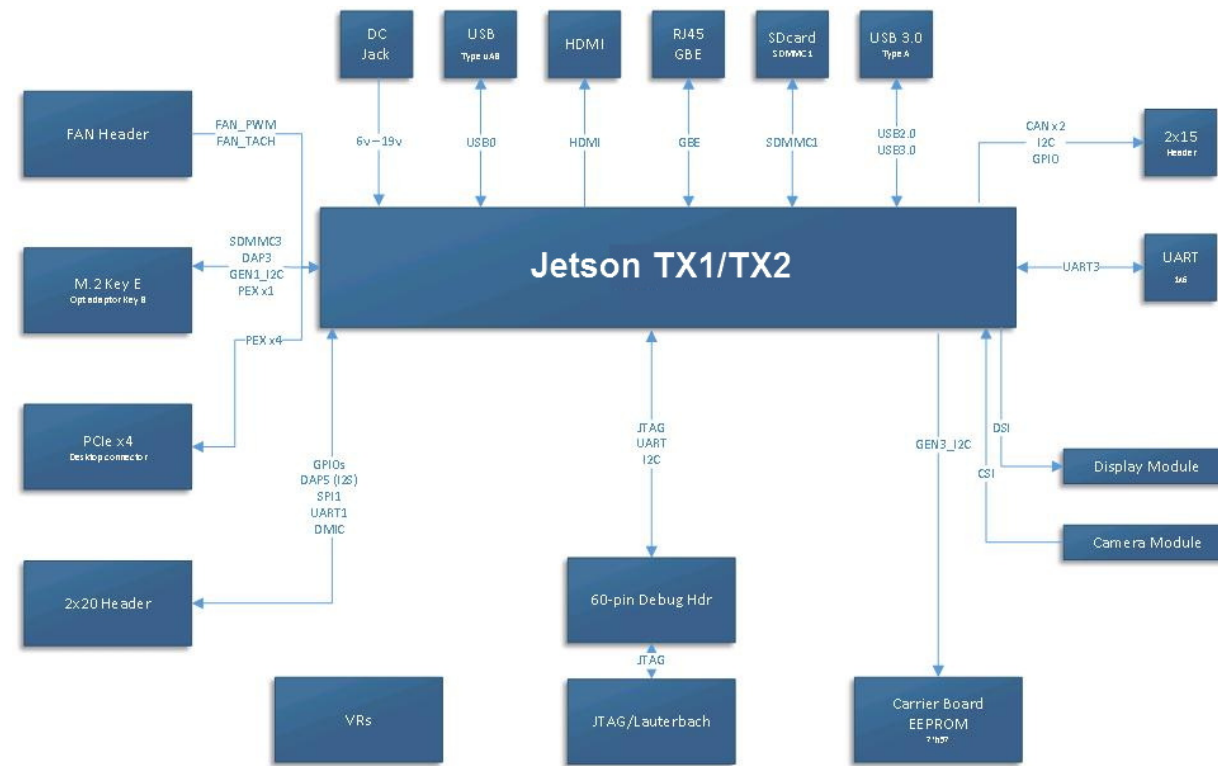
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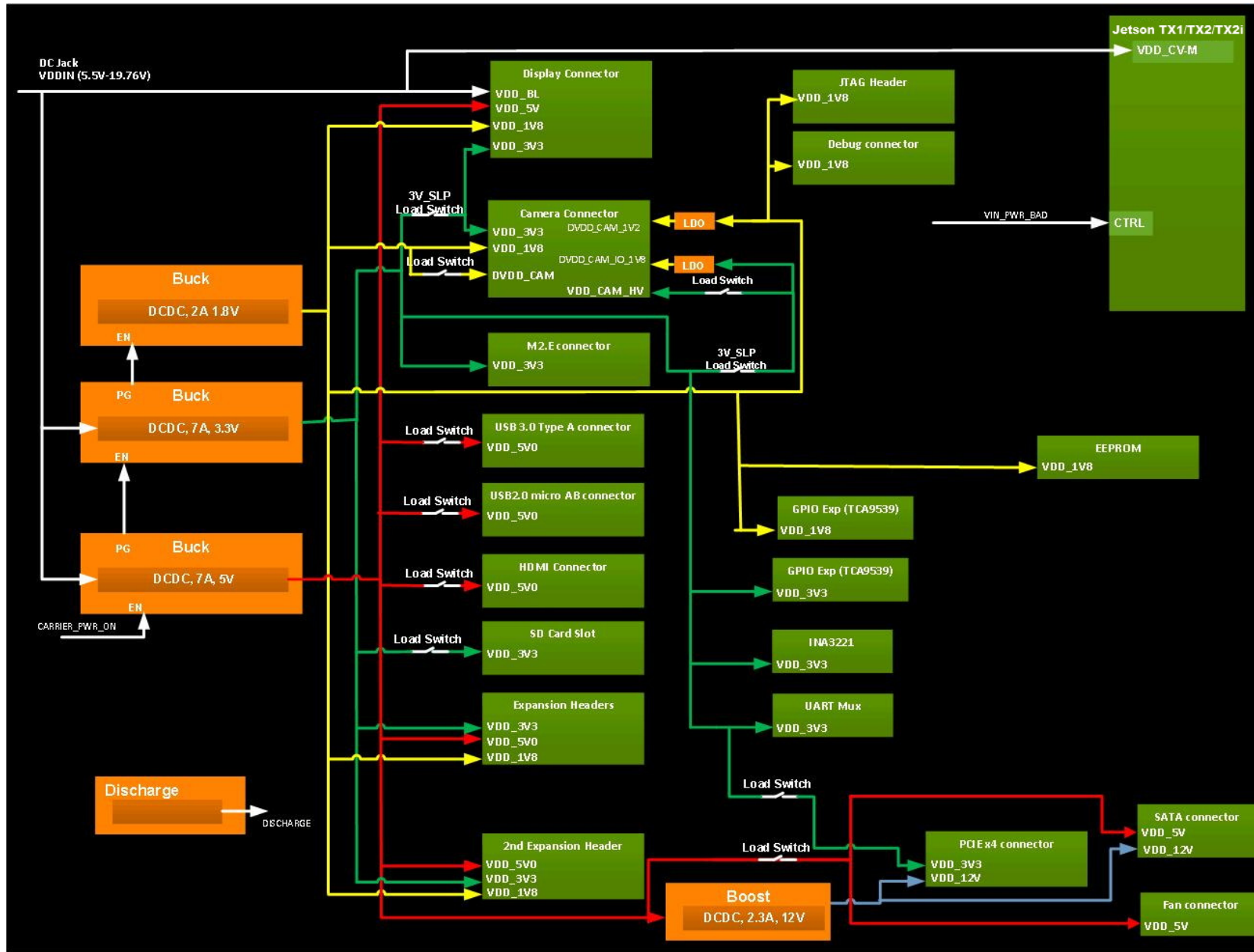
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# Power Tree



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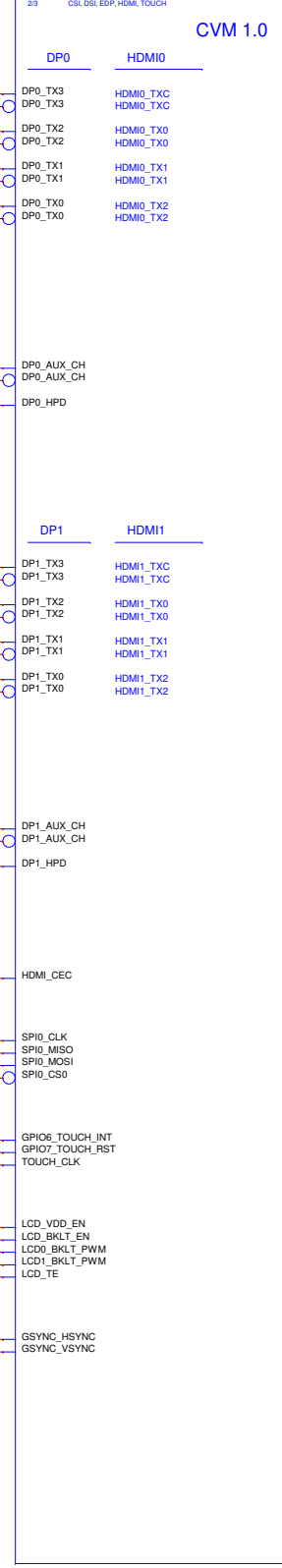
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J13A  
SEAM-50-02.0-S-08-2-A-K-TR  
CVM 1X0  
COMMON



TO DISPLAY MODULE  
SPI TOUCH  
SP4 (Tegra X1)

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO connector 2/3

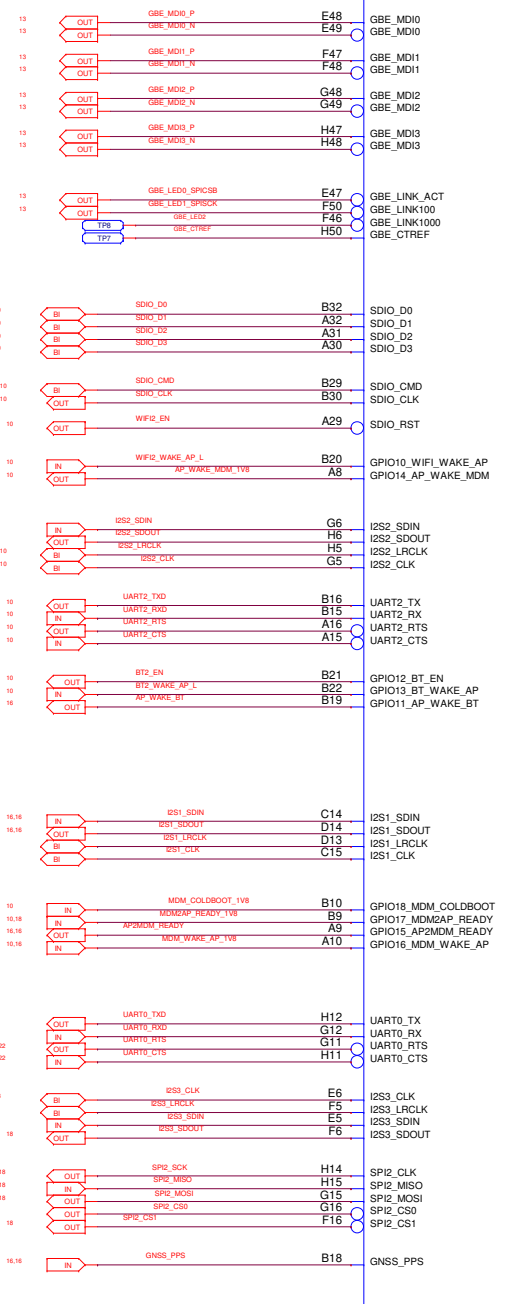
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J138  
SEAM 50-Q2.0-S-08-2-A-K-TR  
CVM\_8X50  
COMMON

33 GBE, WIFI, BT, MODEM, GPS, PCIe, SATA, USB

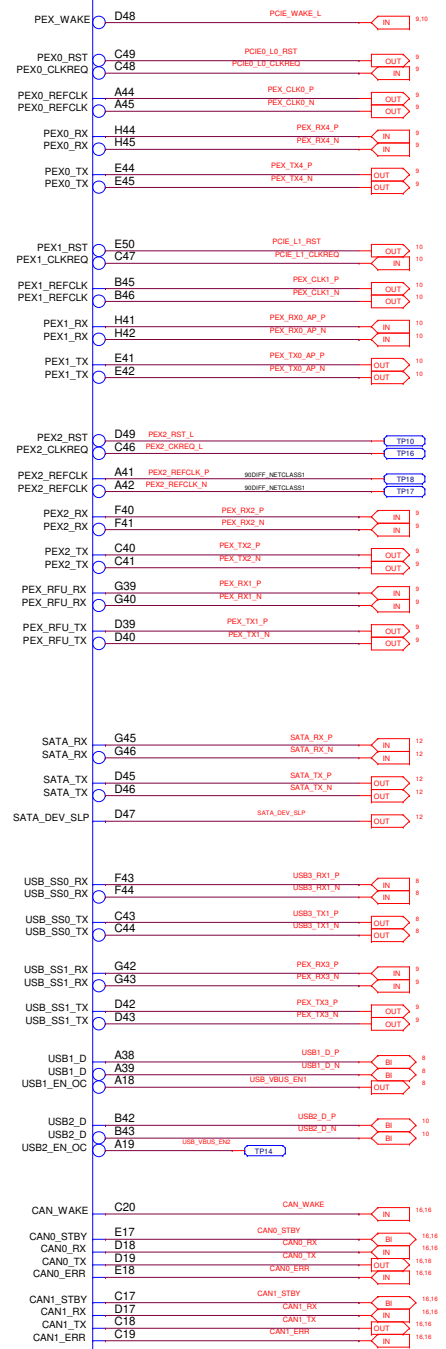
CVM 1.0



WIFI

BT

MODEM



It is recommended that any unused USB 3.0, PCIe or SATA RX lanes should be connected to GND.

Pin B16(UART2\_TX) is associated with RAM\_CODE3 strapping option in Jetson TX2(i).  
Pin A16(UART2\_RTS) is associated with RAM\_CODE2 strapping option in Jetson TX2(i).

These pins must be handled carefully to avoid changing the strapping levels during power-on which could cause the platform to malfunction. See the Jetson TX1/TX2(i) OEM DGs for details.

Pin H12(UART0\_TX) is associated with RAM\_CODE3 strapping option in Jetson TX1.  
Pin G11(UART0\_RTS) is associated with RAM\_CODE5 strapping option in Jetson TX1/TX2(i).

ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> IO connector 3/3
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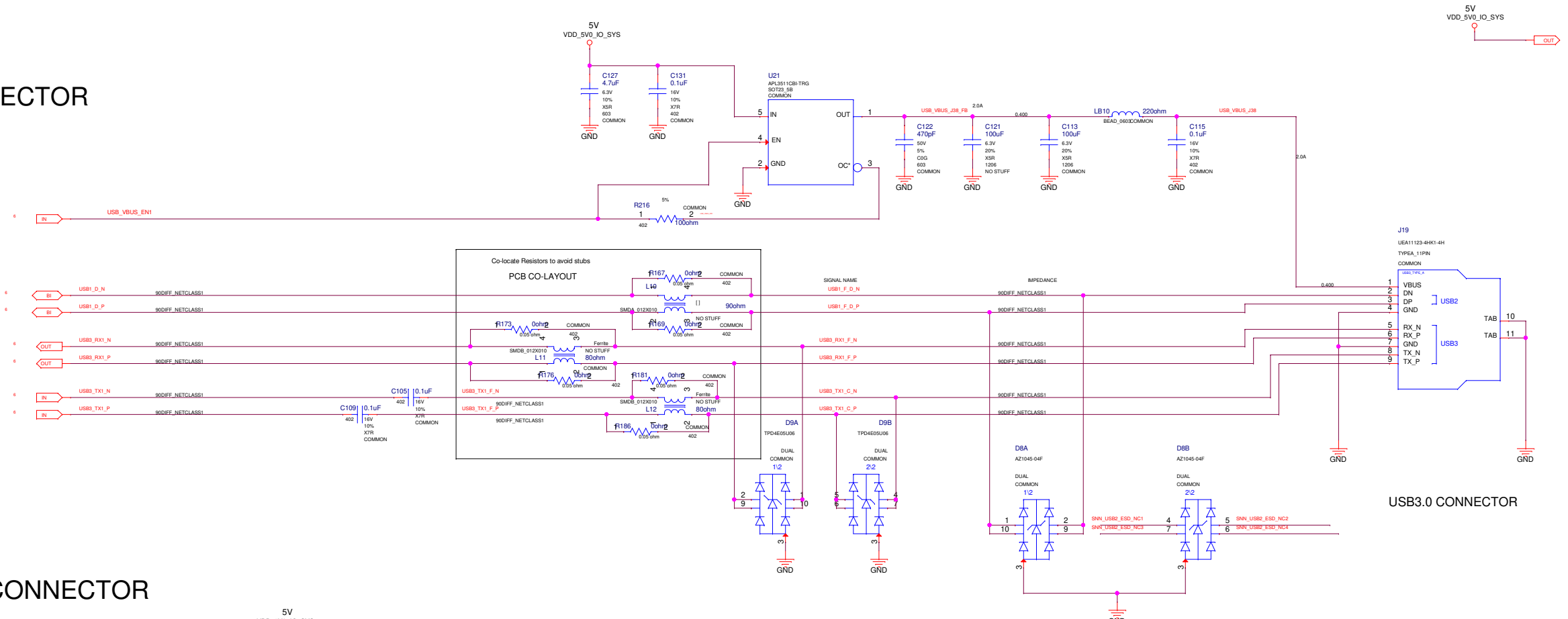
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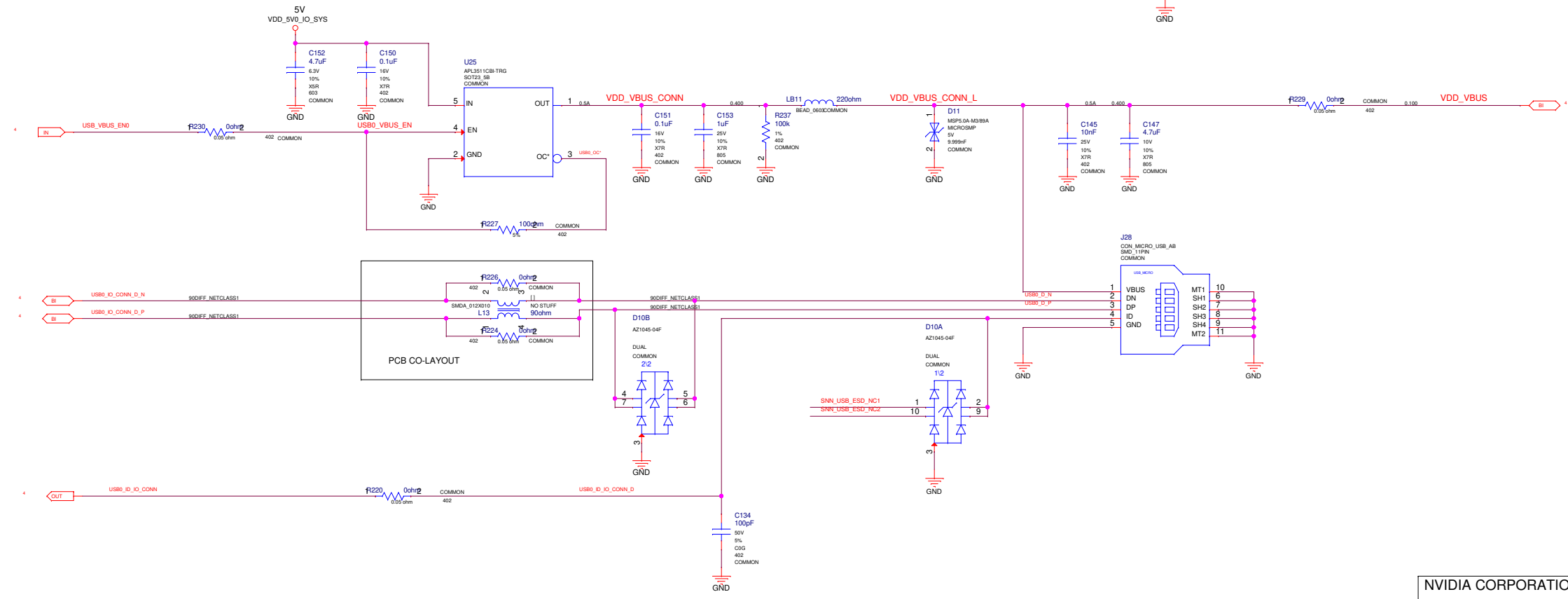
A B C D E F G H

# USB 3.0 TYPE A CONNECTOR



USB3.0 CONNECTOR

# MICRO AB USB 2.0 CONNECTOR



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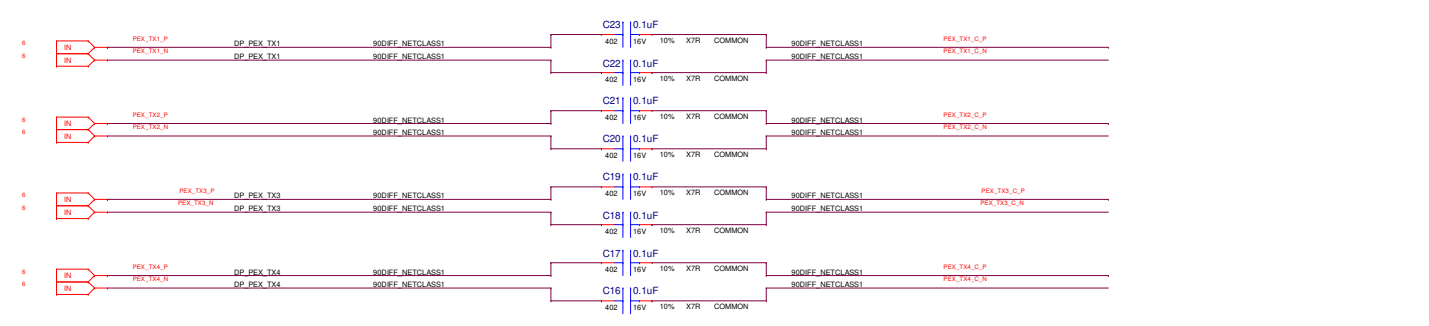
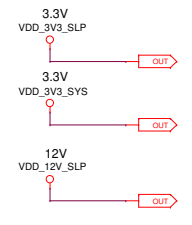
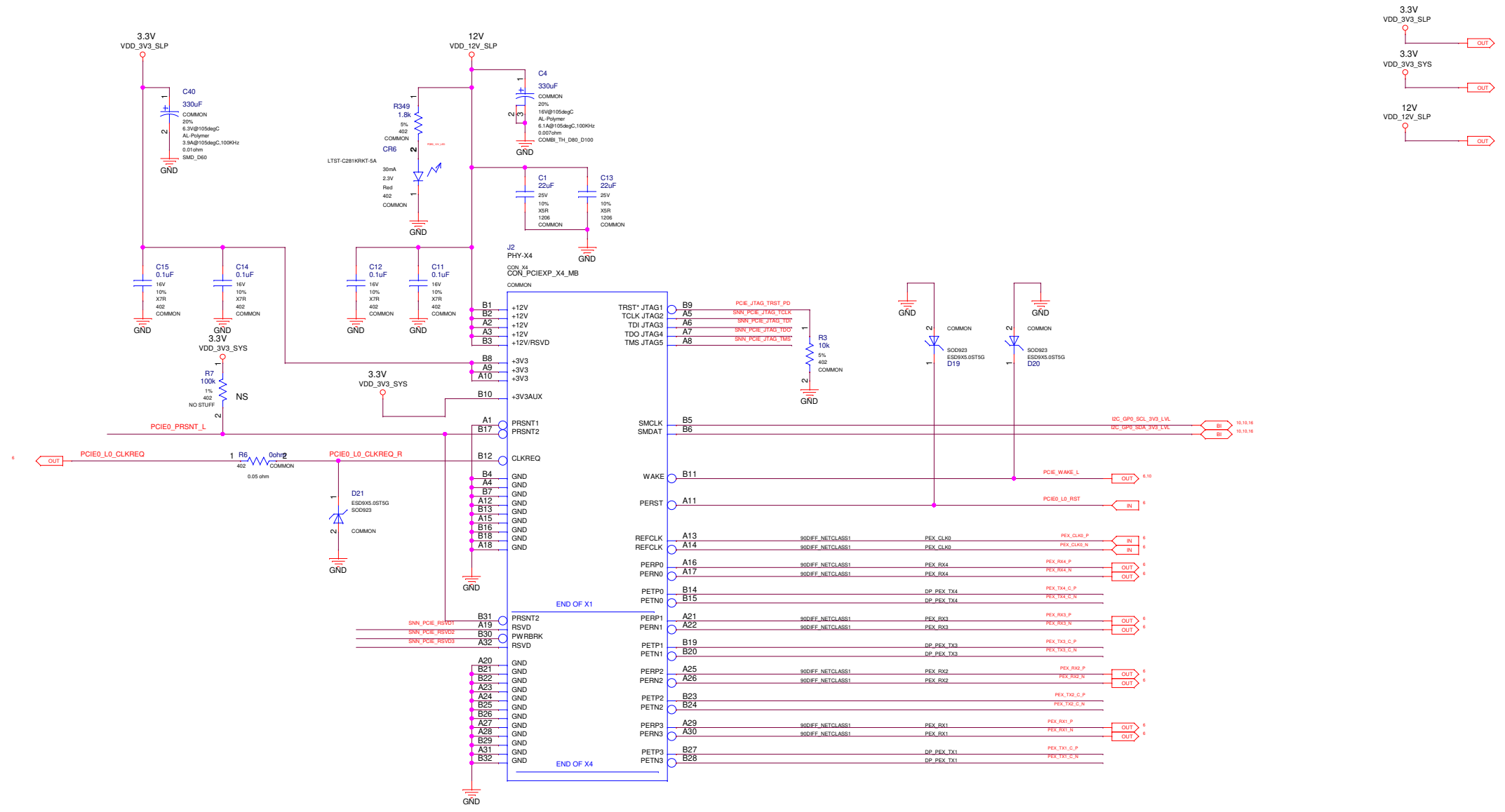
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PAGE DETAIL	USB3.0 type A and USB2.0 micro

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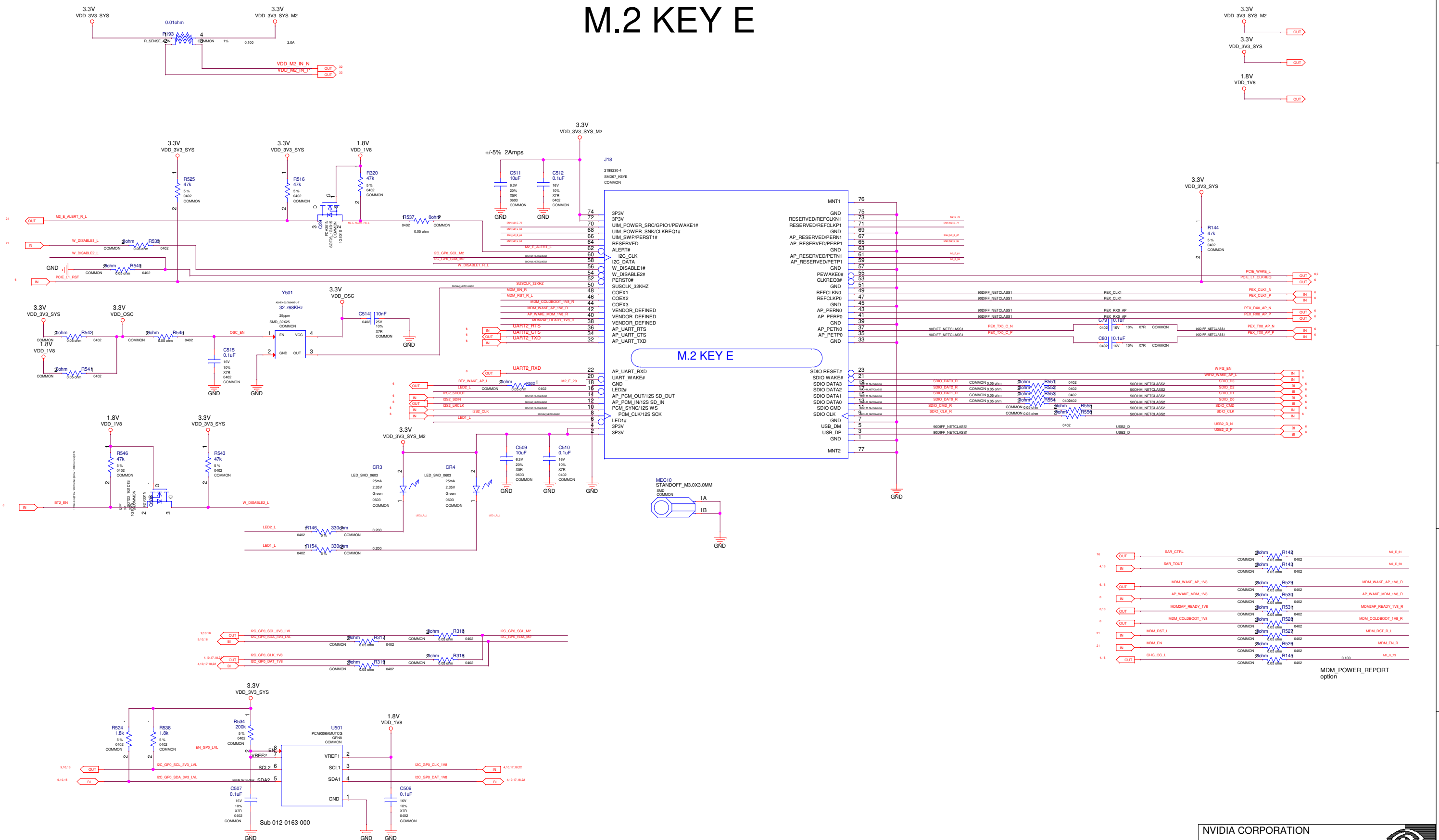


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCIe v4 Connector

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# M.2 KEY E



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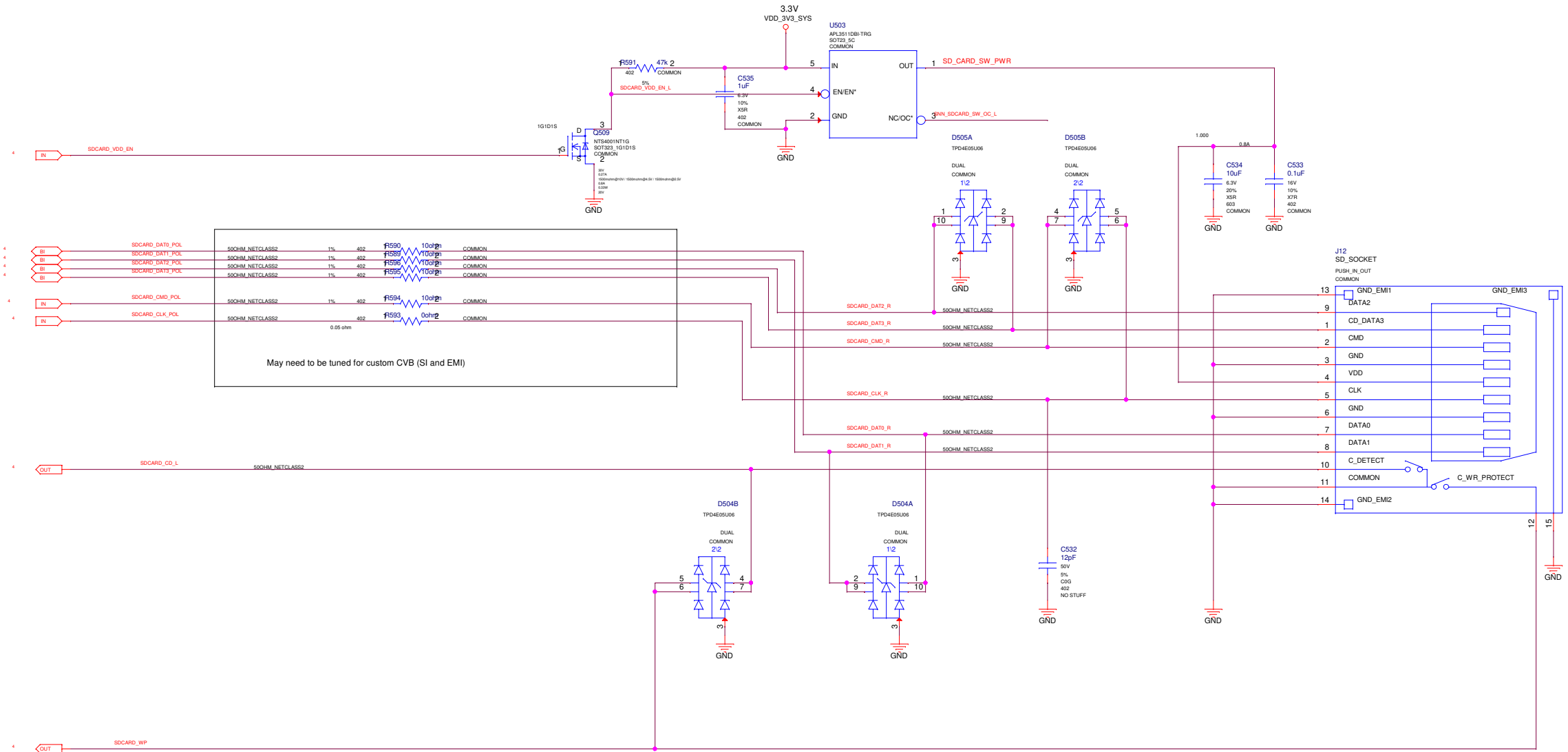
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# SD CARD SOCKET



SDCARD_DATA_POL	500HM_NETCLASS2	1%	402	R590	100Ω	COMMON
SDCARD_DATA1_POL	500HM_NETCLASS2	1%	402	R591	100Ω	COMMON
SDCARD_DATA2_POL	500HM_NETCLASS2	1%	402	R592	100Ω	COMMON
SDCARD_DATA3_POL	500HM_NETCLASS2	1%	402	R593	100Ω	COMMON
SDCARD_CMD_POL	500HM_NETCLASS2	1%	402	R594	100Ω	COMMON
SDCARD_CLK_POL	500HM_NETCLASS2	1%	402	R595	100Ω	COMMON
					0.05 ohm	

May need to be tuned for custom CVB (SI and EMI)

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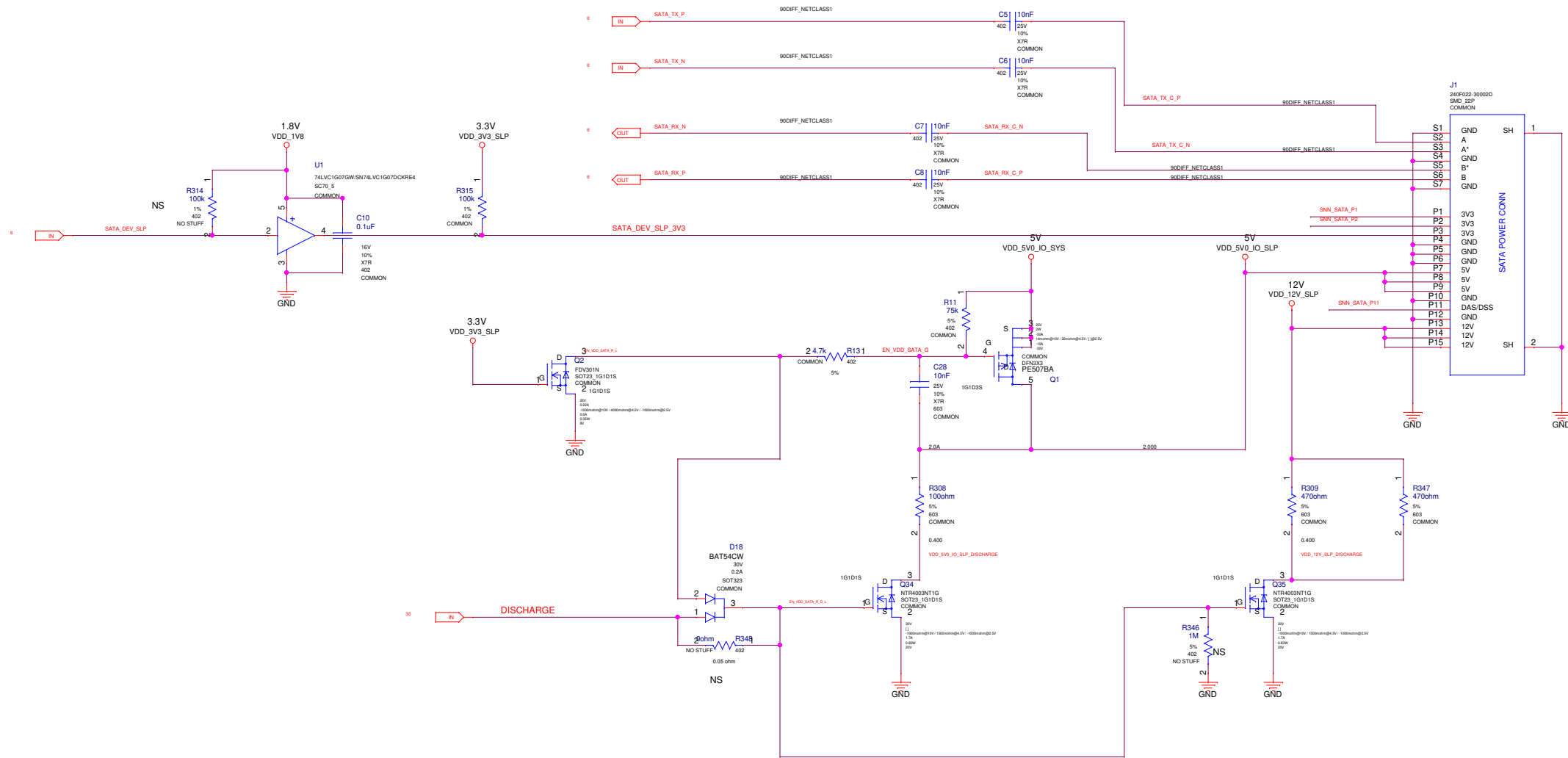
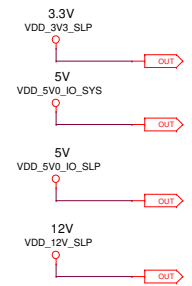
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# SATA Connector



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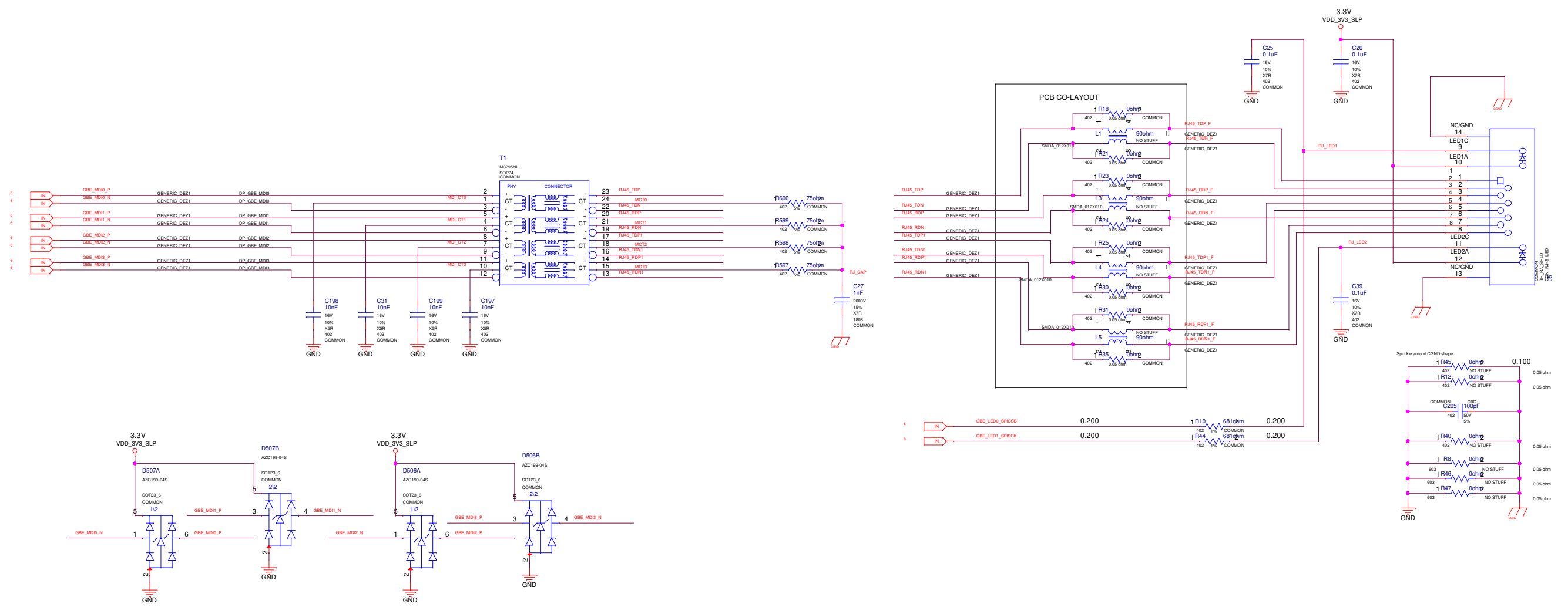


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# Gigabit Ethernet



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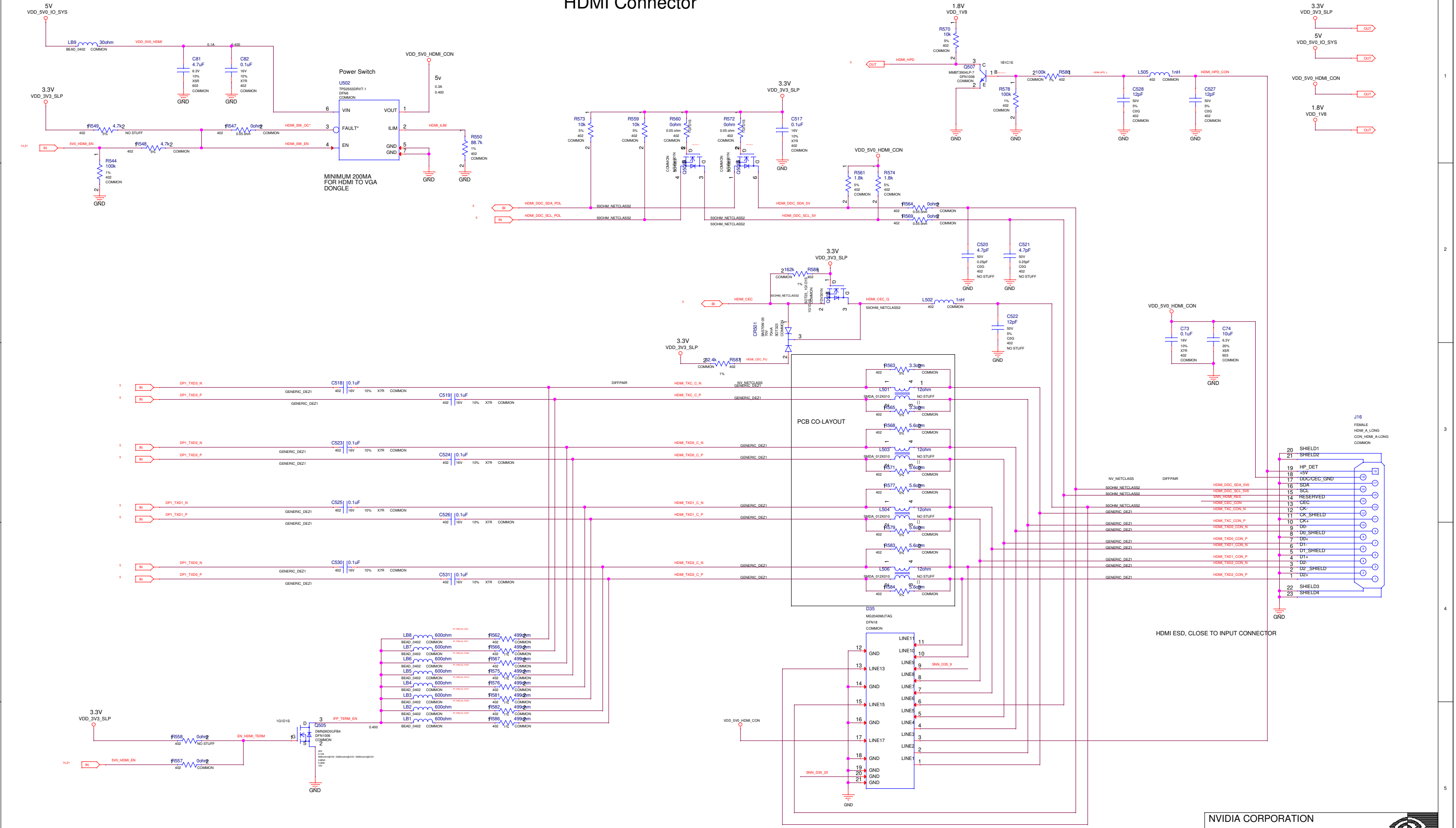
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# HDMI Connector



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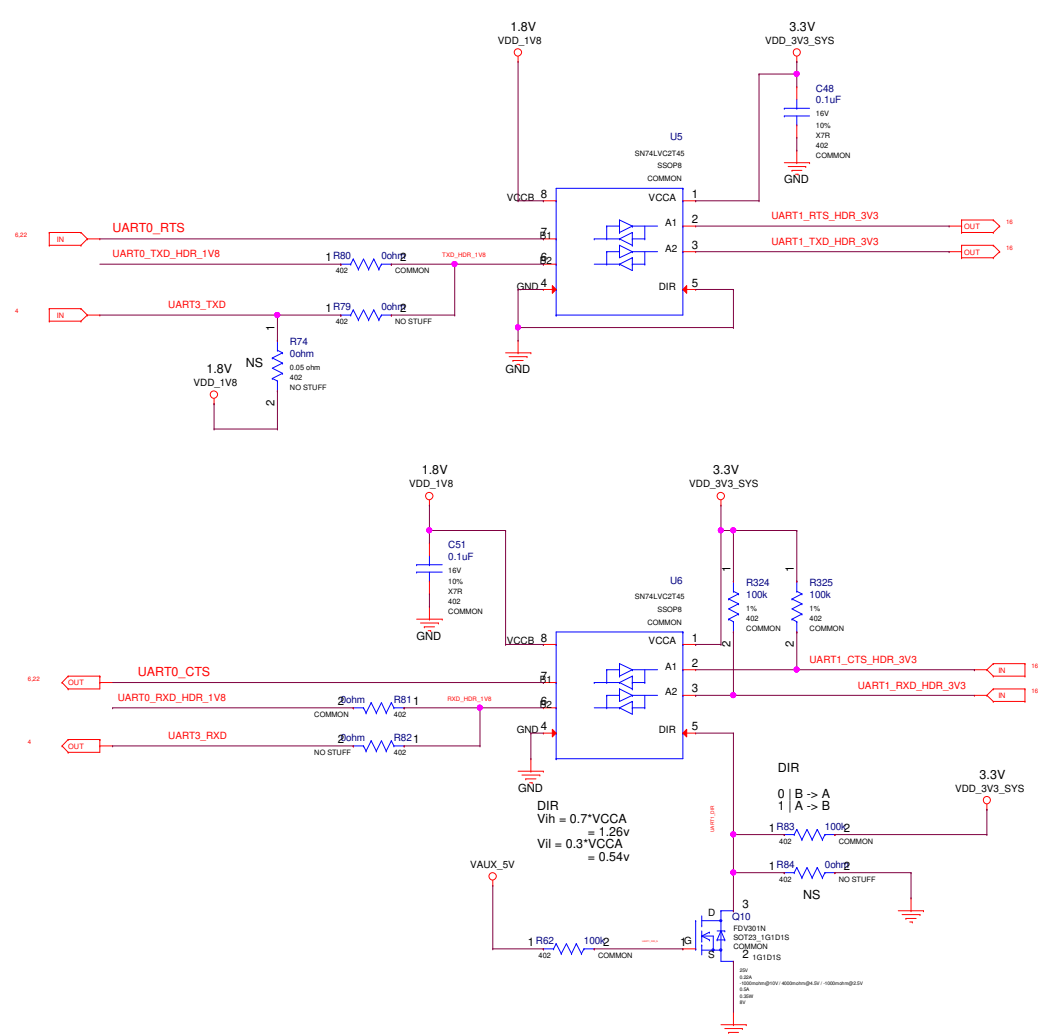
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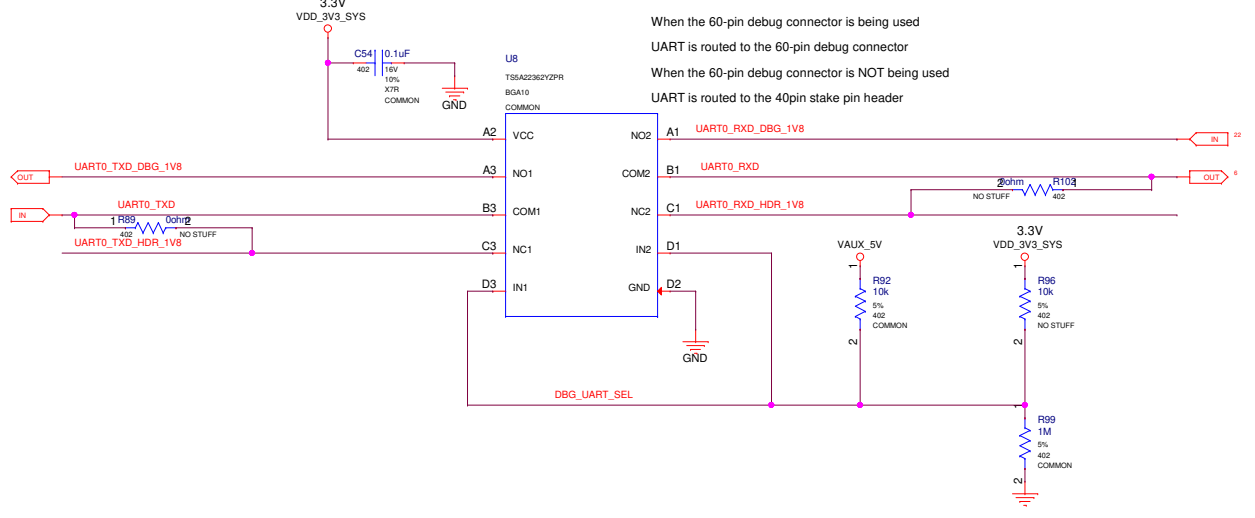
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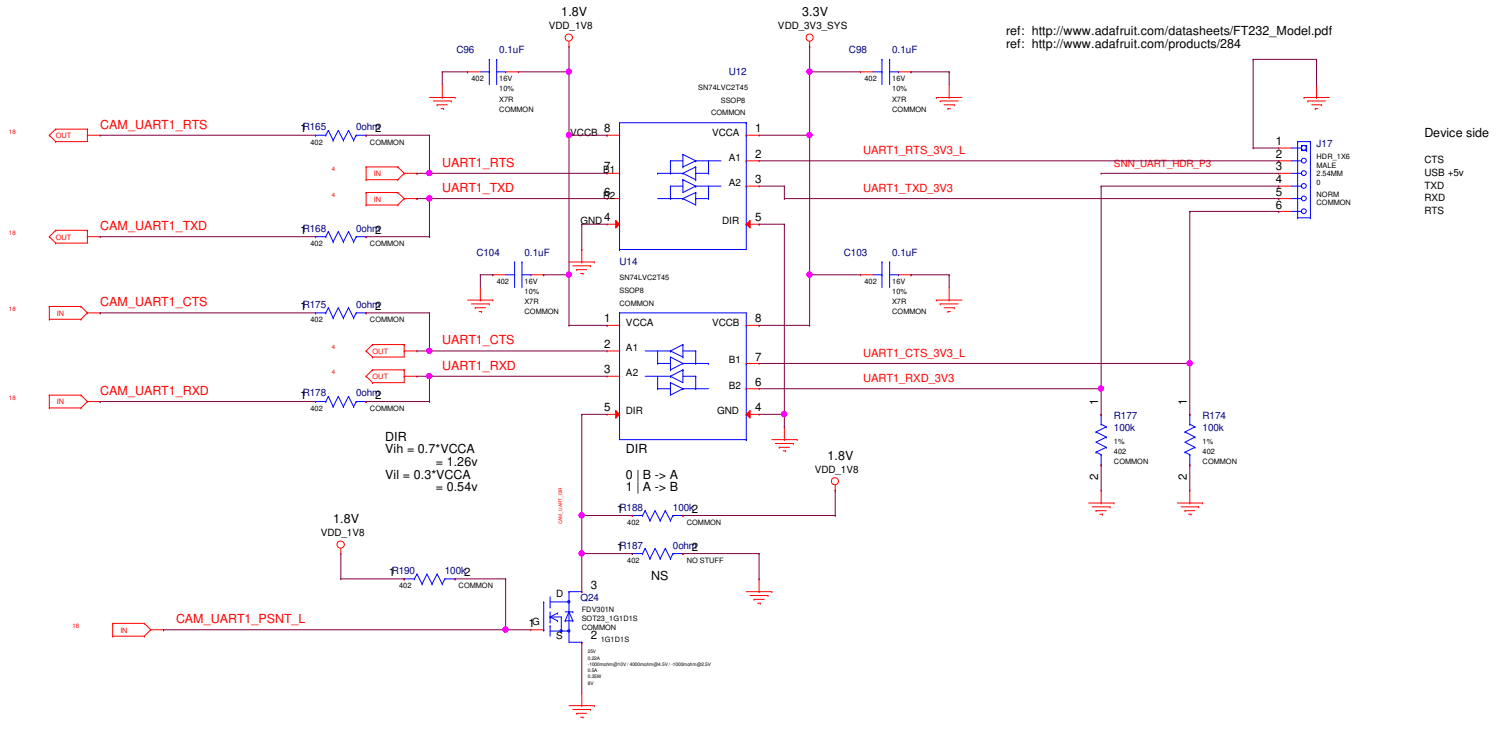


### UART MUX

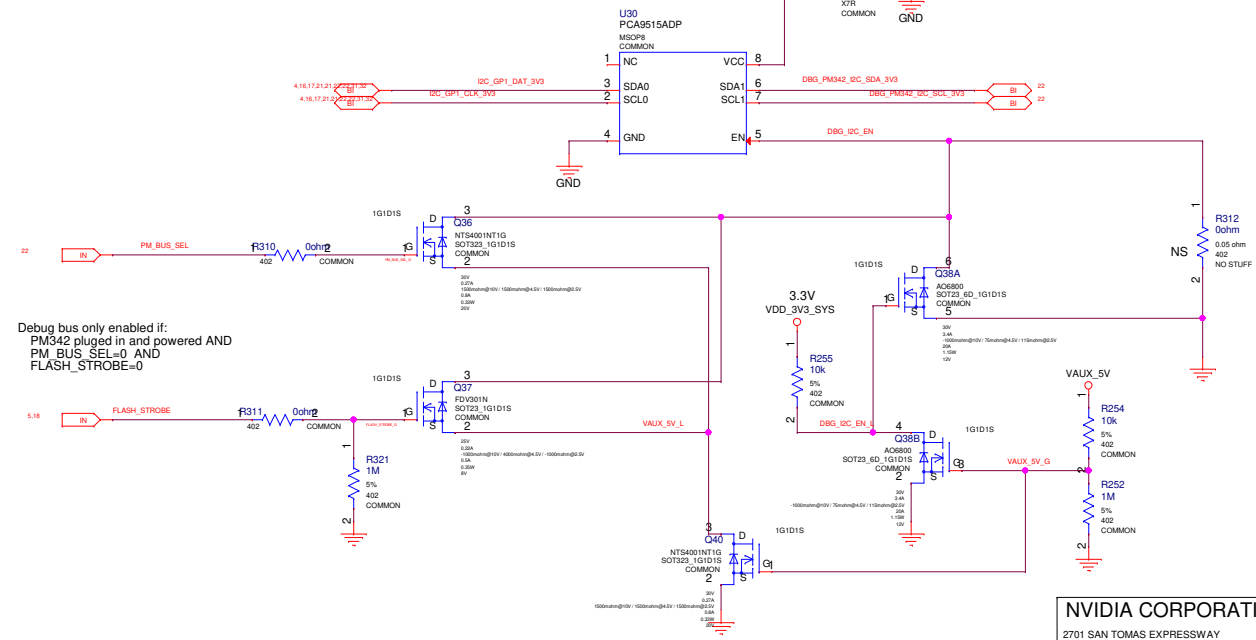
When the 60-pin debug connector is being used  
 UART is routed to the 60-pin debug connector  
 When the 60-pin debug connector is NOT being used  
 UART is routed to the 40pin stake pin header



### SERIAL PORT




### DBG I2C GATE



Debug bus only enabled if:  
 PM342 plugged in and powered AND  
 PM\_BUS\_SEL=0 AND  
 FLASH\_STROBE=0

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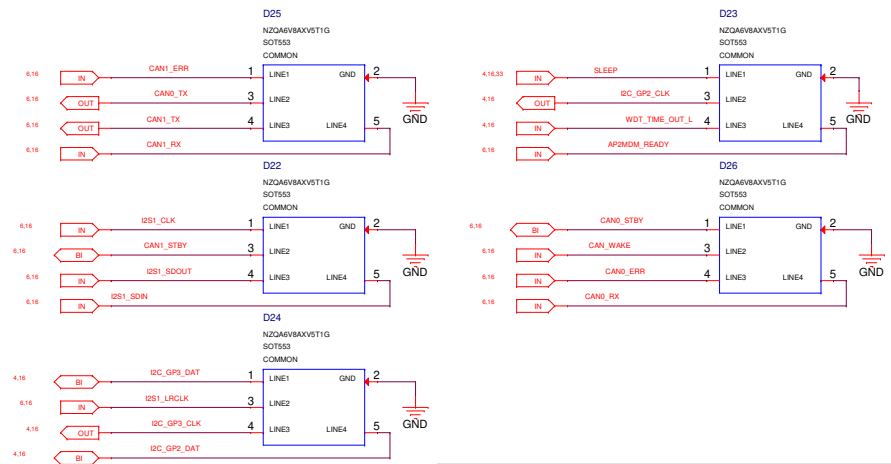
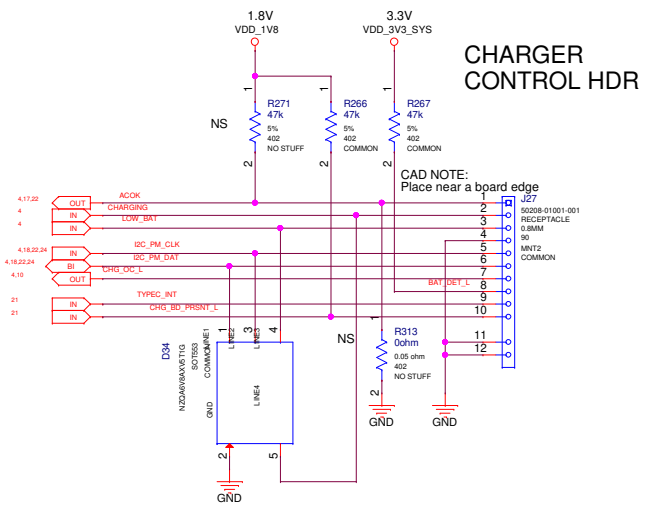
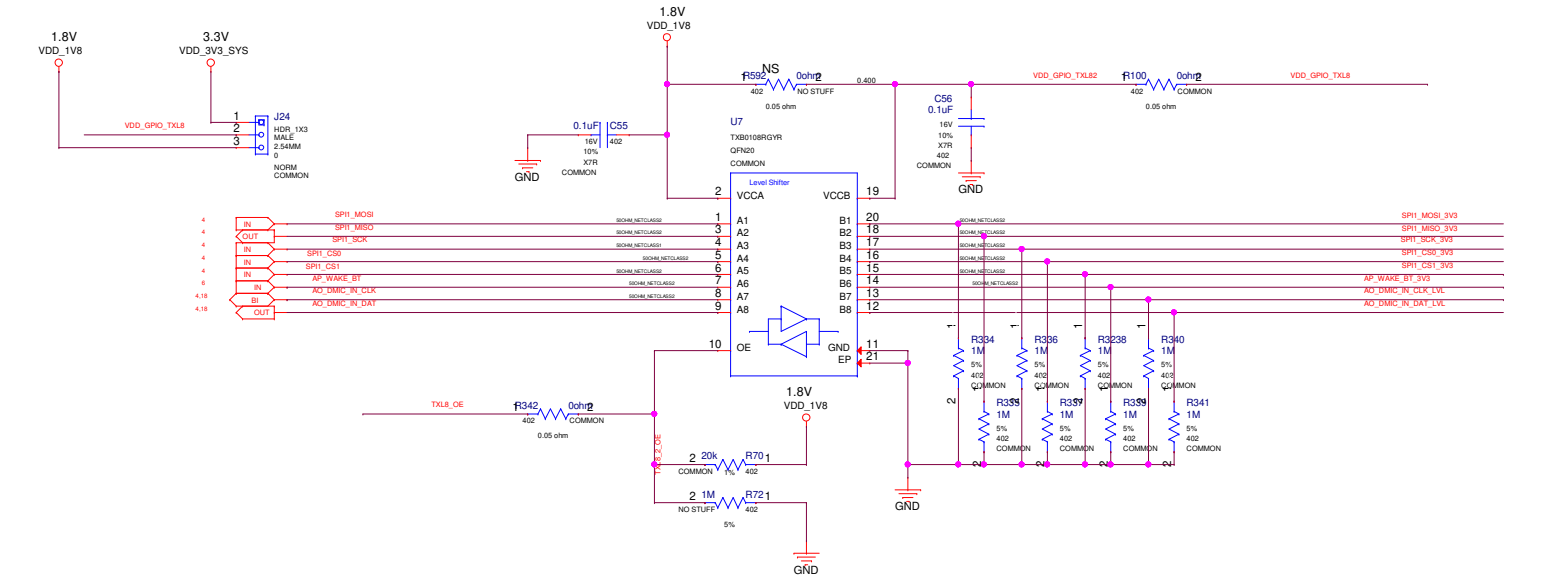
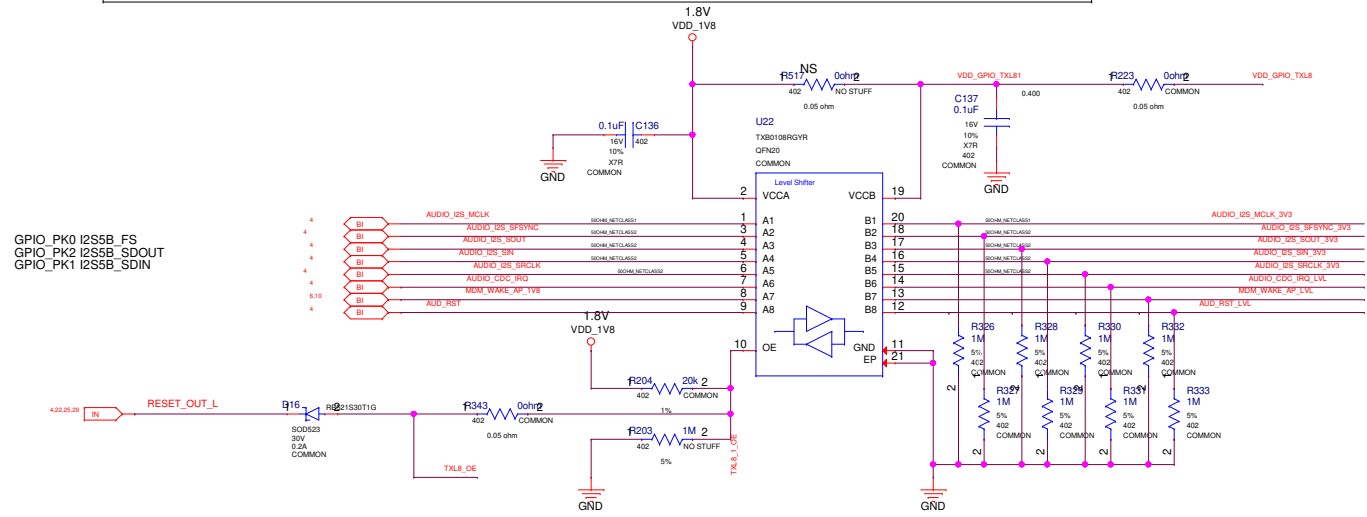
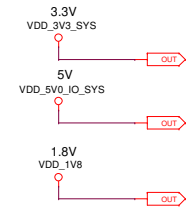
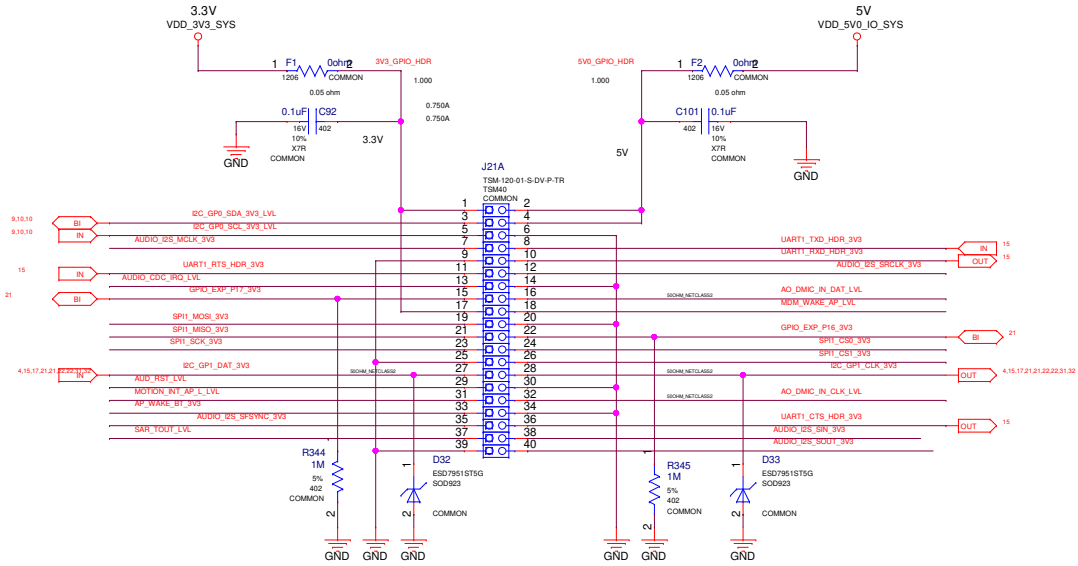
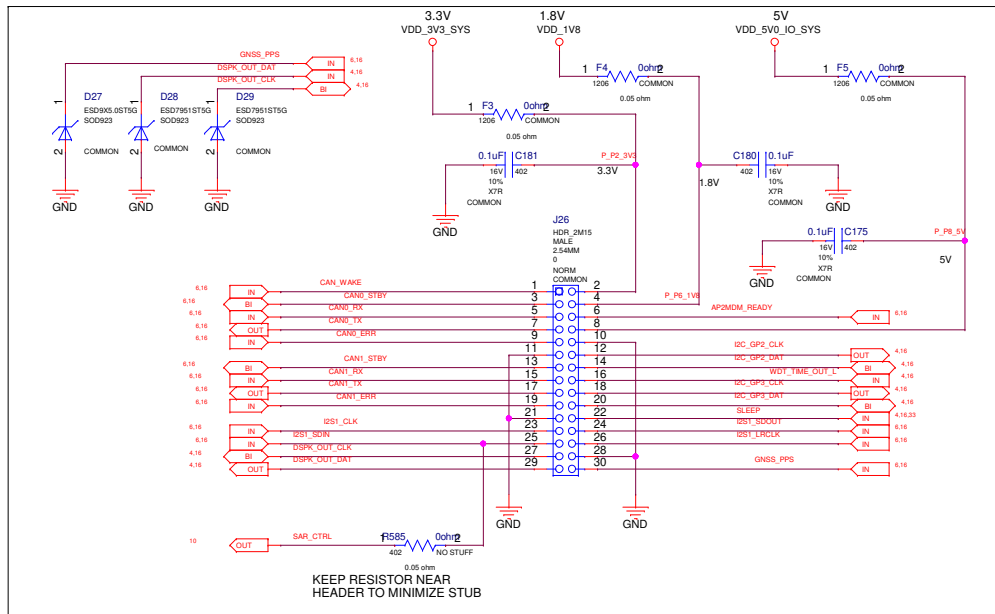
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Serial port and JTAG

# GPIO Expansion Headers



ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> IO Expansion Connector
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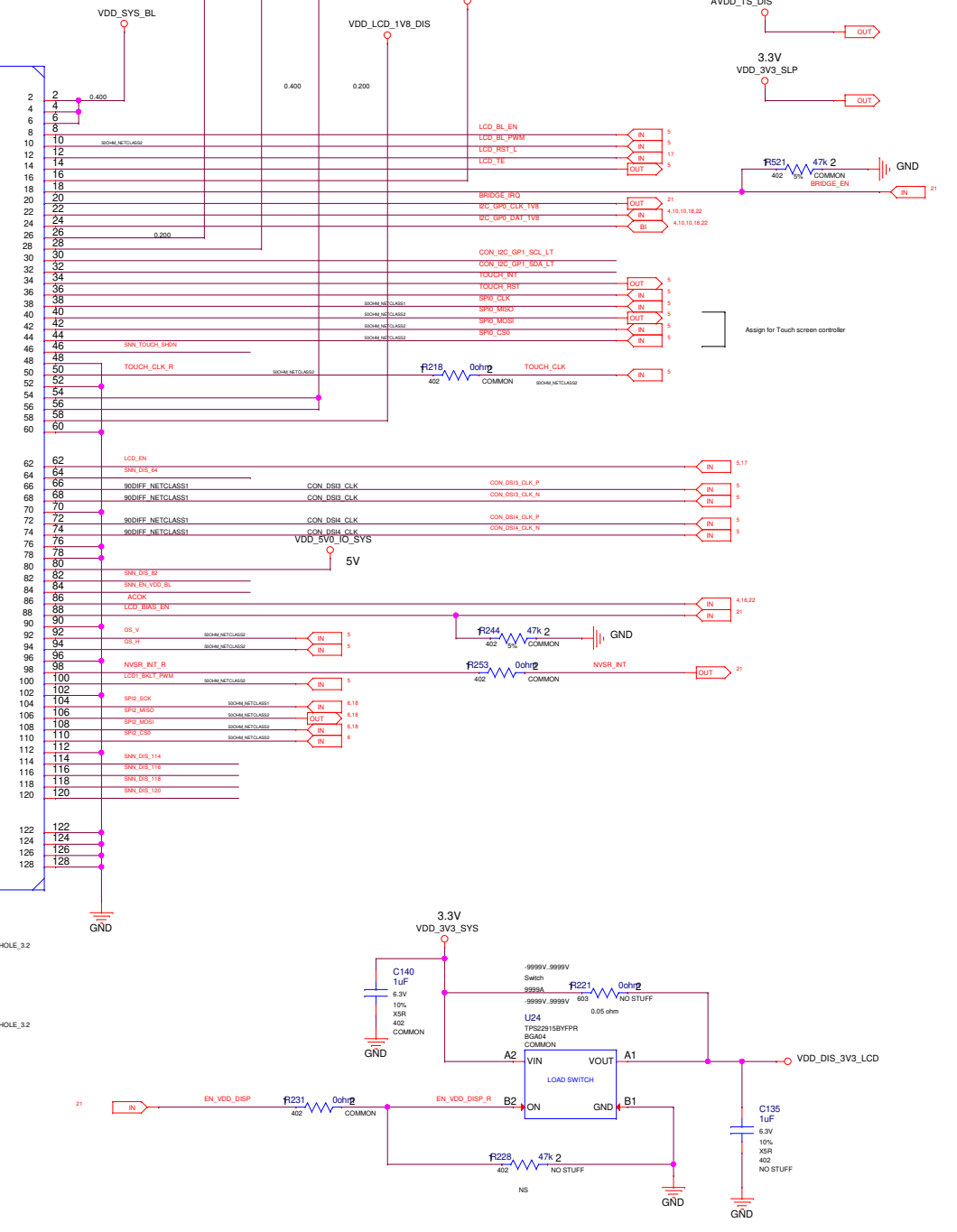
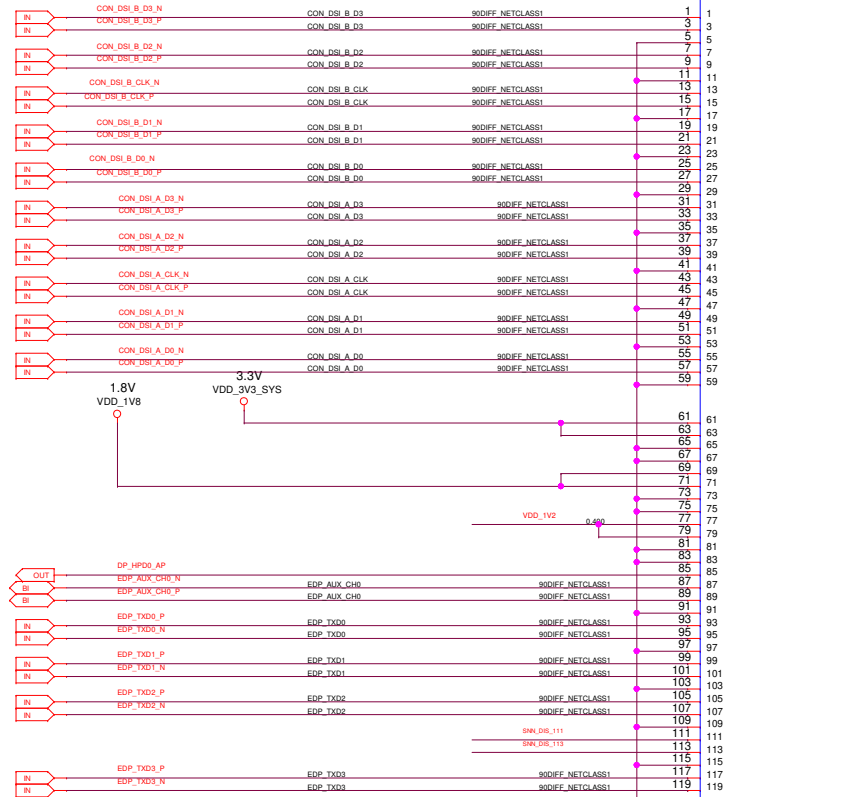
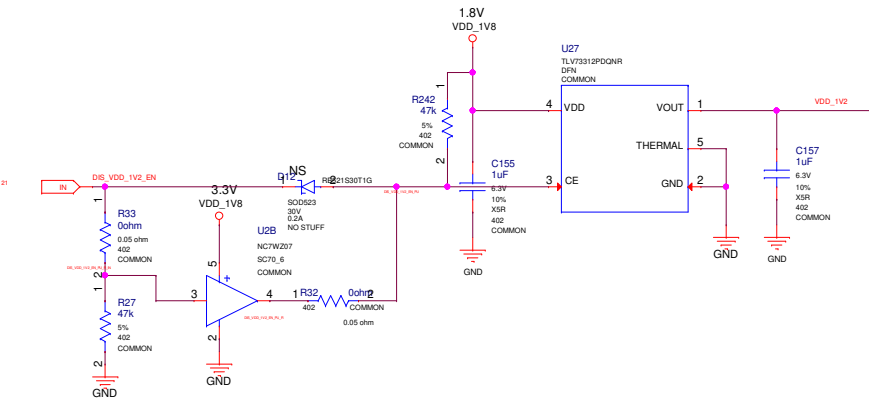
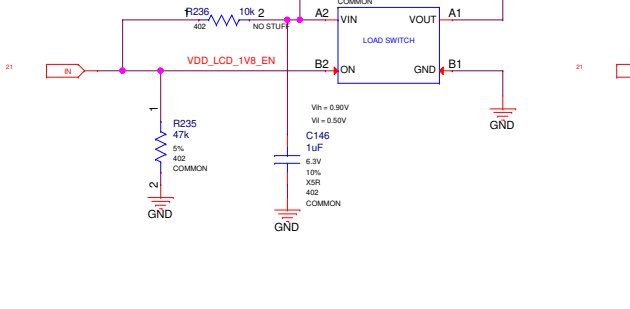
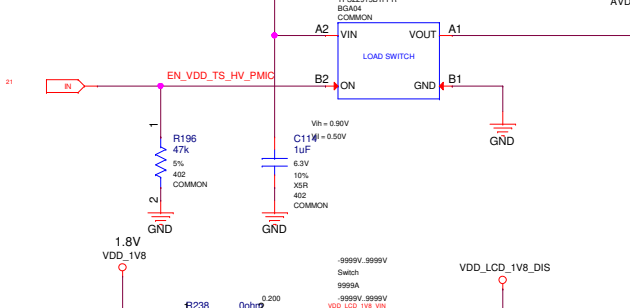
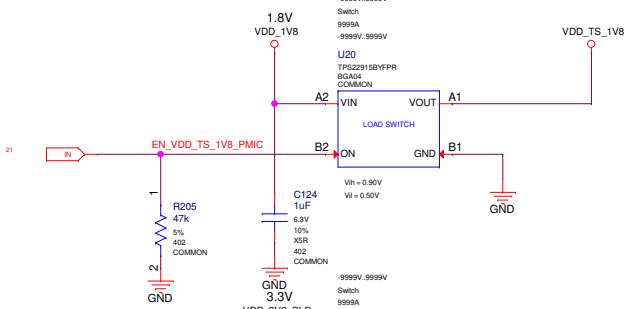
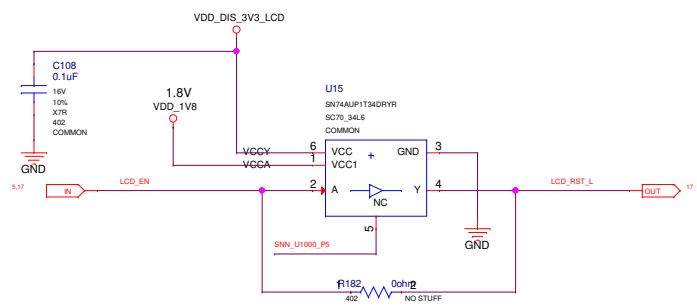
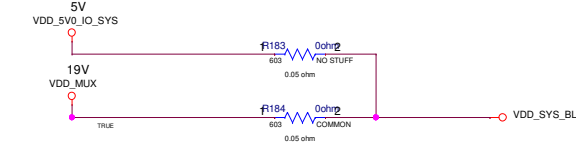
NV_PN	600-82597-BASE-900
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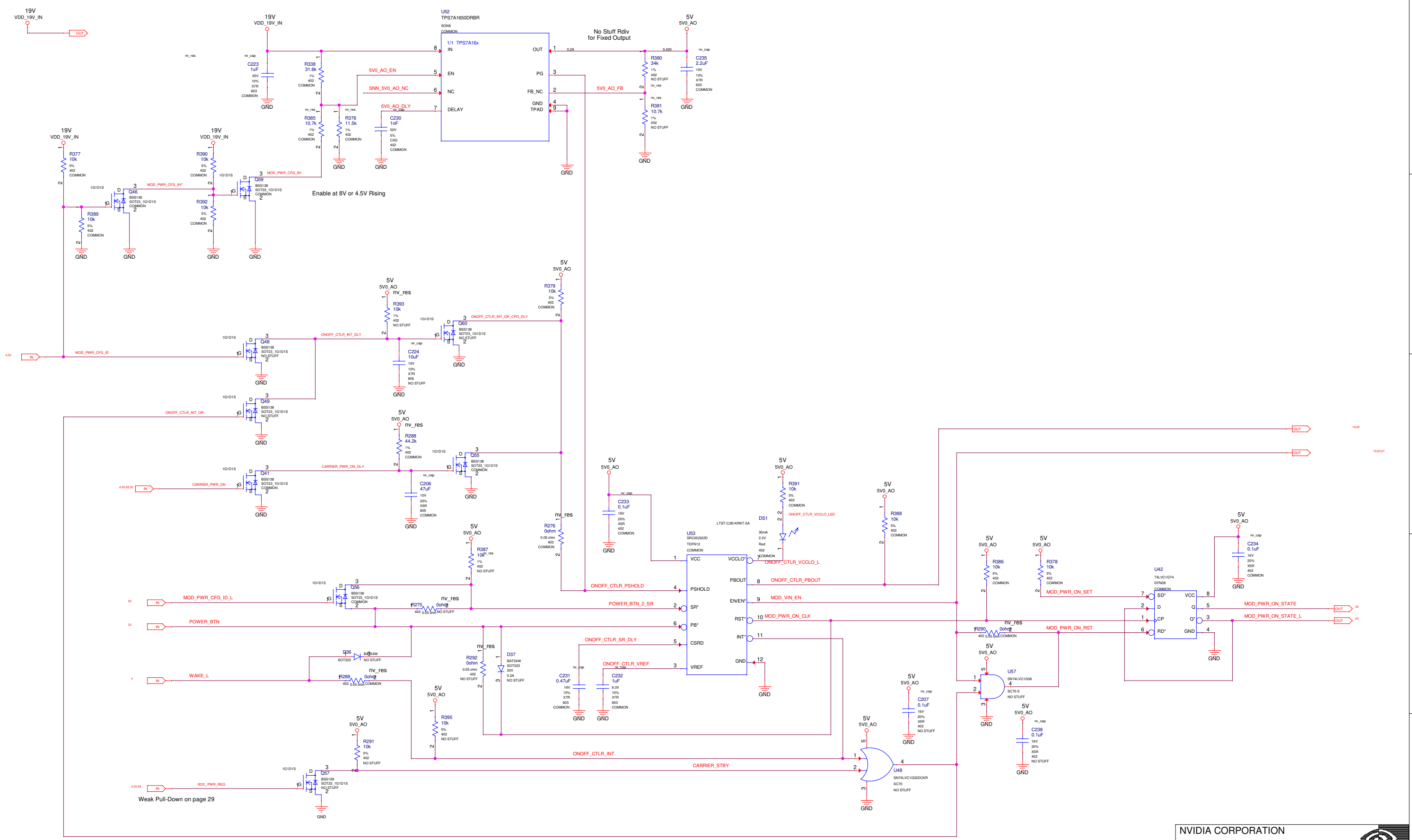


# DISPLAY CONNECTOR



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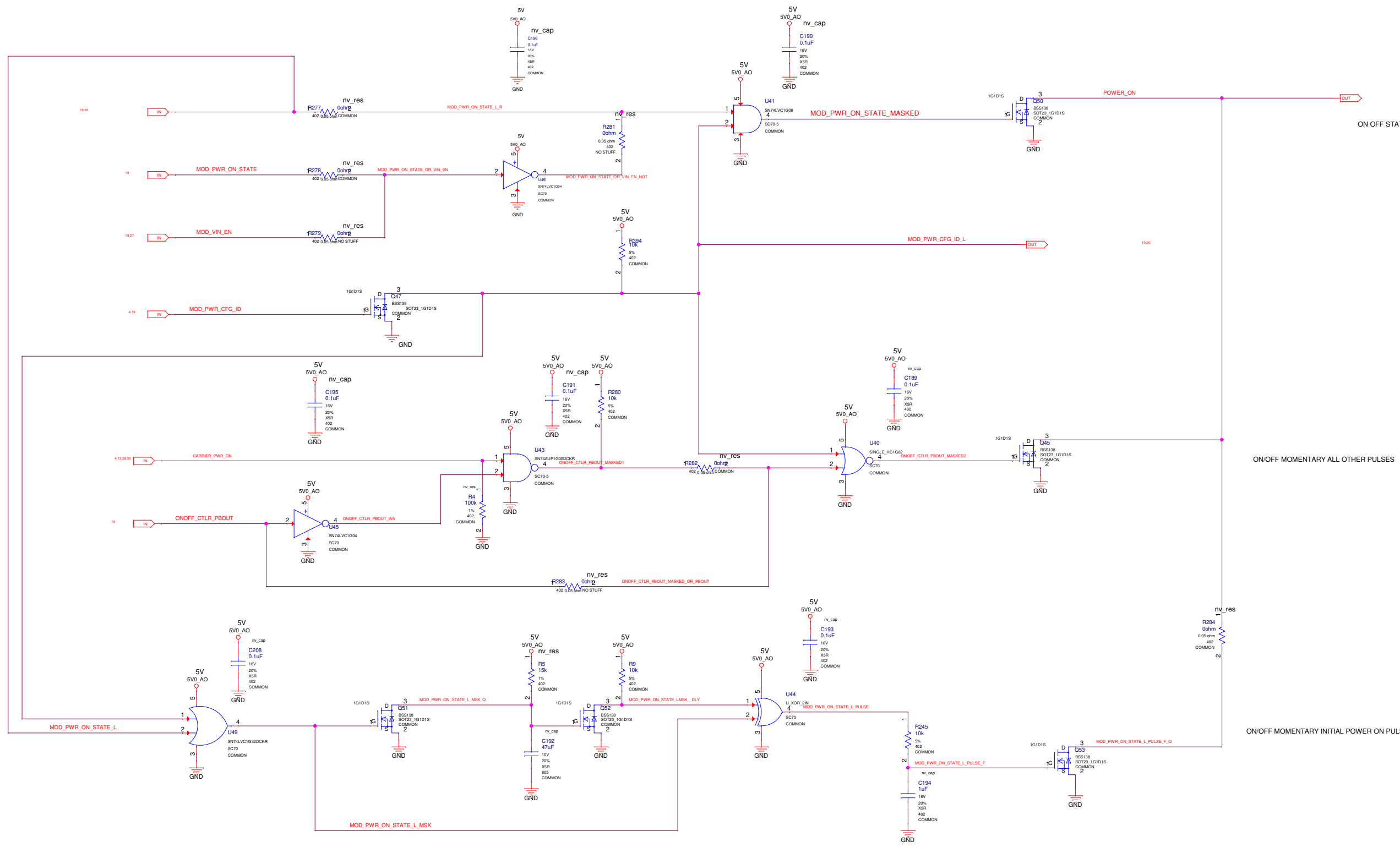
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	ON OFF CONTROLLER

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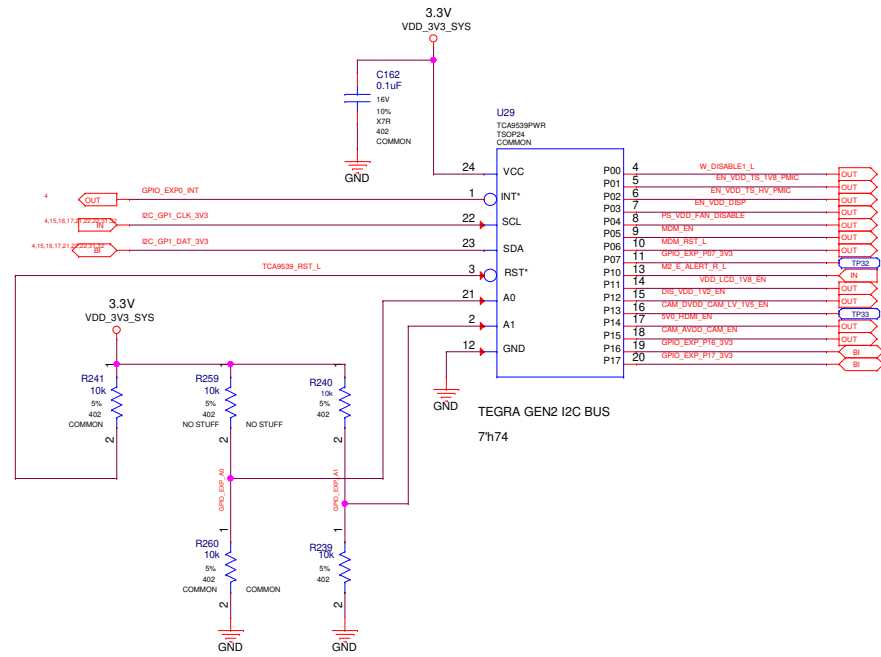
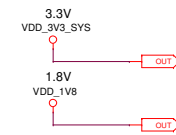
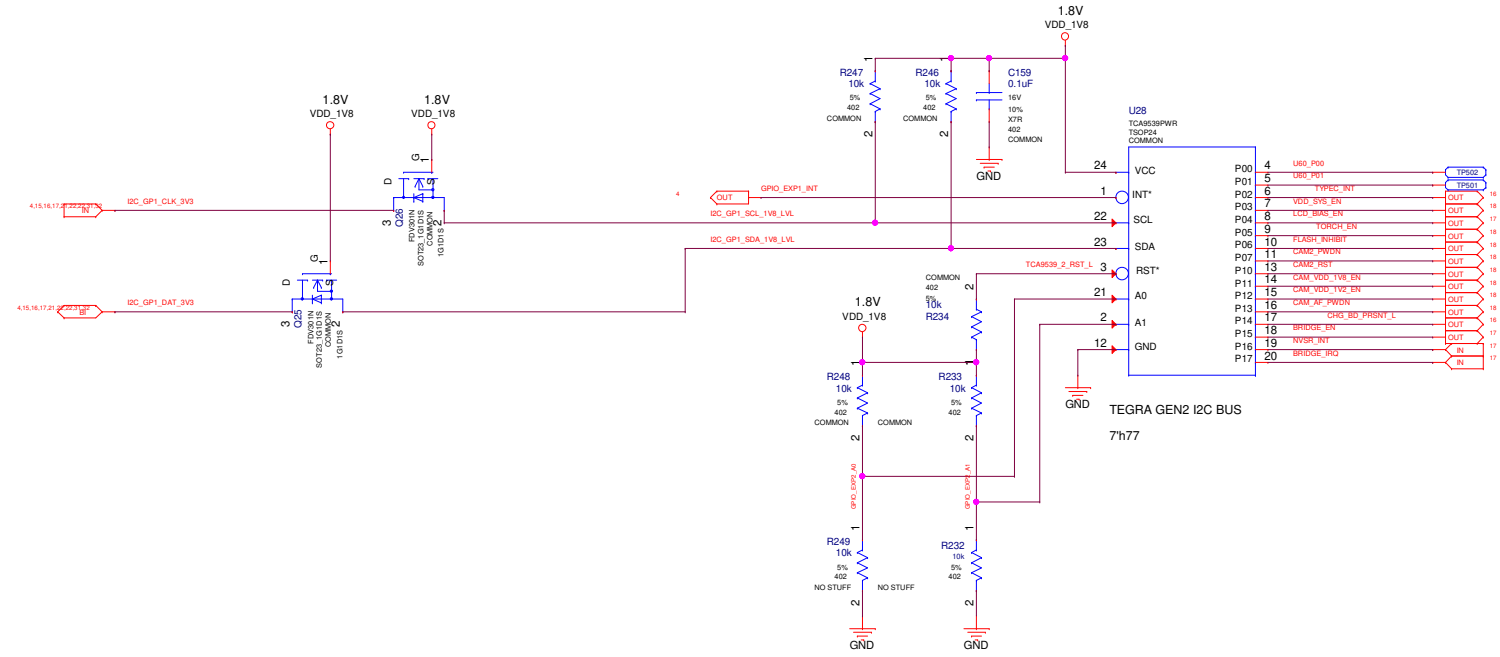


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NV_PN PCB REV BOM REV	<b>600-82597-BASE-900</b> P2597-C02 A	

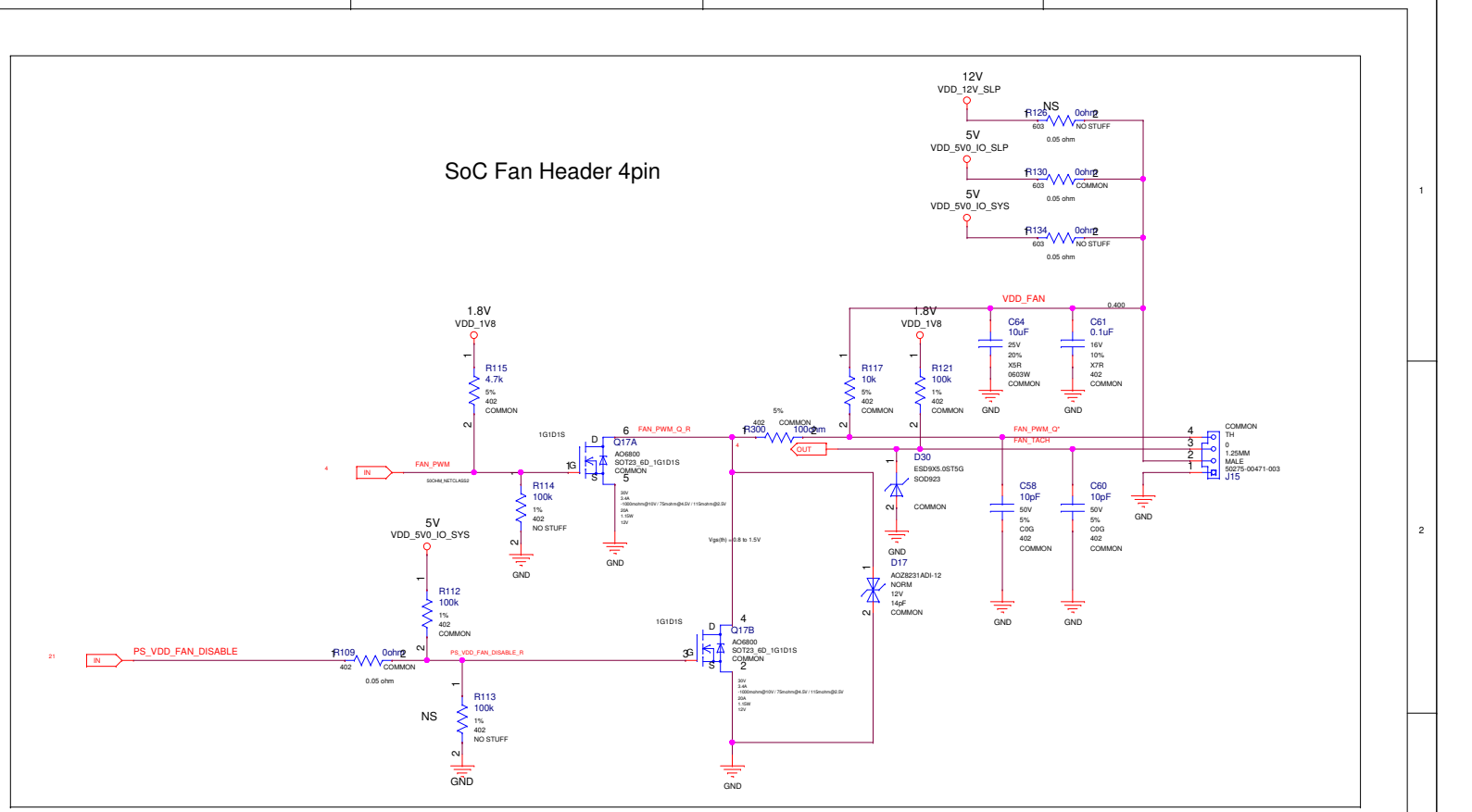
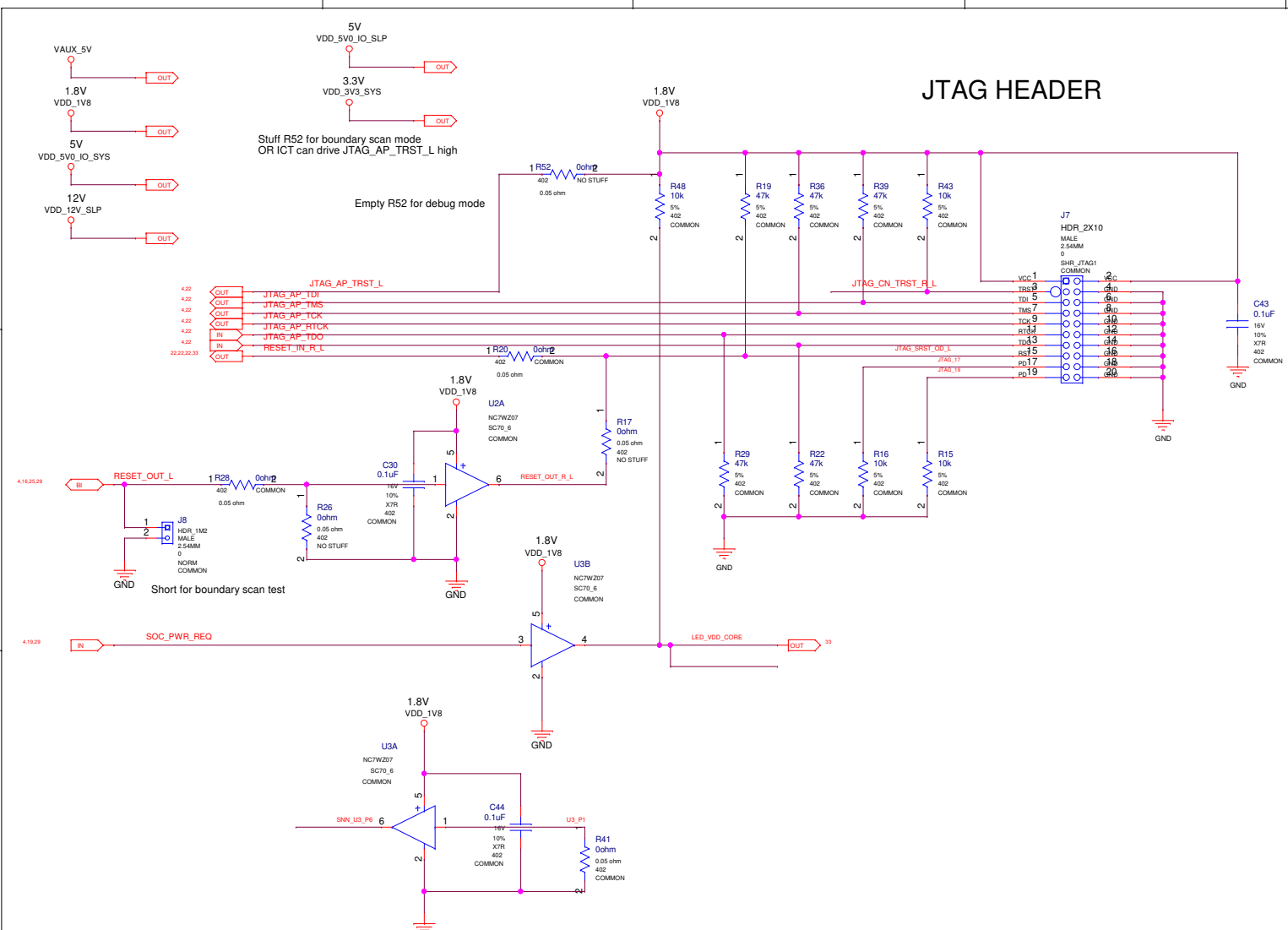
# GPIO EXPANDERS

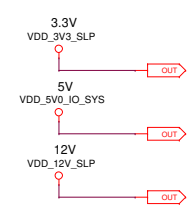
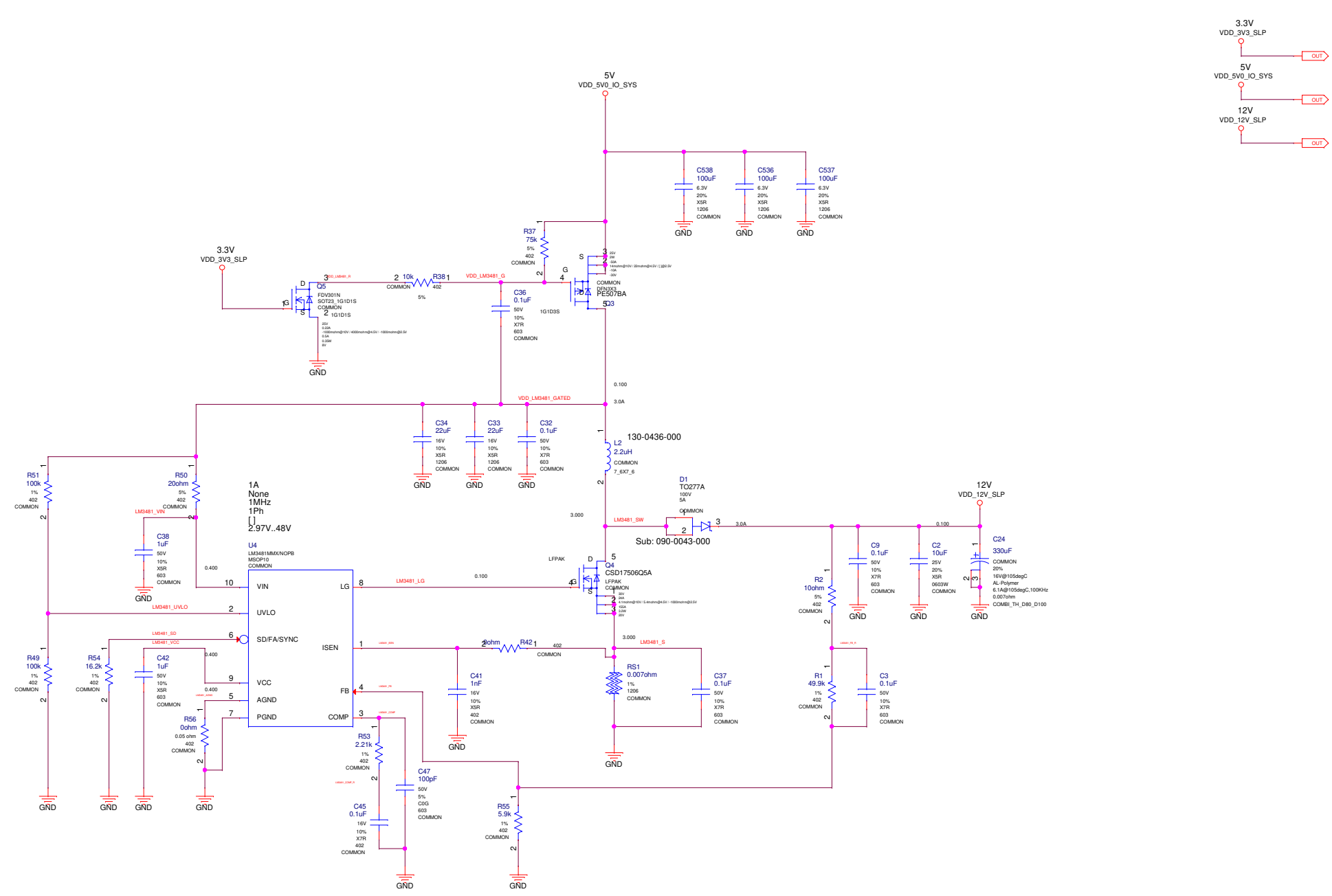



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPIO Expanders

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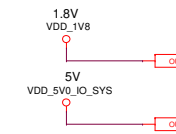
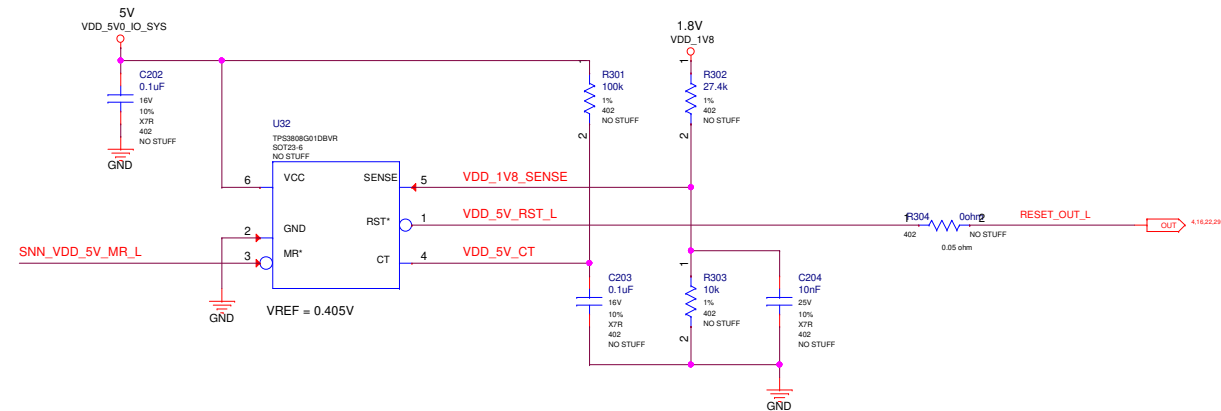
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NV_PN	600-82597-BASE-900	PAGE	23 OF 34
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	12V BOOST

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Supervisor

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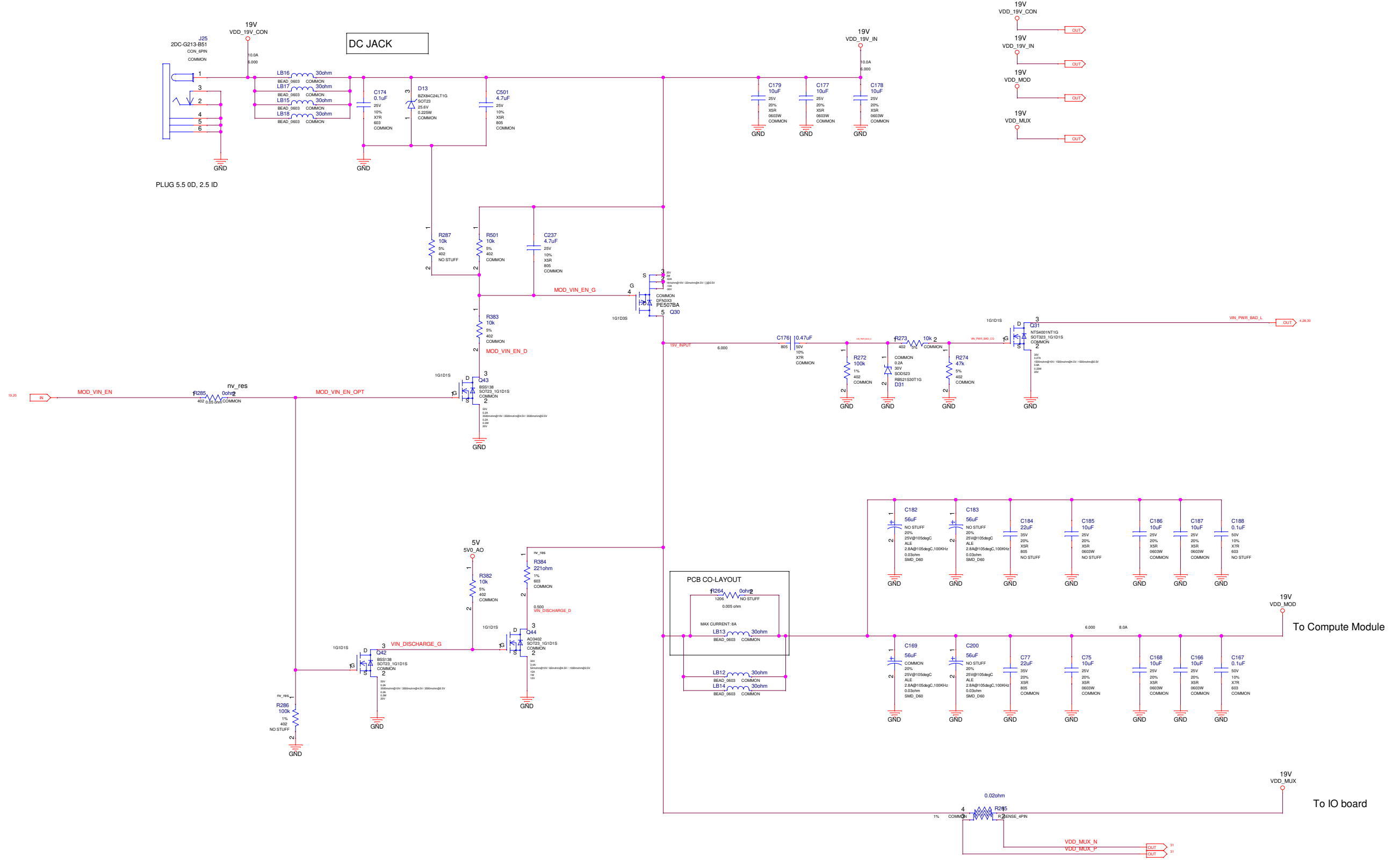
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A B C D E F G H

# 19V Jack



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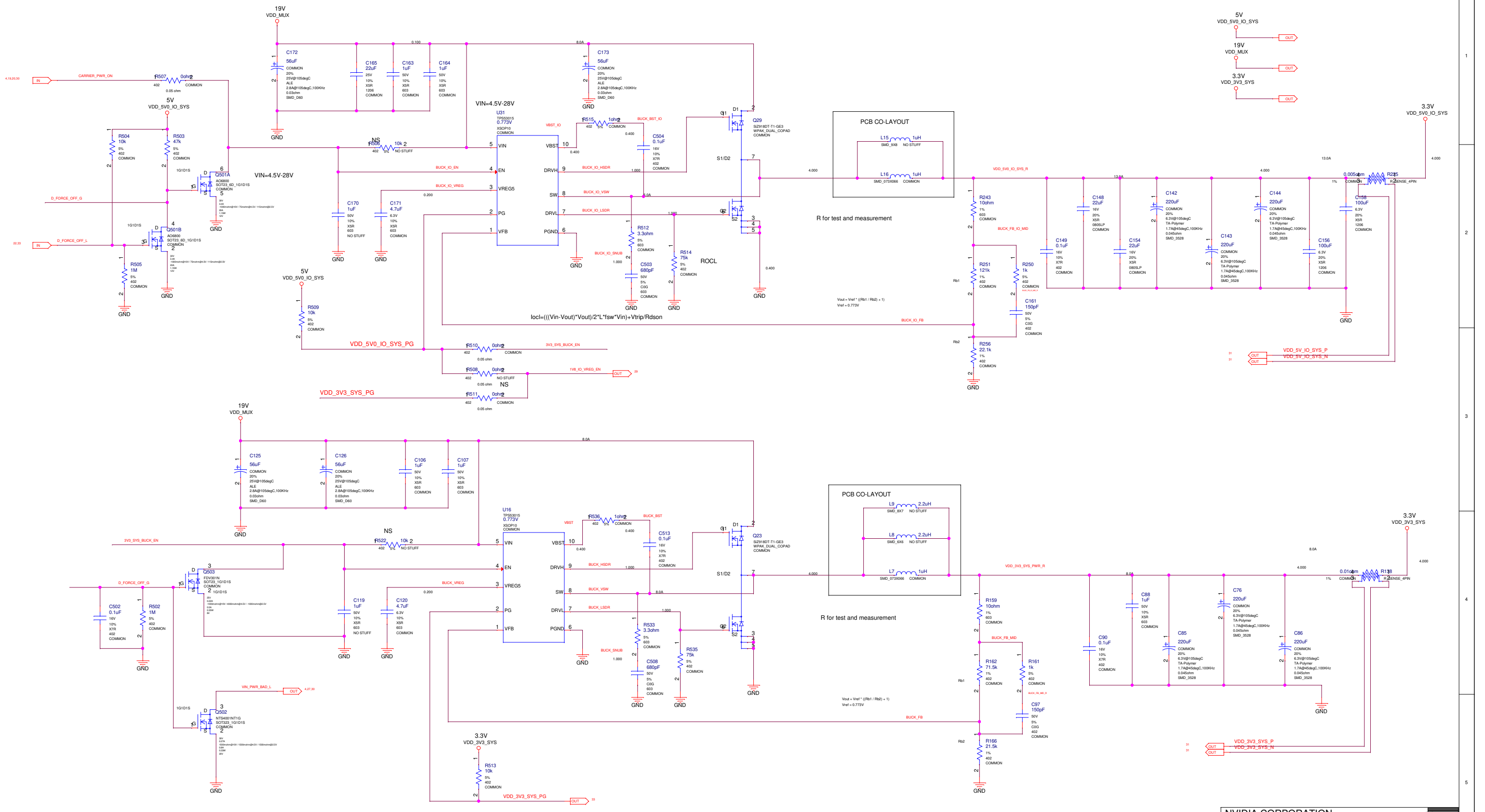
NV_PN	600-82597-BASE-900
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	DC Jack

# 5V & 3V3 SYS POWER SUPPLIES



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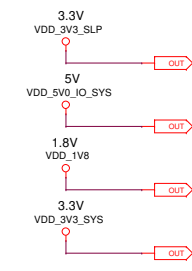
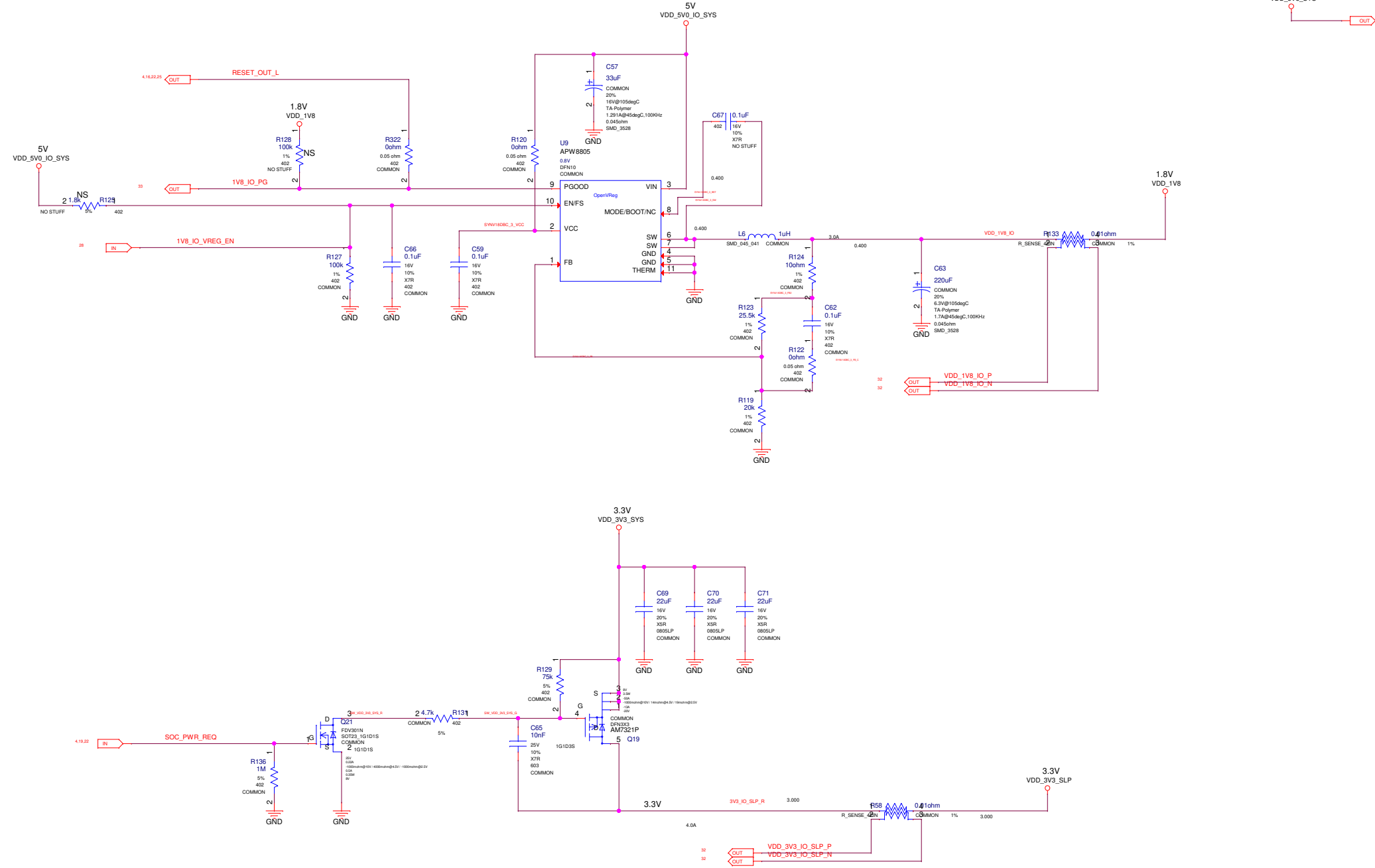
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# 1V8 POWER SUPPLY AND 3V3\_SYS

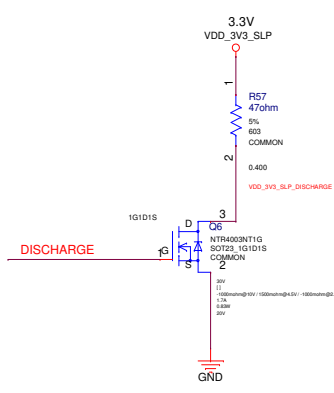
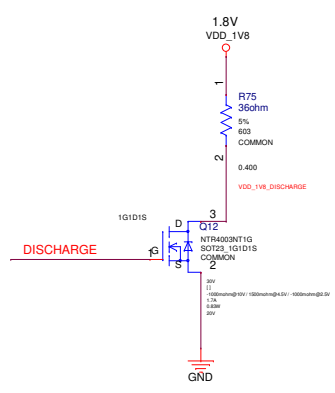
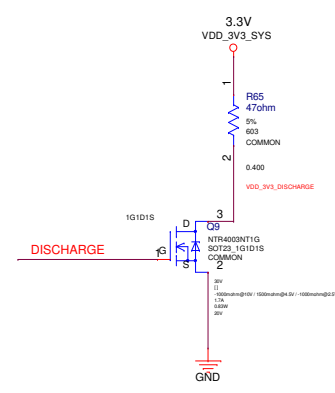
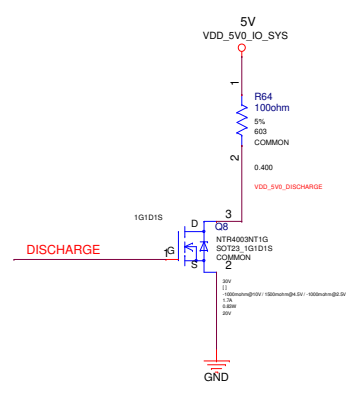
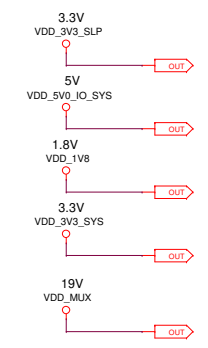
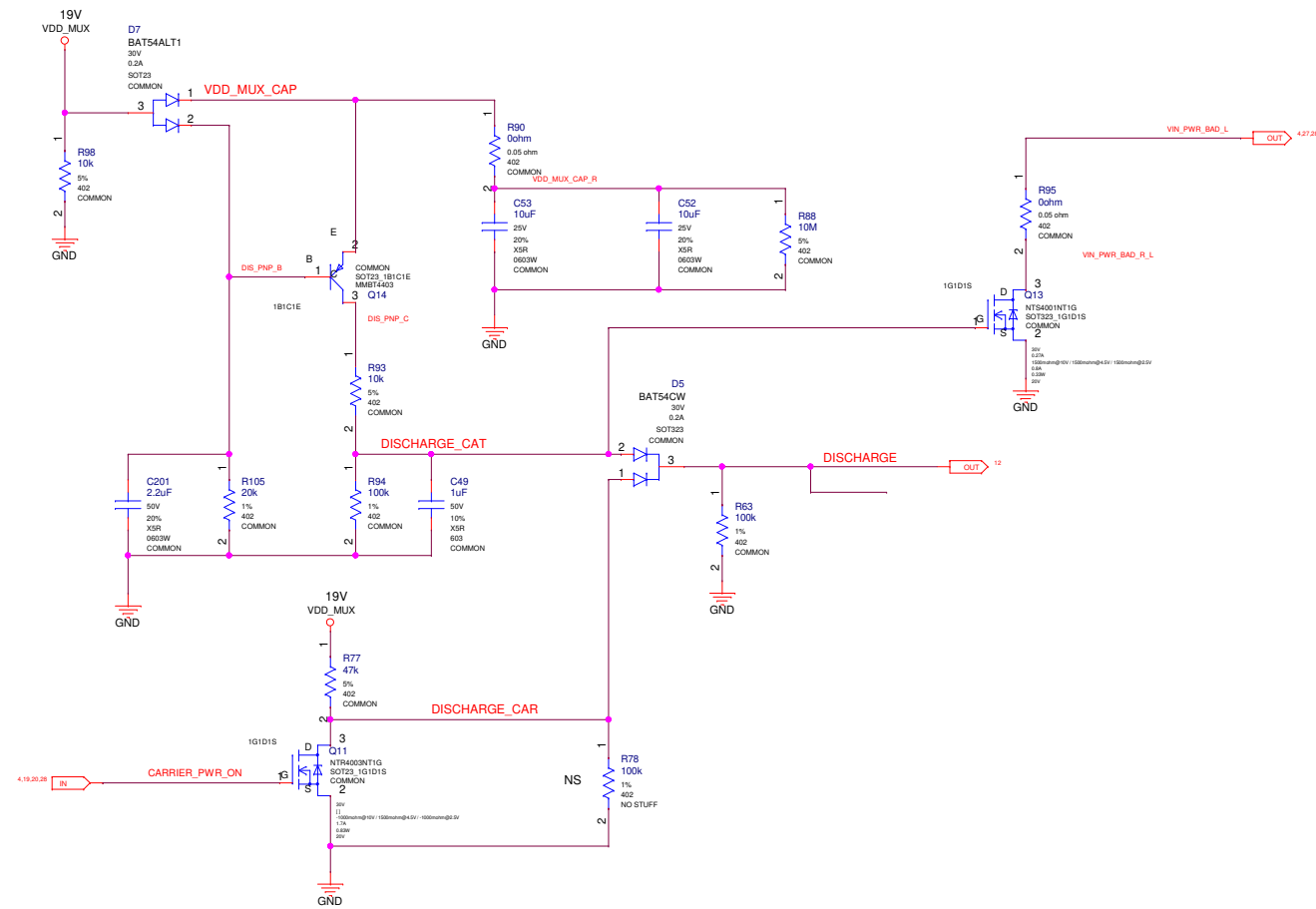


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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	3V3 SLP AND 1.8V Vregs


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# RAIL DISCHARGE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Rail Discharge

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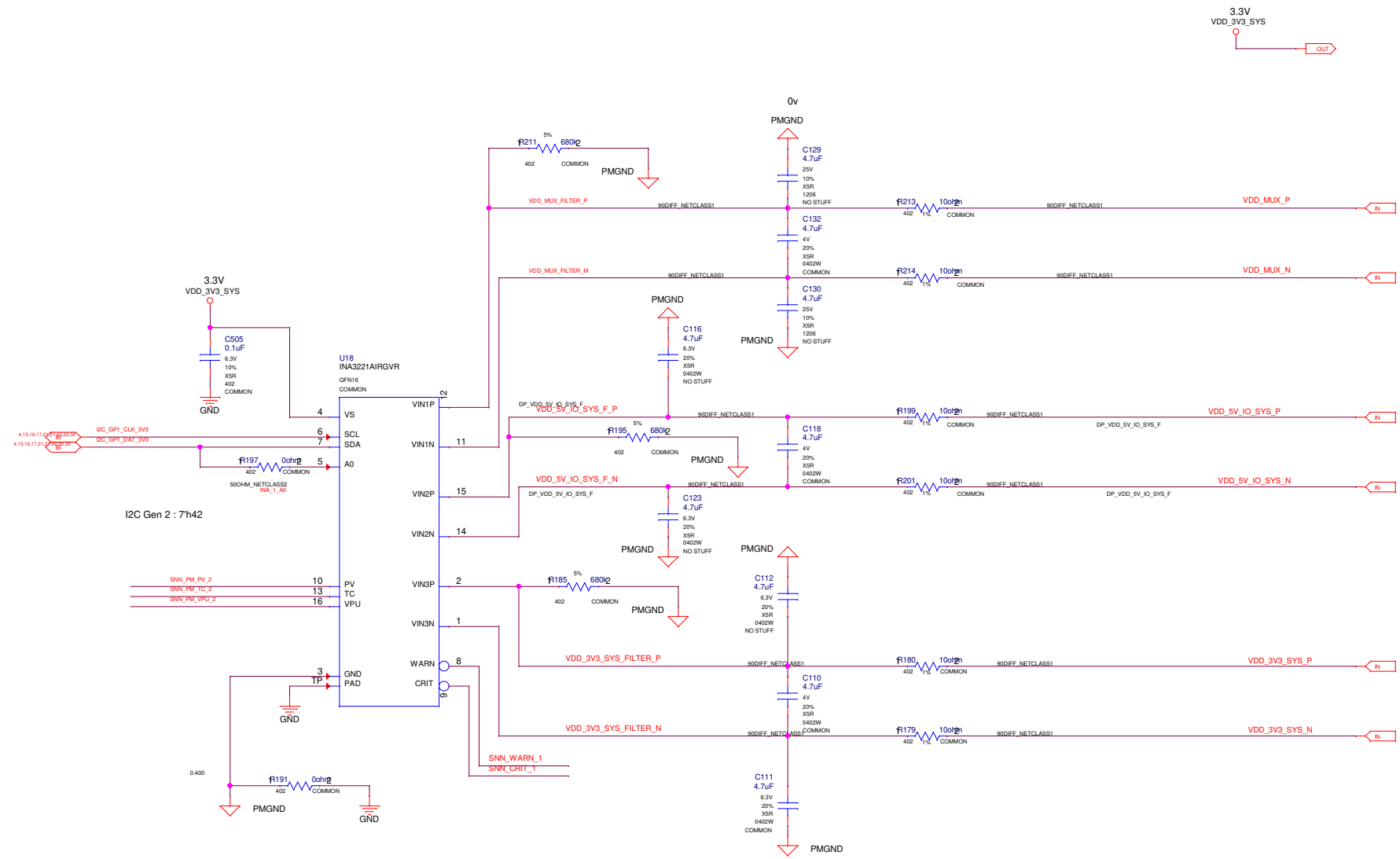


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# POWER MONITORS I



DC JACK to IO board

5V SYSTEM

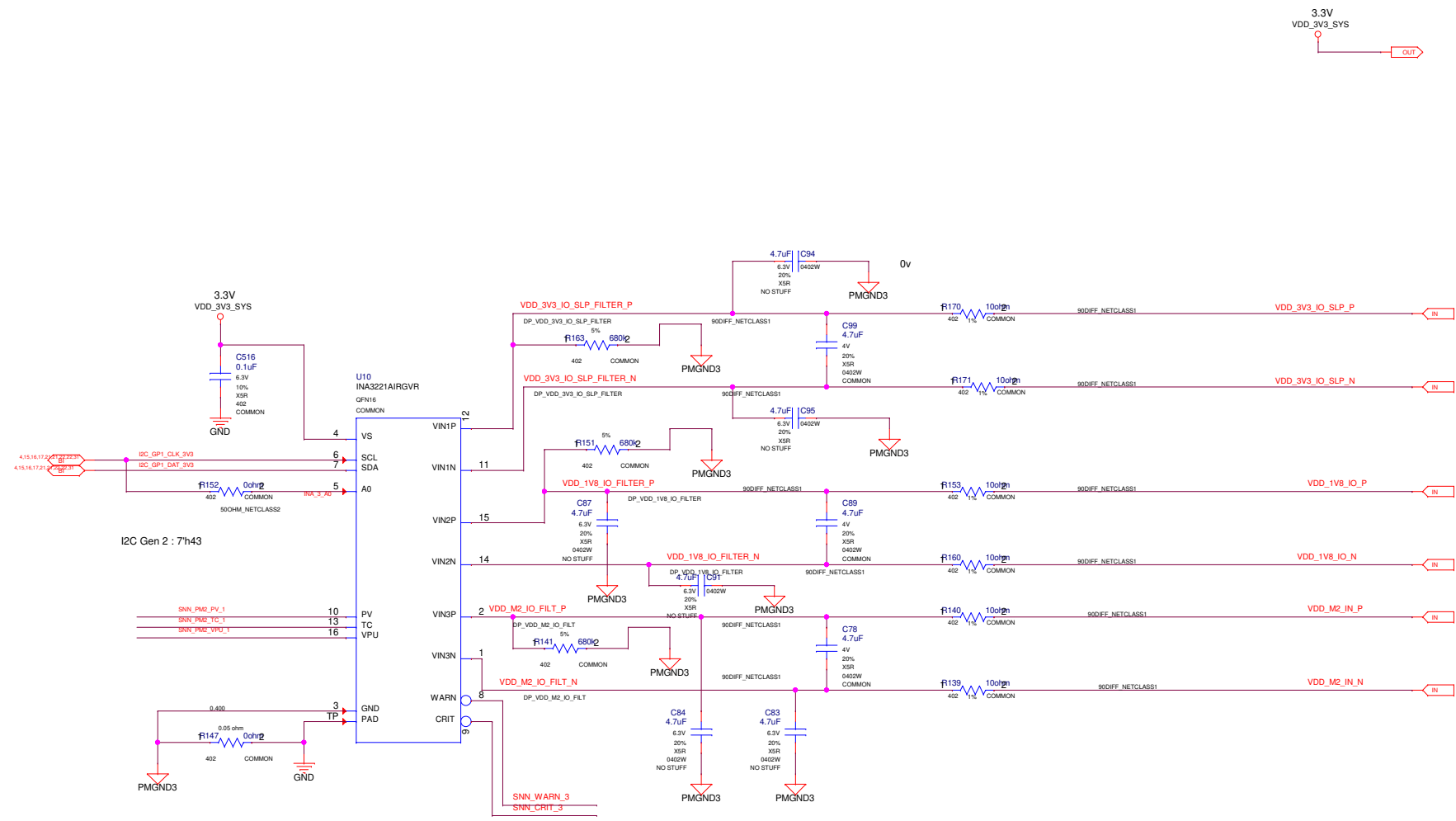
3V3 SYSTEM

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Power Monitor I


# POWER MONITORS II



3V3 RUN RAIL

1.8V SYSTEM

M.2 3.3V

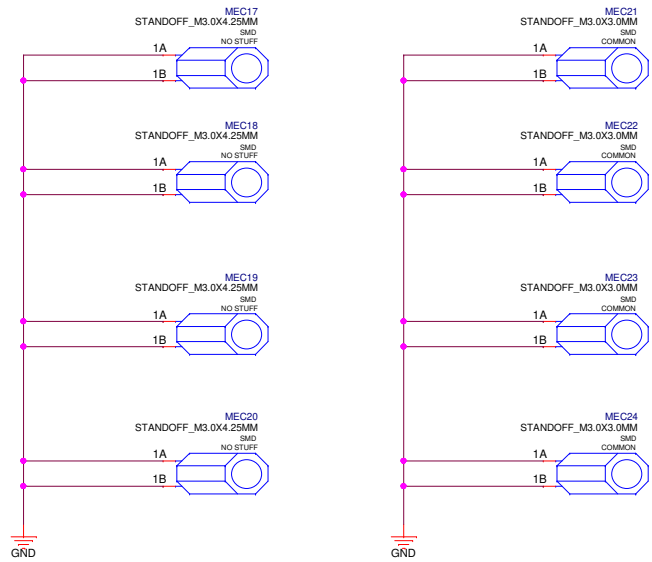
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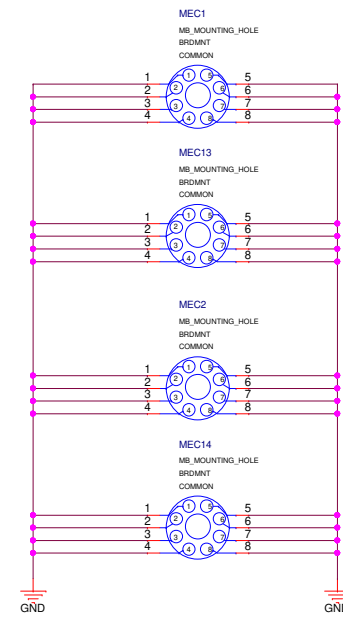
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PAGE DETAIL	Power Monitor II



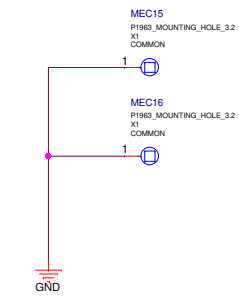
MODULE MOUNTING STANDOFFS  
Top Side Botselom Side



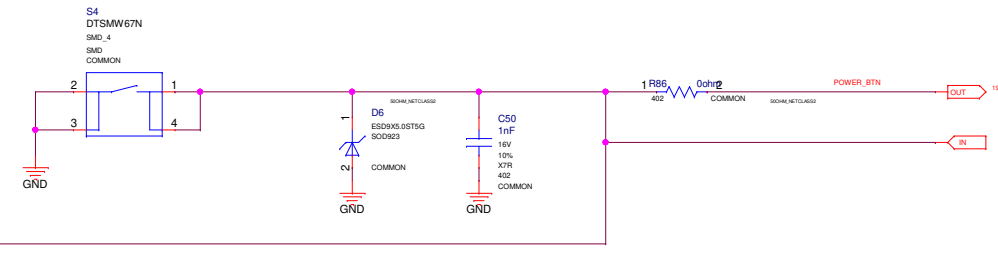
FOUR CORNER  
miniITX MOUNTING HOLES



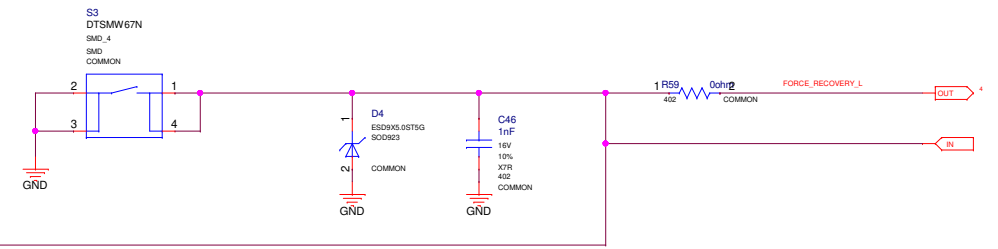
Antenna bracket  
mount



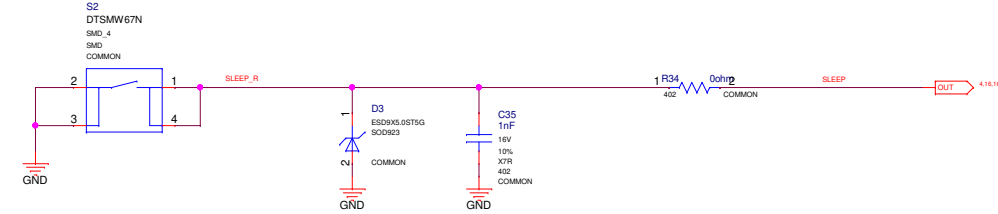
POWER



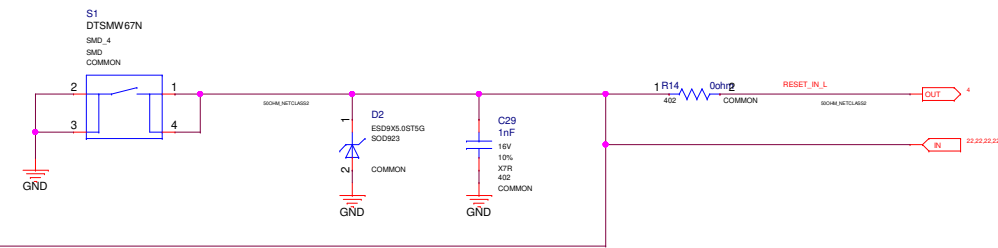
RECOVERY



VOL DOWN



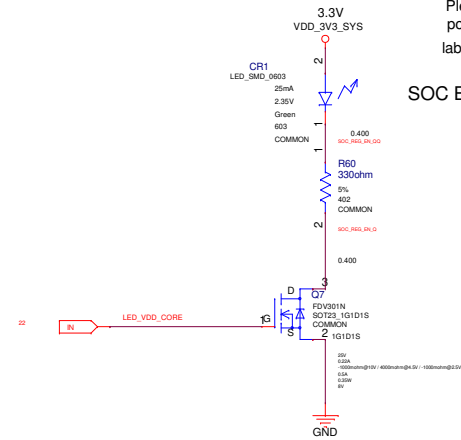
RESET



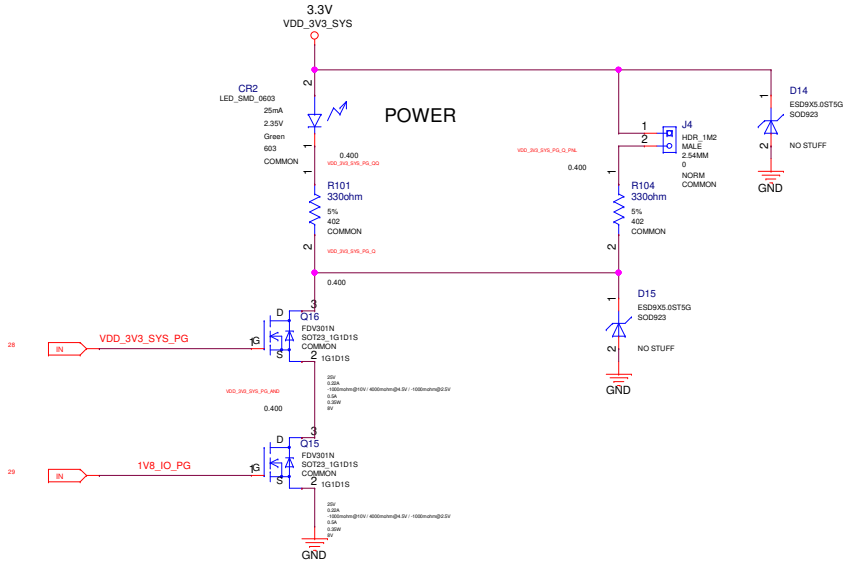
CAD NOTE:

Please place LEDs near the power button in the front label slik per text below

SOC EN



POWER



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Buttons and Mechanical

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# Revision History

## P2597-B03

Page 4: Added a red LED to indicate power is active on the CVM  
 Page 8: Replaced U21 due to EOL on previous part  
 Page 9: Changed an unused pull up to a TVS device on PCIe RST  
 PCIE\_WAKE\_L and PCIE\_CLKREQ  
 Page 10: Change R524 and R538 to 1.8k (tune for gyro bypass)  
 Page 10: Changed M.2 I2C to 1.8v  
 Page 12: Added discharge for VDD\_5V0\_IO\_SLP and VDD\_12V\_SLP  
 Added a red LED to 12v at PCIe connector  
 Changed DEV\_SLP buffer to OD  
 Page 13: Changed R9 to 100pF cap C205 (EU emissions)  
 Page 14: Changed R548 to 4.7k ohm and R544 to 100k  
 Page 15: Changed DBG I2C MUX to I2C repeater with enable  
 Added pull ups on inputs to U6  
 Page 16: Added 1206 0ohm resistors on J26  
 Added pull downs on J21 side of U22 and U7  
 Added reset connection to U22 and U7  
 Added ESD protection  
 Page 22: Added pull-up on J10 pin 48 for direct INA support  
 Added 0ohm resistor on the fan PWM to allow always on  
 Added a pull down on UART4\_TX  
 Added ESD protection to pins 4 and 6 of Q17  
 Page 24: Changed U11 EEPROM to AT24C02D-MAHM-T  
 Page 25: Added supervisor to hold Tegra in reset until 1.8v up  
 Page 27: Added additional bulk site on VDD\_MOD  
 Page 28: Changed 5v and 3.3v VR FETs for better thermal perf  
 Page 30: Added C201 and changed C49 to 1uF to filter DC loss  
 Page 33: Added ESD option for power LED

## P2597-B04

Corrected minor solderpaste issue

Page 12: Stuffed R315  
 Page 14: Changed R563 and R565 to 3.3ohm  
 Page 25: Unstuffed page

## BOM rev B

Page 23: Changed C36 to 0.1uF  
 Page 30: Changed C201 to 2.2uF and R105 to 20k

## P2597-C00

Page 13: Changed ENET CM Cap on transformer primary side  
 from one shared to individual caps  
 Page 14: Changed HDMI ESD diode to a package with  
 footprint compatible parts  
 Page 19: Added ON/OFF supervisor ckt to accomodate both  
 AutoPMIC & MobilePMIC On/Off control  
 Page 20: Added ON/OFF Glue logic to accomodate both  
 AutoPMIC & MobilePMIC On/Off control

## P2597-C01

Page 12: Changed SATA to right angle connetor to remove  
 interference with PCIe card  
 Page 19: Add seperate delay path for CARRIER\_PWR\_ON to  
 allow power cycle on RESET  
 Add option for ON/OFF PB or INT to drive WAKE  
 to allow short POWER\_BTN press to wake module  
 Add logic qualifier to INT for DFF to WAKE not  
 power down on PB press in SLEEP  
 Page 20: Add logic qualifier to gate initial momentary  
 pulse in state mode to remove state PWR\_ON glitch  
 Page 33: Changed 1x2 headers for buttons to 1x10 header,  
 so customer won't poke finger on header while  
 accessing buttons

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	REVISION HISTORY

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BOM REV	A		

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