# Programm

Pipeline



| l.add r8,r7,r5 | IF | ID | EX | WB | | | | | |
| l.addi r2,r2,0x4 | | IF | ID | EX | WB | | | | |
| l.add r8,r8,r13 | | | IF | (ID) | ID | EX | WB | | |
| l.sfne r8,r2 | | | | (IF) | IF | (ID) | (ID) | ID | EX | WB |

n-3   n-2   n-1   n   n+1   n+2   n+3   n+4   n+5   n+6

time [clock cycles]