BBGEN SPEC

Nwell: 0V -> 1.8V

Pwell: -1.3V -> 0.5V[1]

Rail to rail within 10 us

BBGEN Boundary Settings

Bound value		nwell		pwell pos		Bound value		pwell neg	
		LB	UB	LB pos	UB pos			LB neg	UB neg
31	11111	1.771	1.800	X	X	0	000000	0.000	-0.037
30	11110	1.713	1.771	X	X	-1	111111	-0.037	-0.111
29	11101	1.655	1.713	X	X	-2	111110	-0.111	-0.184
28	11100	1.597	1.655	X	X	-3	111101	-0.184	-0.258
27	11011	1.539	1.597	X	X	-4	111100	-0.258	-0.332
26	11010	1.481	1.539	X	X	-5	111011	-0.332	-0.406
25	11001	1.423	1.481	X	X	-6	111010	-0.406	-0.479
24	11000	1.365	1.423	X	X	-7	111001	-0.479	-0.553
23	10111	1.306	1.365	X	X	-8	111000	-0.553	-0.627
22	10110	1.248	1.306	X	X	-9	110111	-0.627	-0.701
21	10101	1.190	1.248	X	X	-10	110110	-0.701	-0.774
20	10100	1.132	1.190	X	X	-11	110101	-0.774	-0.848
19	10011	1.074	1.132	X	X	-12	110100	-0.848	-0.922
18	10010	1.016	1.074	X	X	-13	110011	-0.922	-0.996
17	10001	0.958	1.016	X	X	-14	110010	-0.996	-1.069
16	10000	0.900	0.958	X	X	-15	110001	-1.069	-1.143
15	01111	0.842	0.900	0.842	0.900	-16	110000	-1.143	-1.217
14	01110	0.784	0.842	0.784	0.842	-17	101111	-1.217	-1.290
13	01101	0.726	0.784	0.726	0.784	-18	101110	-1.290	-1.364
12	01100	0.668	0.726	0.668	0.726	-19	101101	-1.364	-1.438
11	01011	0.610	0.668	0.610	0.668	-20	101100	-1.438	-1.512
10	01010	0.552	0.610	0.552	0.610	-21	101011	-1.512	-1.585
9	01001	0.494	0.552	0.494	0.552	-22	101010	-1.585	-1.659
8	01000	0.435	0.494	0.435	0.494	-23	101001	X	X
7	00111	0.377	0.435	0.377	0.435	-24	101000	X	X
6	00110	0.319	0.377	0.319	0.377	-25	100111	X	X
5	00101	0.261	0.319	0.261	0.319	-26	100110	X	X
4	00100	0.203	0.261	0.203	0.261	-27	100101	X	X
3	00011	0.145	0.203	0.145	0.203	-28	100100	X	X
2	00010	0.087	0.145	0.087	0.145	-29	100011	X	X
1	00001	0.029	0.087	0.029	0.087	-30	100010	X	X
0	00000	0.000	0.029	0.000	0.029	-31	100001	X	X

LB/UB reflect the lower bound and upper bound reference voltages for the comparators for a window size setting of zero. For window sizes of one to three the upper bound is shifted by one to three rows.
X: not reachable, grey: possibly reachable, outside sepcifications

1 The actual range supported by the hardware is larger (up to 0.9V and down to -1.6V, however the models are not qualified outside this range and the risk is on side of the user.

BBGEN COMMANDS

Since the APB2CVP module does not support the byte enable feature of the CVP bus a command based programming model has been chosen for writing to the BBGEN controller.

Commands are sent by writing to the base address of the BBGEN controller. Only the lower 32 bits of the CVP interface are considered. The most significant byte is used as opcode, the remaining 3 lower byte are used as parameters.

For programming convenience parameters are always aligned to the next number of bytes and resized if the actual register size is smaller. In case of signed values the sign bit is kept while truncating the remaining bits to fit the actual register size, i.e. the behavior implemented with `resize` as defined in `ieee.numeric_std.all`. Thus the programmer can use uint8_t and int8_t when handling the parameters.

Conventions:
- : Dont care `S` : Value of sign bit * : 0 or 1

addr	w_data
0x00	31 ... 24 | 23 ... 16 | 15 ... 8 | 7 ... 0

NOP

Does nothing.

ADDRESS	Opcode	Byte 2	Byte 1	Byte 0
0x00	0x00	--------	--------	--------

NWELL_BOUND

Sets the nwell reference to the value specified, 5 bit unsigned int.

ADDRESS	Opcode			Nwell ref
0x00	0x01	--------	--------	---*****

PWELL_BOUND

Sets the nwell reference to the value specified, 6 bit signed int.

ADDRESS	Opcode			Pwell ref
0x00	0x02	--------	--------	SSS*****

NWELL_WSIZE

Sets the nwell reference window size (number of DAC steps between lower and upper bound). 2 bit unsigned int.

ADDRESS	Opcode			Nwell wsize
0x00	0x03	--------	--------	------**

PWELL_WSIZE

Sets the pwell reference window size (number of DAC steps between lower and upper bound). 2 bit unsigned int.

ADDRESS	Opcode			Pwell wsize
0x00	0x04	--------	--------	------**

IDLE_TIME

Idle time in cycles between two sampling events after reaching the well voltage. 16 bit unsigned int.

ADDRESS	Opcode		Idle timer value	
0x00	0x05	--------	********	********

SAMPLE_CLK

Sets the clock division from the 100 MHz reference clock in number of cycles per clock phase. 4 bit unsigned int.

ADDRESS	Opcode			Phase length
0x00	0x06	--------	--------	----****

SET_PRESET

Sets the selected preset register (2 bit unsigned int) to the specified pwell reference value (6 bit signed int) and nwell reference value (5 bit unsigned int)

ADDRESS	Opcode	Preset reg	Pwell ref	Nwell ref
0x00	0x07	------**	SSS*****	---*****

SELECT_PRESET

Sets the pwell and nwell bound to the values defined in the specified preset

ADDRESS	Opcode			Preset reg
0x00	0x08	--------	--------	------**

GND_TRANSITION_WSIZE

Sets the pwell reference window size for the transition from negative to positive and vice versa (number of DAC steps between lower and upper bound). 2 bit unsigned int.

ADDRESS	Opcode			Trans. wsize
0x00	0x09	--------	--------	------**

ENABLE_DISABLE

Allows to completely disable and enable the BBGEN, separately for nwell and pwell. Please note that reenabling the BBGEN will drive it into INIT mode where both wells will be driven towards GND to start up in a nown state. During this operation all logic in the controlled is asymmetrically biased and should be in a halt state to prevent unexpected behaviour.

ADDRESS	Opcode			
0x00	0x0A	--------	--------	------**

Bit	Value
0	Nwell: enable (1) / disable (0)
1	Pwell: enable (1) / disable (0)

CHARGEPUMP_CLK

Sets the clock division from the 100 MHz reference clock in number of cycles per clock phase. 4 bit unsigned int.

ADDRESS	Opcode			Phase length
0x00	0x0B	--------	--------	----****

BBGEN registers

The values of the bbgen register bank are memory mapped. Again, for convenience reasons all register values are aligned to full bytes and extended if needed to allow the programmer the use of int8_t or uint8_t.

Conventions:
- : Dont care S : Value of sign bit * : 0 or 1

addr	r_data			
0x00	31 ... 24	23 ... 16	15 ... 8	7 ... 0

Return register

Contains the values of the previous read operation and will be used in later versions to pass return values of commands to the programmer.

ADDRESS 0x00	Byte 3 --------	Byte 2 --------	Byte 1 --------	Byte 0 --------

Reference register

Returns the raw values passed to the monitor for selecting the comparator voltages.

ADDRESS 0x01	Pwell UB ref ---*****	Pwell LB ref ---*****	Nwell UB ref ---*****	Nwell LB ref ---*****

Status register

Returns status information as the raw values passed to the monitor for selecting the comparator voltages and the enable bits for nwell and pwell control, nwell and pwell enable as well as the transition window size for the transitions from positive to negative and vice versa on the pwell.

ADDRESS 0x02	 --------	 ------**	 -------*	 ********

Bit	Category	Value
0	Comperators	Pwell negative upper bound
1		Pwell negative lower bound
2		Pwell positive upper bound
3		Pwell positive lower bound
4		Nwell upper bound
5		Nwell lower bound
6	BBGEN enable bits	Nwell
7		pwell
8	Force sleep	Value of the force sleep signal
9	Weak driver	Value of the weak driver signal
10:15	reserved	
16	Transition window size	LSB
17		MSB
17:31	reserved	

Well bound and window size register

Returns the raw values passed to the monitor for selecting the comparator voltages.

ADDRESS	Pwell wsize	Nwell wsize	Pwell bound	Nwell bound
0x03	000000**	000000**	SSS*****	000*****

Idle time, chargepump and sample clock divider register

Returns the raw values passed to the monitor for selecting the comparator voltages.

ADDRESS	Sample clock	Chrgpump clk	Idle time
0x04	0000****	0000****	**********

Preset register 0 and 1

Returns the preset values for preset 0 and 1

ADDRESS	Pwell bound 1	Nwell bound 1	Pwell bound 0	Nwell bound 0
0x05	SSS*****	000*****	SSS*****	000*****

Returns the preset values for preset 2 and 3

ADDRESS	Pwell bound 3	Nwell bound 3	Pwell bound 2	Nwell bound 2
0x06	SSS*****	000*****	SSS*****	000*****