SONY

Diagonal 7.487 mm (Type 1/2.4) 21Mega-Pixel CMOS Image Sensor with Square Pixel for Color Cameras

IMX230-0AQH5-C

General description and application

IMX230 is a diagonal 7.487mm (Type 1/2.4) 21 Mega-pixel CMOS active pixel type stacked image sensor with a square pixel array. It adopts Exmor RS™ technology to achieve high speed image capturing by column parallel A/D converter circuits and high sensitivity and low noise image (comparing with conventional CMOS image sensor) through the backside illuminated imaging pixel structure. R, G, and B pigment primary color mosaic filter is employed. By introducing spatially varying exposure technology, high dynamic range still pictures and movies are achievable. It equips an electronic shutter with variable integration time. It operates with three power supply voltages: analog 2.5 V, digital 1.1 V and 1.8 V for input/output interface and achieves low power consumption.
IMX230 is designed for use in cellular phones or tablet devices*[1].

Functions and Features

- ◆ Back-illuminated and stacked CMOS image sensor Exmor RS™
- ◆ Single Frame High Dynamic Range (HDR) with equivalent full pixels.
- ◆ High signal to noise ratio (SNR).
- ◆ Full resolution @24fps (Normal / HDR). 4K2K @30fps (Normal / HDR) 1080p @60fps (Normal / HDR)
- ◆ Output video format of RAW10/8, COMP8/6.
- ◆ Pixel binning readout and H/V sub-sampling function.
- ◆ Advanced Noise Reduction (Chroma noise reduction and RAW noise reduction).
- ◆ Independent flipping and mirroring.
- ◆ CSI-2 serial data output (MIPI 2lane/4lane, Max. 1.5Gbps/lane, D-PHY spec. ver. 1.1 compliant)
- ◆ 2-wire serial communication.
- ◆ Two PLLs for independent clock generation for pixel control and data output interface.
- ◆ Dynamic Defect Pixel Correction.
- ◆ Zero shutter lag.
- ◆ Power-on reset function
- ◆ Dual sensor synchronization operation.
- ◆ 9K bit of OTP ROM for users.
- ◆ Built-in temperature sensor

NOTE)
1. When using this product for another application, Sony does not guarantee the quality and reliability of product. Therefore, don't use this for applications other than cellular phone and Tablet PCs. Consult your Sony sales representative if you have any questions.

Exmor RS

* Exmor RS is a trademark of Sony Corporation. The Exmor RS is a Sony's CMOS image sensor with high-resolution, high-performance and compact size by replacing a supporting substrate in Exmor R™ which changed fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type, with layered chips formed signal processing circuits.

Device Structure

◆ CMOS image sensor
◆ Image size : Diagonal 7.487 mm (Type 1/2.4)
◆ Total number of pixels : 5408 (H) × 4112 (V) approx. 22.24 M pixels
◆ Number of effective pixels : 5360 (H) × 4032 (V) approx. 21.61 M pixels
◆ Number of active pixels : 5344 (H) × 4016 (V) approx. 21.46 M pixels
◆ Chip size : 7.216 mm (H) × 5.497 mm (V)
◆ Unit cell size : 1.12 µm (H) × 1.12 µm (V)
◆ Substrate material : Silicon

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	-0.3 to +4.2	V	refer to VSS level
Supply voltage (digital)	VDIG	-0.3 to +1.54	V	
Supply voltage (interface)	VIF	-0.3 to +2.52	V	
Input voltage (digital)	VI	-0.3 to +2.52	V	
Output voltage (digital)	VO	-0.3 to +2.52	V	
Guaranteed Operating temperature	TOPR	-20 to +70	˚C	
Guaranteed storage temperature	TSTG	-30 to +80	˚C	
Guaranteed performance temperature	TSPEC	-20 to +60	˚C	

Recommended Operating Voltage

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	2.5 ± 0.1 V	V	refer to VSS level
Supply voltage (digital)	VDIG	1.1 ± 0.1	V	
Supply voltage (interface)	VIF	1.8 ± 0.1	V	

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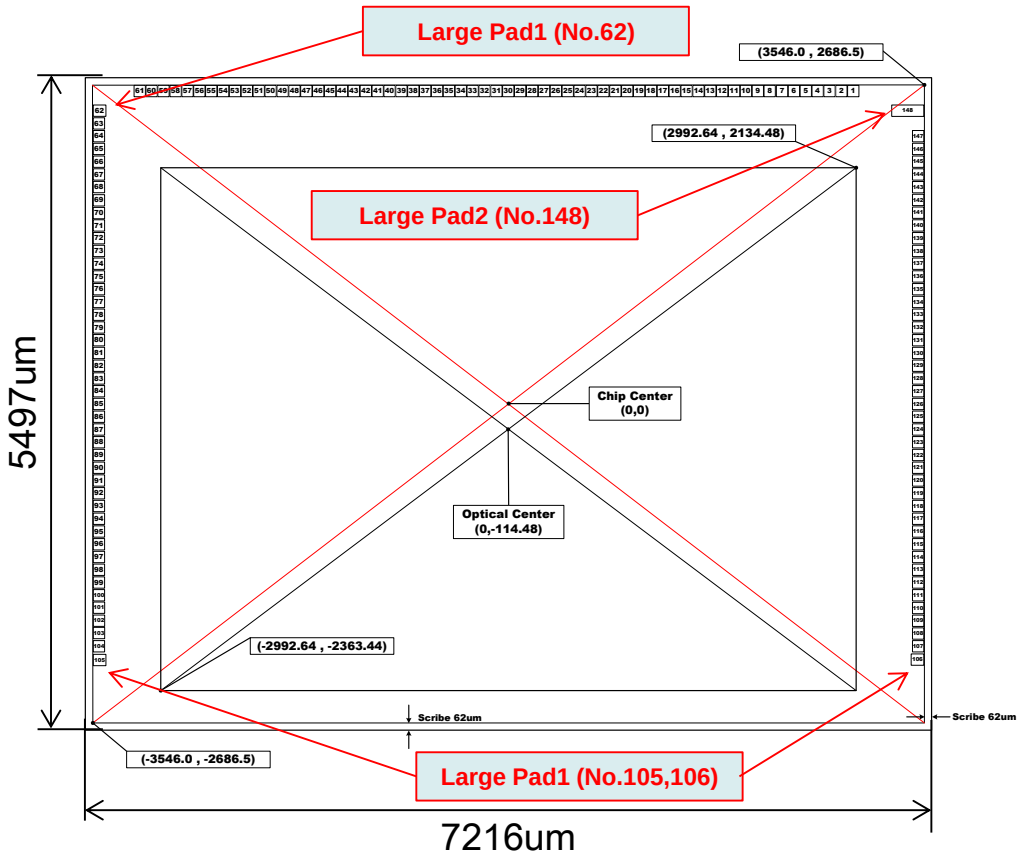
Contents

1. Chip Center and Optical Center



※Actual size of a chip will be smaller than indicated when dicing (scribe) is taken into account

Figure 1 Chip Center and Optical Center (x and y coordinates in μm)

2. Pin Coordinates

Table 1 Pin Coordinates

No.	Symbol	X	Y
1	VDDMODE1	3240	2630
2	VDDMODE0	3132	2630
3	VBO1	3024	2630
4	TREGEN	2916	2630
5	VDDLSC1	2808	2630
6	VSSLSC1	2700	2630
7	VDDMIO1	2592	2630
8	XCLR	2484	2630
9	POREN	2376	2630
10	INCK	2268	2630
11	XPORCD	2160	2630
12	VDDHVC2	2052	2630
13	ATBVCM	1944	2630
14	LPFIN2	1836	2630
15	LPFIN1	1728	2630
16	SENBIAS	1620	2630
17	VSSHVC2	1512	2630
18	VSSHVC1A	1404	2630
19	VSSHVC1B	1296	2630
20	VSSHVC1C	1188	2630
21	VCMM1	1080	2630
22	VCMM2	972	2630
23	VCMP1	864	2630
24	VCMP2	756	2630
25	VDDHVC1A	648	2630
26	VDDHVC1B	540	2630
27	VDDHVC1C	432	2630
28	VSSLSC2	324	2630
29	VDDLSC2	216	2630
30	VDDLSC3	108	2630
31	VDDMIO2	0	2630
32	VSSLSC3	-108	2630
33	D4N	-216	2630
34	D4P	-324	2630
35	D2N	-432	2630
36	D2P	-540	2630
37	VDDLIO2	-648	2630
38	VDDLSC4	-756	2630
39	VSSLSC4	-864	2630
40	CKN	-972	2630
41	CKP	-1080	2630
42	VSSLSC5	-1188	2630
43	VDDLSC5	-1296	2630
44	VDDLIO1	-1404	2630
45	D1N	-1512	2630
46	D1P	-1620	2630
47	D3N	-1728	2630
48	D3P	-1836	2630
49	VSSLSC6	-1944	2630
50	VDDLPL2	-2052	2630

No.	Symbol	X	Y
51	VDDLPL1	-2160	2630
52	VSSLPL	-2268	2630
53	SWDIO	-2376	2630
54	SWTCK	-2484	2630
55	GPO	-2592	2630
56	VSSLSC7	-2700	2630
57	VDDLSC6	-2808	2630
58	VDDMIO3	-2916	2630
59	VSSSUB	-3024	2630
60	VDDSUB	-3132	2630
61	VBO2	-3240	2630
62	VSSHSN1	-3489	2346
63	VDDHSN1	-3489	2238
64	VPL1	-3489	2130
65	VRL1	-3489	2022
66	VPI2	-3489	1914
67	SCK	-3489	1806
68	SDI	-3489	1698
69	SDO	-3489	1590
70	SCSB	-3489	1482
71	GYINT	-3489	1374
72	VDDMIO4	-3489	1266
73	VSSLSC8	-3489	1158
74	VSSLSC9	-3489	1050
75	VDDLSC7	-3489	942
76	VDDLSC8	-3489	834
77	SCL	-3489	726
78	SDA	-3489	618
79	SLASEL	-3489	510
80	FSTROBE	-3489	402
81	TESTOUT	-3489	294
82	VDDMIO5	-3489	186
83	VSSLSC10	-3489	78
84	VDDLSC9	-3489	-30
85	VDDHSN2	-3489	-138
86	VSSHSN2	-3489	-246
87	VDDHFIL	-3489	-354
88	TENABLE	-3489	-462
89	TEST1	-3489	-570
90	TEST2	-3489	-678
91	TEST3	-3489	-786
92	VDDMIO6	-3489	-894
93	VSSLSC11	-3489	-1002
94	VSSLSC12	-3489	-1110
95	VDDLSC10	-3489	-1218
96	VDDLSC11	-3489	-1326
97	VDDLVS1	-3489	-1434
98	VSSLVS1	-3489	-1542
99	VSSLCN1	-3489	-1650
100	VDDLCN1	-3489	-1758

No.	Symbol	X	Y
101	VSSLCB1	-3489	-1866
102	VDDHCM1	-3489	-1974
103	VSSHSN3	-3489	-2082
104	VPL2	-3489	-2190
105	VDDHSN3	-3489	-2298
106	VDDHSN4	3489	-2298
107	VPL3	3489	-2190
108	VSSHSN4	3489	-2082
109	VDDHCM2	3489	-1974
110	VSSLCB2	3489	-1866
111	VDDLCN2	3489	-1758
112	VSSLCN2	3489	-1650
113	VDDLSC12	3489	-1542
114	VDDLSC13	3489	-1434
115	VSSLSC13	3489	-1326
116	VSSLSC14	3489	-1218
117	VDDLSC14	3489	-1110
118	VSSHAN	3489	-1002
119	VDDHAN	3489	-894
120	TVMON	3489	-786
121	TVCDSIN	3489	-678
122	VDDHSN5	3489	-570
123	VSSHSN5	3489	-462
124	VDDMIO7	3489	-354

No.	Symbol	X	Y
125	VSSLVS2	3489	-246
126	VDDLVS2	3489	-138
127	VDDLSC15	3489	-30
128	VDDLSC16	3489	78
129	VSSLSC15	3489	186
130	VSSLSC16	3489	294
131	VCD	3489	402
132	VSSHCD	3489	510
133	VDDHCD	3489	618
134	VSSHVB	3489	726
135	VDDHVB	3489	834
136	VPE	3489	942
137	VBE	3489	1050
138	VCK	3489	1158
139	VCP	3489	1266
140	VSSHCP	3489	1374
141	VDDHCP	3489	1482
142	VDDLSC17	3489	1590
143	VSSLSC17	3489	1698
144	VPI1	3489	1806
145	VRL2	3489	1914
146	VPL4	3489	2022
147	VDDHSN6	3489	2130
148	VSSHSN6	3453	2344

3. Pin Description

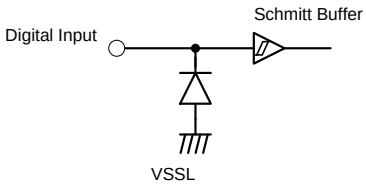
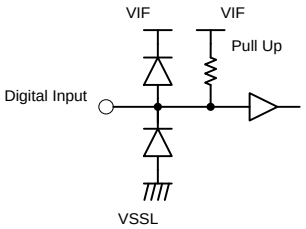
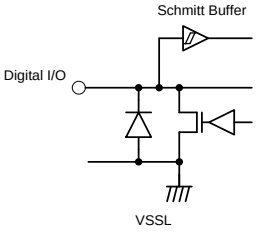
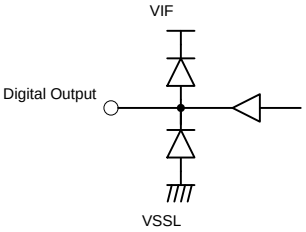
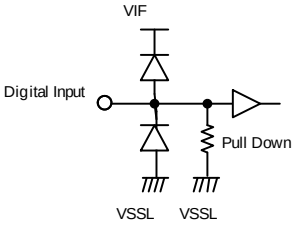
Table 2 Pin Description

No.	Symbol	I/O	A/D	Description	Remarks
1	VDDMODE1	I	D	digital input	
2	VDDMODE0	I	D	digital input	
3	VBO1	Power	A	VANA power supply	
4	TREGEN	O	D	digital output	NC
5	VDDLSC1	Power	D	VDIG power supply	
6	VSSLSC1	GND	D	VDIG GND	
7	VDDMIO1	Power	D	VIF power supply	
8	XCLR	I	D	digital input	NC
9	POREN	I	D	digital input	NC
10	INCK	I	D	digital input	Clock Input
11	XPORCD	I	D	digital input	NC
12	VDDHVC2	Power	A	VANA power supply	
13	ATBVCM	O	A	analog output	NC
14	LPFIN2	I	A	analog input	
15	LPFIN1	I	A	analog input	
16	SENBIAS	O	A	analog output	NC
17	VSSHVC2	GND	A	VANA GND	
18	VSSHVC1A	GND	A	VANA GND	
19	VSSHVC1B	GND	A	VANA GND	
20	VSSHVC1C	GND	A	VANA GND	
21	VCMM1	O	A	analog output	NC
22	VCMM2	O	A	analog output	NC
23	VCMP1	O	A	analog output	NC
24	VCMP2	O	A	analog output	NC
25	VDDHVC1A	Power	A	VANA power supply	
26	VDDHVC1B	Power	A	VANA power supply	
27	VDDHVC1C	Power	A	VANA power supply	
28	VSSLSC2	GND	D	VDIG GND	
29	VDDLSC2	Power	D	VDIG power supply	
30	VDDLSC3	Power	D	VDIG power supply	
31	VDDMIO2	Power	D	VIF power supply	
32	VSSLSC3	GND	D	VDIG GND	
33	D4N	O	D	digital output	MIPI output（DATA）
34	D4P	O	D	digital output	MIPI output（DATA）
35	D2N	O	D	digital output	MIPI output（DATA）
36	D2P	O	D	digital output	MIPI output（DATA）
37	VDDLIO2	Power	D	VDIG power supply	
38	VDDLSC4	Power	D	VDIG power supply	
39	VSSLSC4	GND	D	VDIG GND	
40	CKN	O	D	digital output	MIPI output（CLK）
41	CKP	O	D	digital output	MIPI output（CLK）
42	VSSLSC5	GND	D	VDIG GND	
43	VDDLSC5	Power	D	VDIG power supply	
44	VDDLIO1	Power	D	VDIG power supply	
45	D1N	O	D	digital output	MIPI output（DATA）
46	D1P	O	D	digital output	MIPI output（DATA）
47	D3N	O	D	digital output	MIPI output（DATA）
48	D3P	O	D	digital output	MIPI output（DATA）

No.	Symbol	I/O	A/D	Description	Remarks
49	VSSLSC6	GND	D	VDIG GND	
50	VDDLPL2	Power	D	VDIG power supply	
51	VDDLPL1	Power	D	VDIG power supply	
52	VSSLPL	GND	D	VDIG GND	
53	SWDIO	I/O	D	digital I/O	NC
54	SWTCK	I	D	digital input	NC
55	GPO	O	D	digital output	NC
56	VSSLSC7	GND	D	VDIG GND	
57	VDDLSC6	Power	D	VDIG power supply	
58	VDDMIO3	Power	D	VIF power supply	
59	VSSSUB	GND	D	VDIG GND	
60	VDDSUB	Power	A	VANA power supply	
61	VBO2	Power	A	VANA power supply	
62	VSSHSN1	GND	A	VANA GND	
63	VDDHSN1	Power	A	VANA power supply	
64	VPL1	Minus	A	analog input	
65	VRL1	Minus	A	analog input	
66	VPI2	Power	A	analog input	
67	SCK	O	D	digital output	NC
68	SDI	I/O	D	digital I/O	
69	SDO	O	D	digital output	NC
70	SCSB	O	D	digital output	NC
71	GYINT	I	D	digital input	
72	VDDMIO4	Power	D	VIF power supply	
73	VSSLSC8	GND	D	VDIG GND	
74	VSSLSC9	GND	D	VDIG GND	
75	VDDLSC7	Power	D	VDIG power supply	
76	VDDLSC8	Power	D	VDIG power supply	
77	SCL	I/O	D	digital I/O	I2C serial communication.
78	SDA	I/O	D	digital I/O	I2C serial communication.
79	SLASEL	I	D	digital input	I2C slave address select
80	FSTROBE	O	D	digital output	Flash strobe
81	TESTOUT	O	D	digital output	NC
82	VDDMIO5	Power	D	VIF power supply	
83	VSSLSC10	GND	D	VDIG GND	
84	VDDLSC9	Power	D	VDIG power supply	
85	VDDHSN2	Power	A	VANA power supply	
86	VSSHSN2	GND	A	VANA GND	
87	VDDHFIL	Power	A	VANA power supply	
88	TENABLE	I	D	digital input	NC
89	TEST1	I	D	digital input	NC
90	TEST2	I	D	digital input	NC
91	TEST3	I	D	digital input	NC
92	VDDMIO6	Power	D	VIF power supply	
93	VSSLSC11	GND	D	VDIG GND	
94	VSSLSC12	GND	D	VDIG GND	
95	VDDLSC10	Power	D	VDIG power supply	
96	VDDLSC11	Power	D	VDIG power supply	
97	VDDLVS1	Power	D	VDIG power supply	
98	VSSLVS1	GND	D	VDIG GND	
99	VSSLCN1	GND	D	VDIG GND	
100	VDDLCN1	Power	D	VDIG power supply	

No.	Symbol	I/O	A/D	Description	Remarks
101	VSSLCB1	GND	D	VDIG GND	
102	VDDHCM1	Power	A	VANA power supply	
103	VSSHSN3	GND	A	VANA GND	
104	VPL2	Minus	A	analog input	
105	VDDHSN3	Power	A	VANA power supply	
106	VDDHSN4	Power	A	VANA power supply	
107	VPL3	Minus	A	analog input	
108	VSSHSN4	GND	A	VANA GND	
109	VDDHCM2	Power	A	VANA power supply	
110	VSSLCB2	GND	D	VDIG GND	
111	VDDLCN2	Power	D	VDIG power supply	
112	VSSLCN2	GND	D	VDIG GND	
113	VDDLSC12	Power	D	VDIG power supply	
114	VDDLSC13	Power	D	VDIG power supply	
115	VSSLSC13	GND	D	VDIG GND	
116	VSSLSC14	GND	D	VDIG GND	
117	VDDLSC14	Power	D	VDIG power supply	
118	VSSHAN	GND	A	VANA GND	
119	VDDHAN	Power	A	VANA power supply	
120	TVMON	O	A	analog output	NC
121	TVCDSIN	I	A	analog input	NC
122	VDDHSN5	Power	A	VANA power supply	
123	VSSHSN5	GND	A	VANA GND	
124	VDDMIO7	Power	D	VIF power supply	
125	VSSLVS2	GND	D	VDIG GND	
126	VDDLVS2	Power	D	VDIG power supply	
127	VDDLSC15	Power	D	VDIG power supply	
128	VDDLSC16	Power	D	VDIG power supply	
129	VSSLSC15	GND	D	VDIG GND	
130	VSSLSC16	GND	D	VDIG GND	
131	VCD	Minus	A	analog output	
132	VSSHCD	GND	A	VANA GND	
133	VDDHCD	Power	A	VANA power supply	
134	VSSHVB	GND	A	VANA GND	
135	VDDHVB	Power	A	VANA power supply	
136	VPE	Power	A	analog output	
137	VBE	Power	A	analog output	
138	VCK	O	A	analog output	
139	VCP	Minus	A	analog output	
140	VSSHCP	GND	A	VANA GND	
141	VDDHCP	Power	A	VANA power supply	
142	VDDLSC17	Power	D	VDIG power supply	
143	VSSLSC17	GND	D	VDIG GND	
144	VPI1	Power	A	analog input	
145	VRL2	Minus	A	analog input	
146	VPL4	Minus	A	analog input	
147	VDDHSN6	Power	A	VANA power supply	
148	VSSHSN6	GND	A	VANA GND	

4. Input/Output Equivalent Circuit

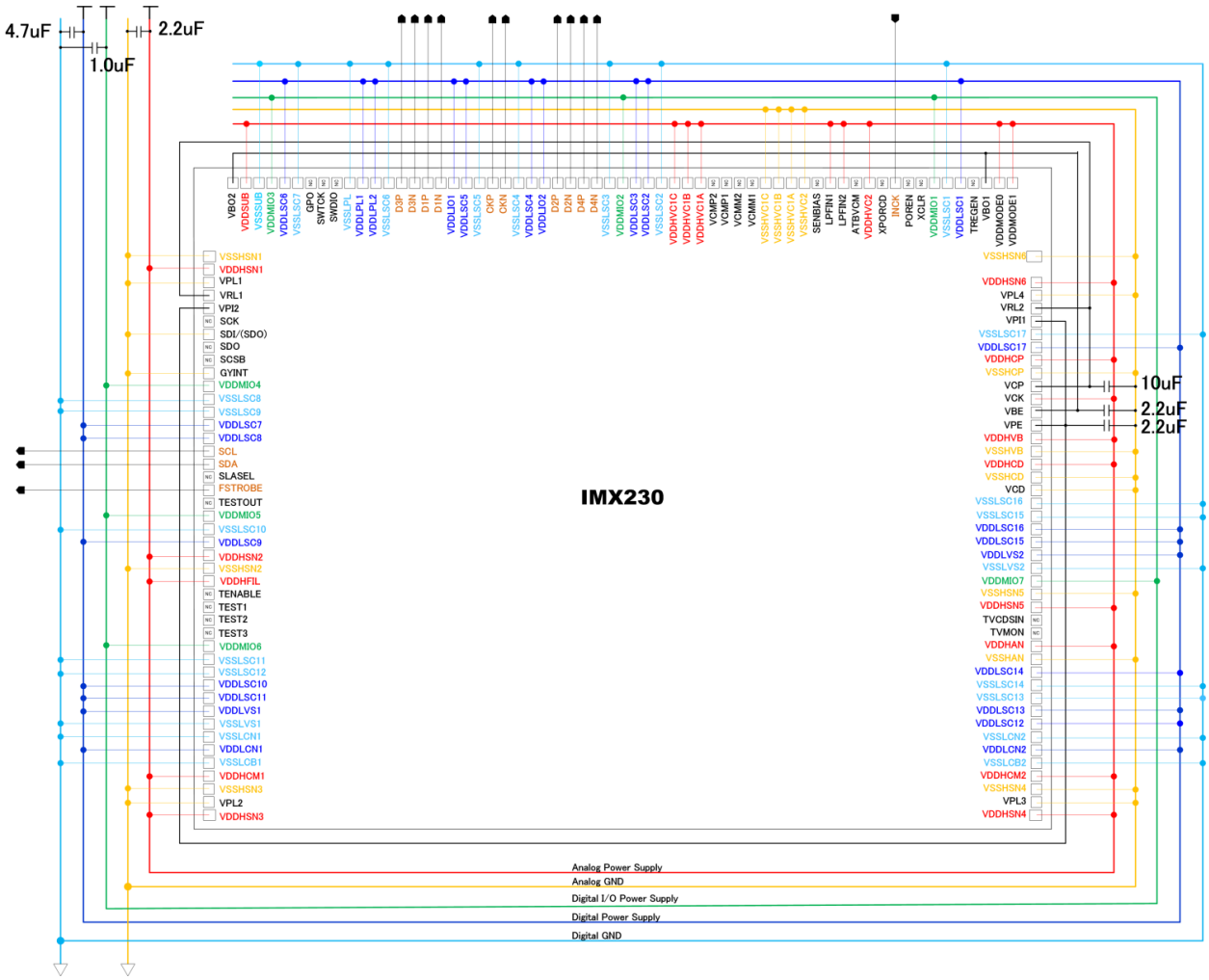
Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
INCK		XCLR	
SCL SDA		REGEN FSTROBE	
SLASEL			

VDDH : 2.5 V power supply
VSSH : 2.5 V GND

VIF : 1.8 V power supply
VSSL : VDIG GND

Figure 2 Input/Output Equivalent Circuit

5. Peripheral Circuit Diagram



Note : When fixing the potential of the chip back side, connect it to GND.
Note : Two 4.7uF in parallel is able to be used instead of a 10uF capacitor.

Figure 3 Peripheral Circuit (Recommended schematics)

6. Functional Description

6-1 System Outline

IMX230 is a CMOS active pixel type image sensor which adopts the Exmor RS™ technology to achieve high sensitivity, low noise, and high speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, digital amplifier, image binning circuit, timing control circuit for imaging size and frame rate, CSI2 image data high speed serial interface, PLL oscillator, and serial communication interface to control these functions.
Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.
A onetime programmable memory is embedded in the chip for storing the user data. It has 9 K-bit for users, 16 K-bit as a whole.

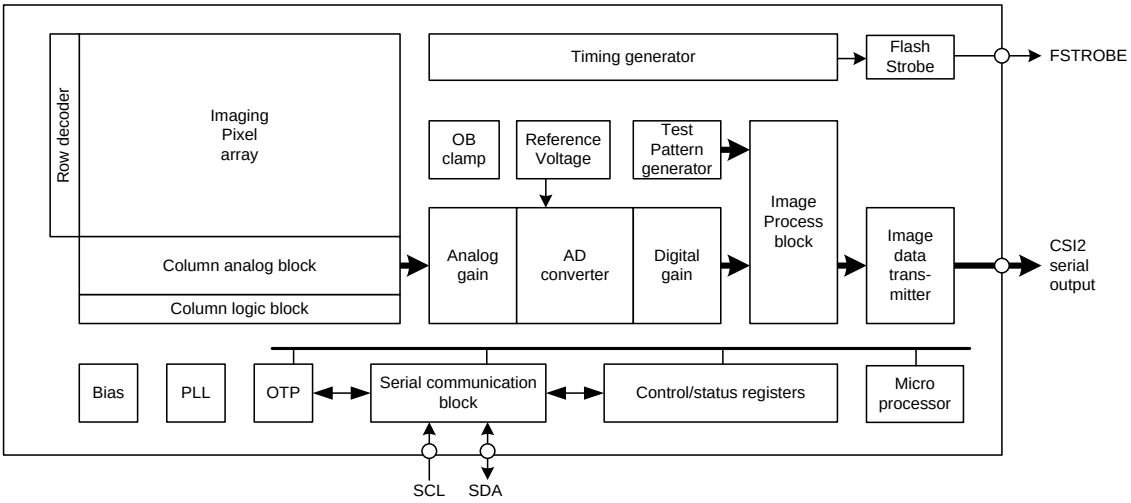


Figure 4 Overview of functional block diagram

6-2 Control register setting by the serial communication

The IMX can use the 2-wire serial communication method for sensor control. These specifications are described for sensor control using the 2-wire serial communication as follows. See Application Notes for more details of each function beyond the following description.

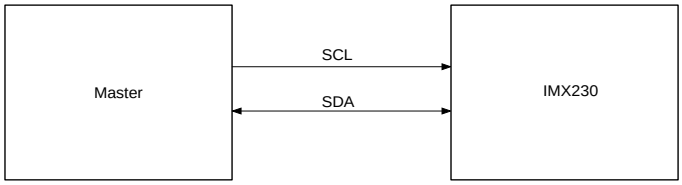


Figure 5 2-wire serial communication

6-2-1 2-wire Serial Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Instance (CCI). CCI is an I2C fast-mode compatible interface, and the data transfer protocol is I2C standard.
This 2-wire serial communication circuit can be used to access the control-registers and status-registers of IMX.

Table 3 Description of 2-wire Serial Communication Pins

pin name	description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of IMX230 are mapped on the 16-bit address space and the register categories shown as below. Detail register information is shown in Register Map.

Table 4 Specification of register address map for 2-wire serial communication

	address range	description
I^2C register	0x0000 - 0x0fff	Configuration register Read Only and Read/Write Dynamic register
	0x1000 - 0x1fff	Parameter limit register Read Only static resister
	0x2000 - 0x2fff	Reserved
	0x3000 - 0xffff	Manufacture specific register

6-2-2 Communication Protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

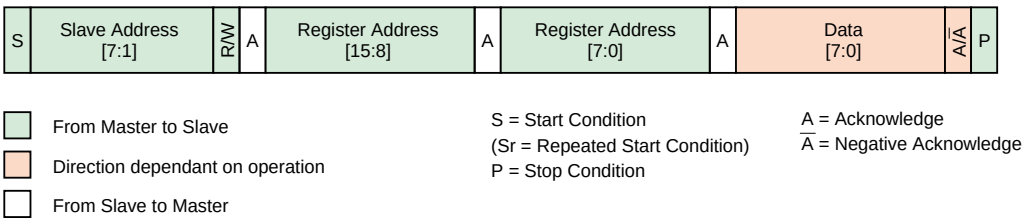
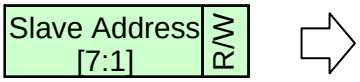


Figure 6 2-wire serial communication protocol

IMX230 has a default slave address shown as below.
The slave address is selectable by pin connection of SLASEL.
When called by the selected slave address, serial communication interface is activated.
Duplication of the address on the same bus must be prevented.
*For other slave address options, refer to Application Note.



Slave Address (Read or Write) * See Table 5 for R/W bit	SLASEL (pin#79)
MSB LSB 0 0 1 0 0 0 0 R/W	L or NC
MSB LSB 0 0 1 1 0 1 0 R/W	H

R/W shows the direction of communication.

Figure 7 Slave address

Table 5 R/W bit

R/W bit	direction of communication
0	Write (Master → Sensor)
1	Read (Sensor → Master)

6-3 Clock generation and PLL

IMX230 equips embedded PLL to generate the necessary internal clocks and CSI2 transmission clocks. Set the related registers according to the operation condition. See Application Notes for more details of each function.

6-3-1 Clock System Diagram

IMX230 is equipped with two PLL, One outputs VTCL for image processing, the other is OPCK for MIPI output.
Based on the clock that is input in the range of 6-27MHz, output of 400-1200MHz can be of the PLL for VTCK, PLL of OPCK for is capable of outputting 400-1500MHz.
It is possible to divide the range of 1/1 to 1/4 of the PLL VTCK, and to multiply in the range of 34-200.
It is possible to divide the range of 1/1 to 1/15 of the PLL OPCK, and to multiply in the range of 15-1500.

Typically, IMX230 can be driven from the dual PLL mode to operate the both of PLLs, but it also supports single PLL mode to move only one side of the PLL.

In PLL single mode, PREPLLCK_OP_DIV and PLL_OP_MPY are ignored..

.

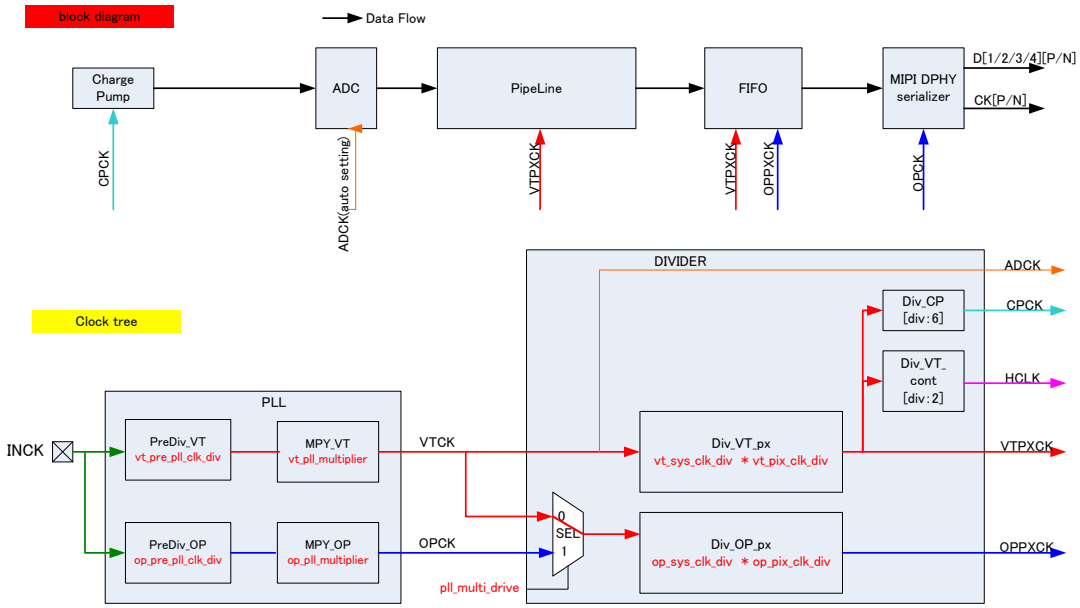


Figure 8 Clock System Diagram (PLL single mode)

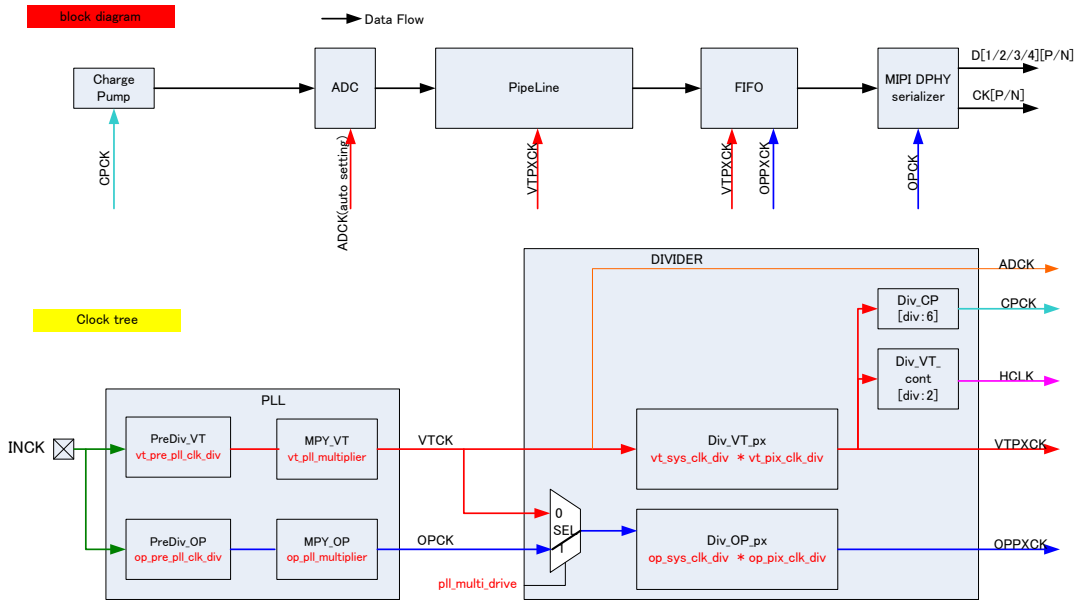


Figure 9 Clock System Diagram (PLL dual mode)

6-4 Description of operation clocks

The followings are general descriptions for each clock. See Application Note for more detail.

6-4-1 INCK

INCK is an external input clock (6 to 27MHz). See “AC characteristics” for electrical requirements to INCK.

6-4-2 VTCK, OPCK(PLL output)

These clocks are the root of all the operation clocks in IMX230 and it designates the data rate. DCKP/DCKN; CSI2 interface clock is generated from OPCK by dividing into 1/2 (or1/4) frequency since the interface is operated in double data rate format.

6-4-3 VTPXCK Clock

The clock for internal image processing is generated by dividing into 1/8, 1/10, 1/12, 1/14, 1/16, 1/18, 1/20, 1/24, 1/28, 1/32, 1/36 or 1/40 frequency. This clock is used as the base of integration time, frame rate, and etc.

6-4-4 OPPXCK Clock

The clock for internal image processing is generated by dividing into 1/6, 1/8, 1/10, 1/12, 1/16 or 1/20 frequency according to the word length of the CSI2 interface. This clock is designating the pixel rate and etc.

6-5 Image Readout Operation

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, IMX230 outputs the image data.

See Application Notes for more details of each function.

6-5-1 Physical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with pin #1 located at the upper left corner.

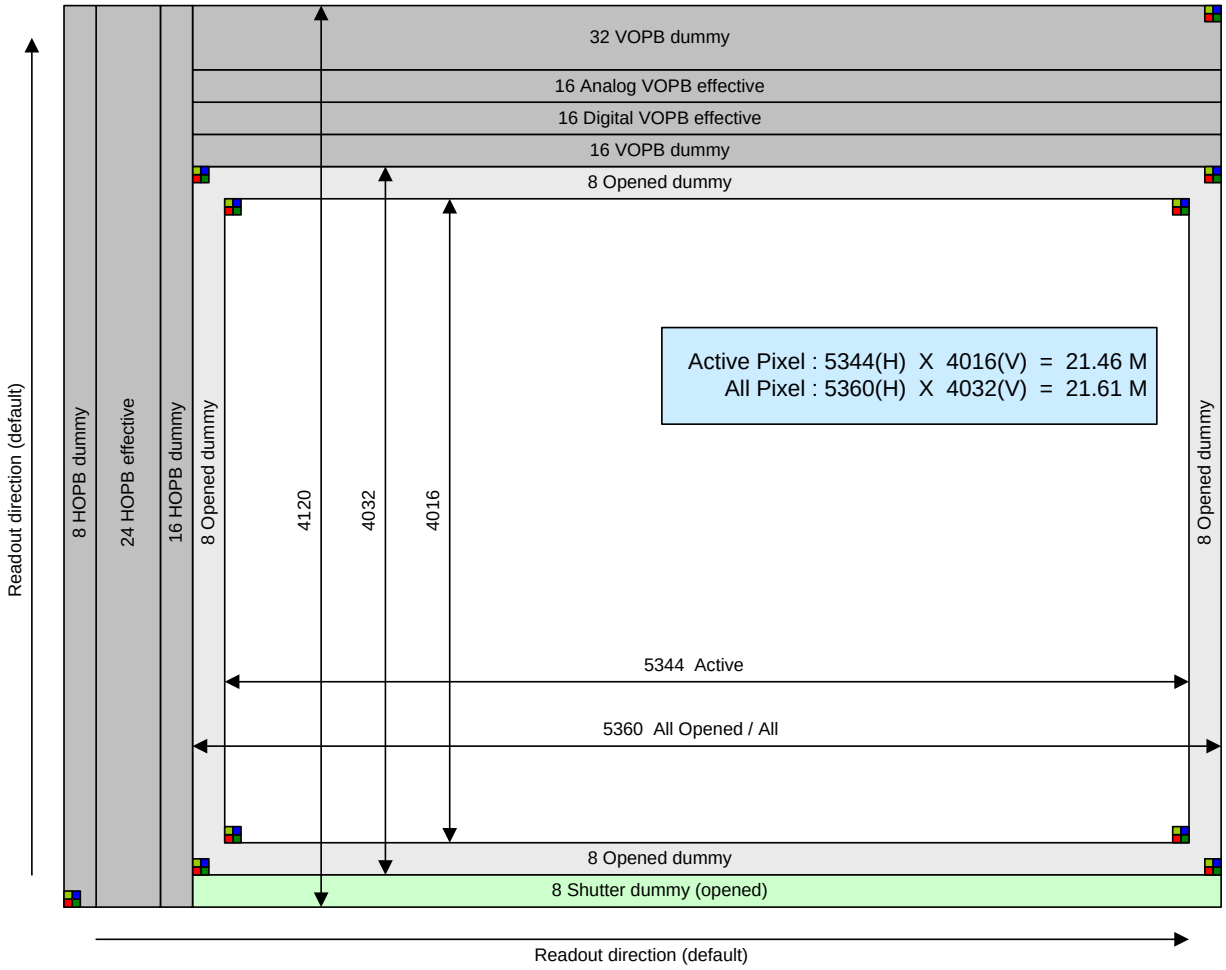


Figure 10 physical alignment of the imaging pixel array

6-5-2 Color coding and order of reading image date

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals, respectively. The line with R & Gr signals and the line with Gb & B signals are output one after the other alternatively.

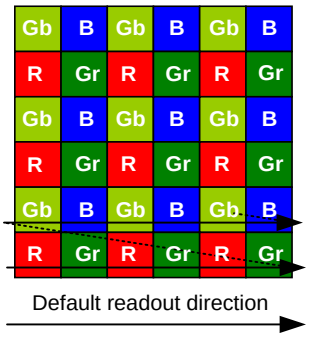


Figure 11 Color coding alignment

6-6 Output Image Format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.

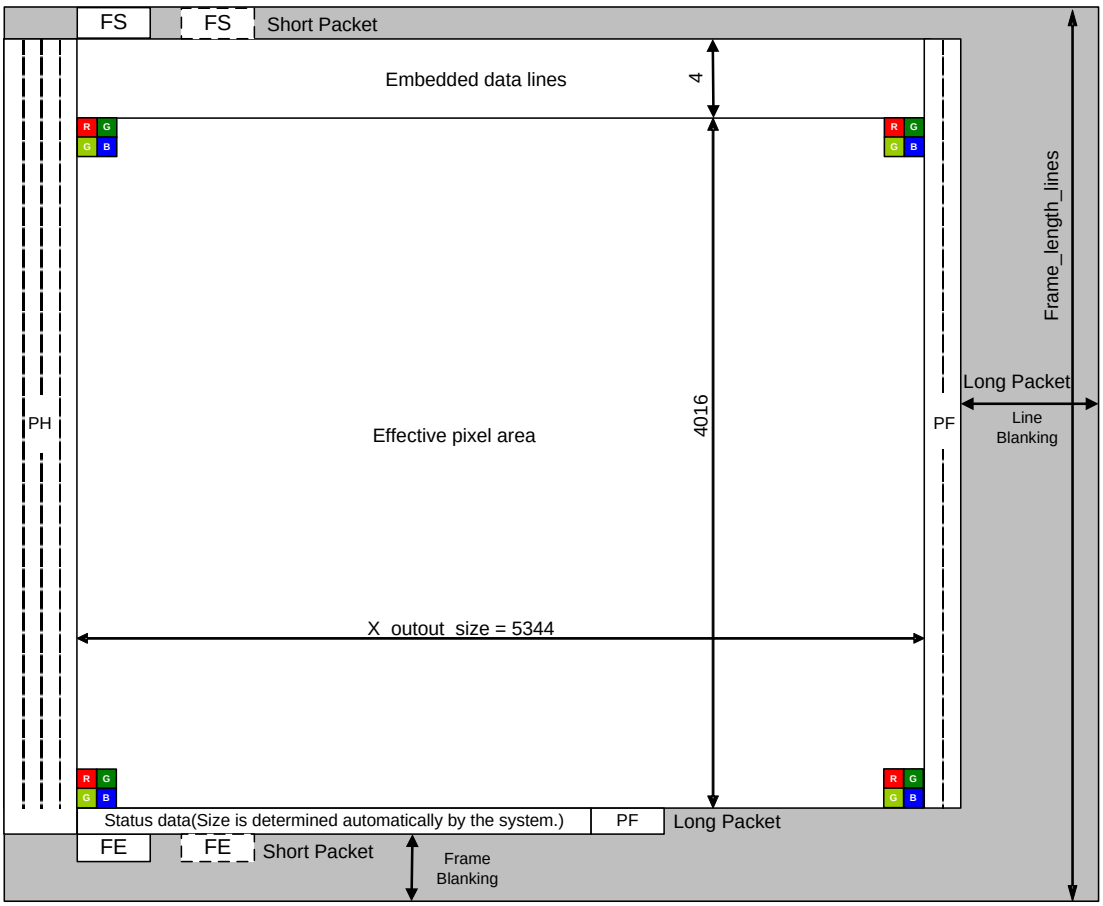


Figure 12 Full pixel output mode data structure

If same virtual channel ID is used for both pixel and Stats data, only one FS and one FE will be generated.

6-6-1 Embedded Data Line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame.
The corresponding registers are indicated by “EDL” column of the Register Map.
An unfixed value is output when not outputting embedded data.

See Application Notes for contents and output sequence of Embedded Data Lines.

6-6-2 STATS data control

STATS data is average value of luminance for each sub-block of a given field-of-view (FOV) setting of the sensor.
Number of sub-block is varied according to the size of FOV.
STATS data is 14bits values and sent via MIPI (embedded) or I2C.
The sensor can be configured to output “STATS data” during frame blanking for HDR movie use.

6-6-3 Image size of mode

IMX230 can capture and output full size, cropped/scaled image in combination with the normal mode or HDR mode.
Examples are shown in the table below. Definitions of each parameter are shown in the below figure.

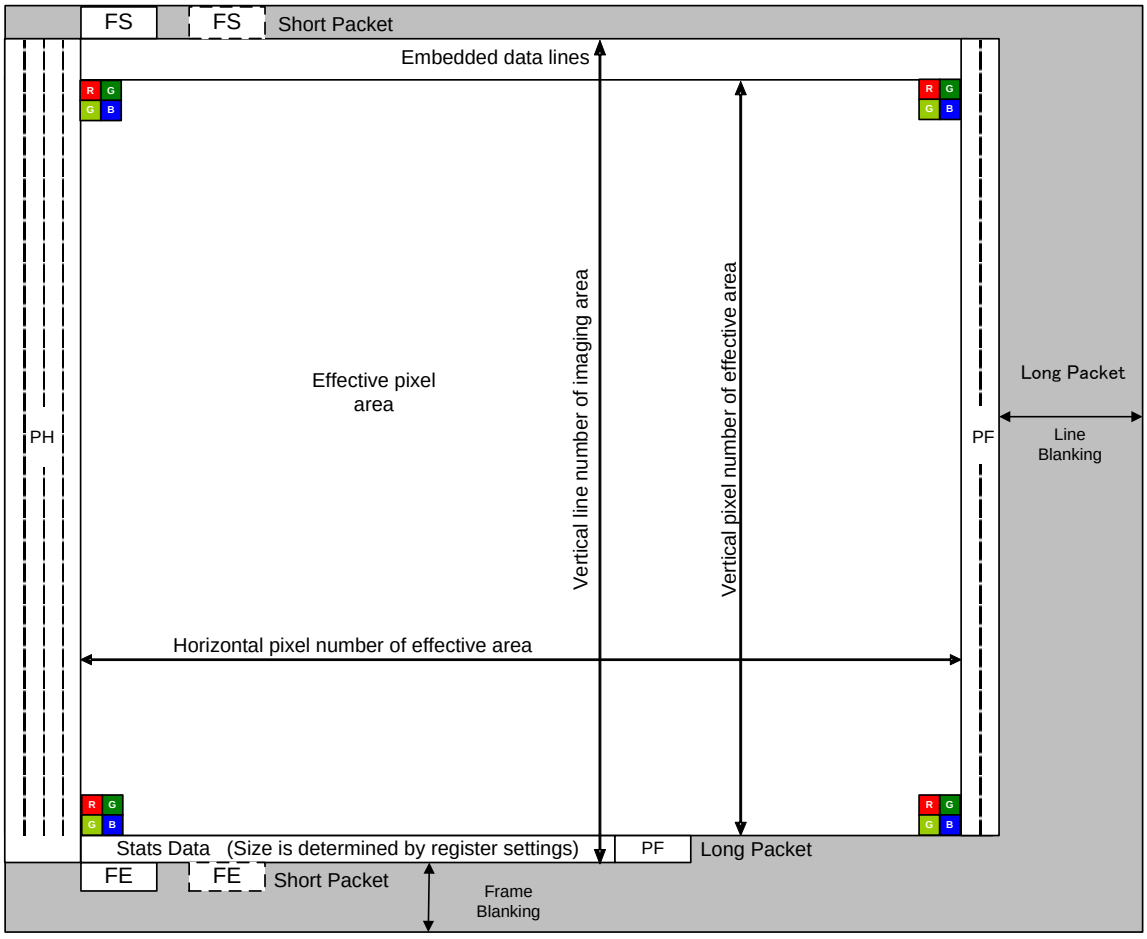


Figure 13 Image size parameter definition

Table 6 modes and image sizes

		Modes									
		Full resolution		2 Binning (V: 1/2, H: 1/2)		HDR Full-resolution		HDR 2 binning (V: 1/2, H: 1/2)		4 Binning (V: 1/4, H: 1/4)	
Number of vertical lines in imaging area		4020-4022		2012-2014		4020-4022		2012-2014		740-742	
Number of horizontal pixels in effective area		5334		2672		5334		2672		1296	
Number of lines and start position		Start position	Number of lines	Start position	Number of lines	Start position	Number of lines	Start position	Number of lines	Start position	Number of lines
Name of the areas	Frame start	1	1	1	1	1	1	1	1	1	1
	Embedded data lines	2	4	2	4	2	4	2	4	2	4
	Number of vertical pixels in effective area	6	4016	6	2008	6	4016	6	2008	6	736
	STATS data					4022	0,1	2014	0,1		
	Frame end	4022	1	2014	1	4022 ~ 4023	1	2014~ 2015	1	742	1

* See Application Note or consult with support window of our sales representative about Horizontal size of HDR.

6-6-4 Description about operation mode

IMX230 has five modes that All-pixel, binning (V:1/2, H:1/2) , binning (V:1/4, H:1/4) and, HDR(Full pixel) and HDR (V:1/2, H:1/2).

6-6-5 Image area control capabilities

As control function for image's viewing area and /or image size, IMX230 has capability of analog crop, digital crop, scaling and output crop. The relation of image output size and the resister is shown below.

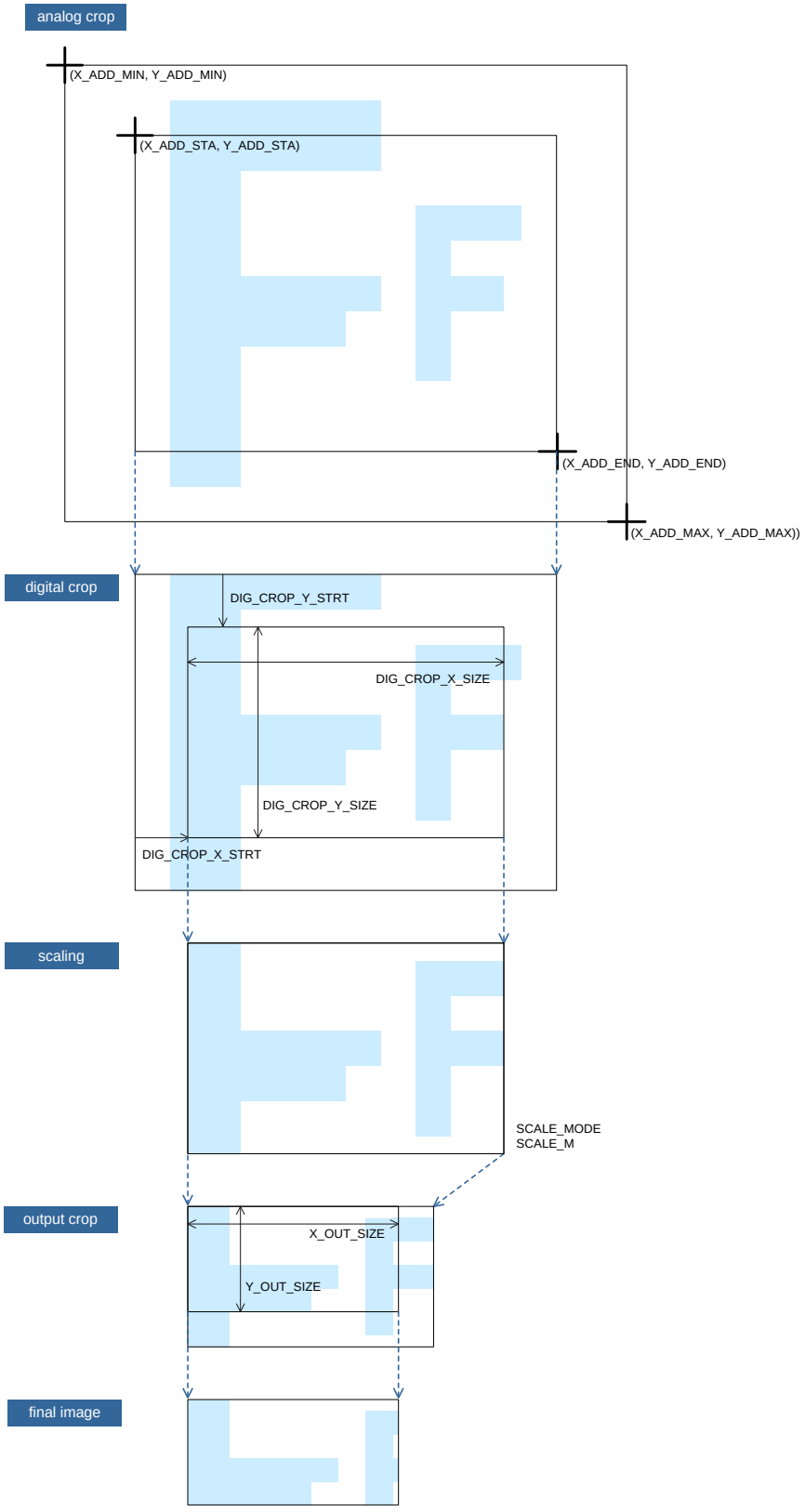


Figure 14 image area control capabilities

Readout Start Position

Default readout position of IMX230 starts from the lower left when PIN1 is placed at the upper right corner. Because the lens will invert the image both vertically and horizontally, the proper image can be archived when PIN1 is placed at the upper right corner.

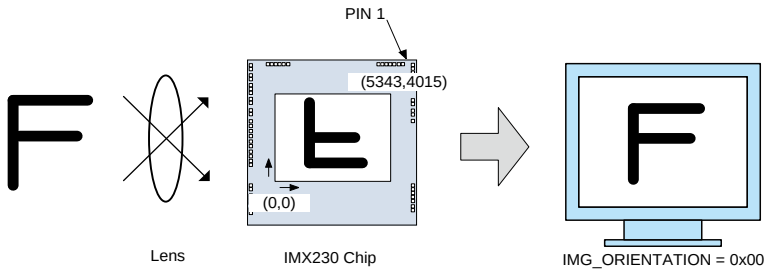


Figure 15 Readout start position

Vertical flip and horizontal mirror readout modes can be specified by the register below. And when readout start and end positions are matching the readout size, the same area is displayed when flipping/mirroring the image. When changing the readout direction, the color of first readout pixel (R/Gr/Gb/B) also changes with it.

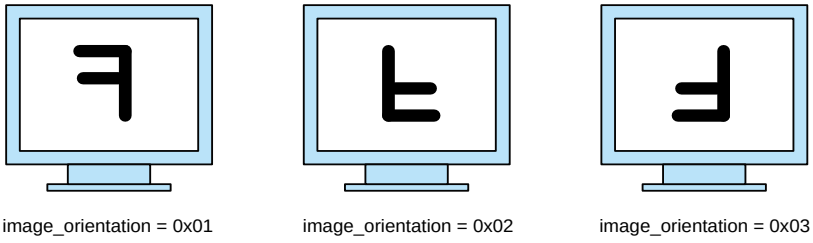


Figure 16 Read out image for each combination of flip and mirror

6-7 Gain setting

IMX230 can apply analog gain on photo-electron signal and digital gain on digital signal after ADC. Range of settable range is as follows.

Table 7 Range of Gains

	Max.
Analog Gain	18dB
Digital Gain	24dB

6-8 Image compensation function

There are some additional functions in sensor image pipeline. Use-case may be chosen in terms of trade-off for power consumption and image quality for example.

See Application Notes for more details of each function.

6-8-1 Defect Pixel Correction

The defect correction function includes static defect correction and dynamic defect correction.

The static defect correction is to correct the defective pixels according to address data stored in OTP. There are two areas; one for Sony's factory area, another for module vendors.
The dynamic defect correction eliminates any critical defects detected on RGB pixel array by estimating from surrounding adjacent pixels value.

6-8-2 Adaptive Tone Reproduction (ATR)

Adaptive Tone Reproduction (ATR) function converts a 14 bit HDR image to a 10 bit range image using adaptive tone curve. It is active in HDR movie operation, HDR still image capture or HDR preview mode.

6-8-3 Chroma Noise Reduction (CNR)

Chroma Noise Reduction (CNR) mainly reduces chroma noise.

6-8-4 Adaptive RAW Noise Reduction(ARNR)

Adaptive RAW Noise Reduction(ARNR) mainly reduces optical shot noise.

6-9 Miscellaneous functions

IMX230 has the following additional functions to be used for various final products' features.

See Application Notes for more details of each function.

6-9-1 Thermal Meter

This function is to measure the thermal data from internal sensor then average it. Measurement results could be read via I2C or EBD data.

6-9-2 Test pattern output and type of test pattern

IMX230 can output the following test pattern by build-in pattern generator.
Test patterns of Solid Color, 100% Color Bar, Fade to Gray Color Bar, PN9 are available.
For Solid Color mode, each value of R, Gr, Gb and B is adjustable.

6-9-3 Long Exposure Setting

IMX230 can achieve a vey long exposure time (up to 128 times of 1 vertical period) by simply expanding the vertical blanking time setting.

6-9-4 OTP (One Time Programmable Read Only Memory)

Total of 9K bit of OTP is available for users. It is divided into 18 pages and 10 pages of them are usable at user's discretion while 18th pare is assigned as the area for defective pixel correction, model ID, and partially write protected. See OTP manual for details.

6-9-5 3D Mode

IMX230 supports synchronized shooting operation of two image sensors by implementing both slave and master mode for each sensor. To enable this feature, master/slave must be set for each sensor by software control method.

6-9-6 Flash light control sequence

IMX230 can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins (FSTROBE).

6-10 Image signal interface

6-10-1 MIPI transmitter

IMX230 outputs image signal by CSI2 high speed serial interface consisted of one pair of clock line and four pairs of data line. See MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) version 1.01.00 and MIPI Alliance Specification for D-PHY version 1.00.00 for details.

Because signal is transmitted by differential pair, impedance (generally 100 Ω) between differential pair near the receiver side during HS mode is required. Otherwise, select receiver with build-in impedance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

7. How to operate IMX230

7-1 Power on Reset

IMX230 has the built in “Power On Reset” function.
It automatically initializes the internal circuits without external intervention as power supplies are brought up with XCLR pin is left OPEN. To control initialization process of internal circuits externally after power on, XCLR shall be kept LOW while power supplies are brought up to skip the power on reset function.
For detail of power on sequence based on the external reset and the power reset, refer to following section of "Power on sequence"

7-2 Power on sequence

7-2-1 Power on slew rate

Maximum slew rate (mV/us) is specified for each power supply to avoid oscillation during power on.

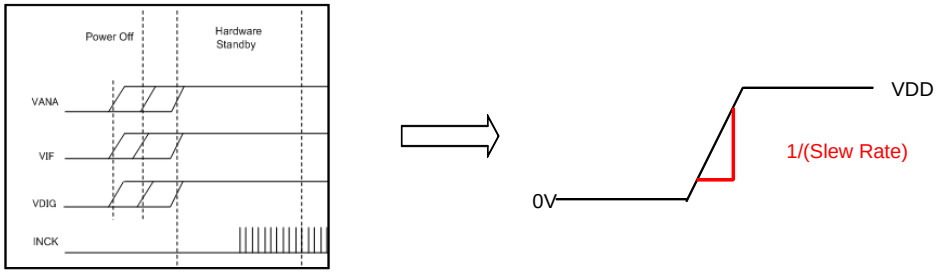


Figure 17 Power on slew rate

Table 8 Limitation on power-on slew rate

Power Supplies	Slew Rate			Comment
	Min	Max	Unit	
VANA, VIF, VDIG		100	mV/µs	

7-2-2 Startup sequence with 2-wire serial communication (external reset)

Follow the power supply start up sequence below.

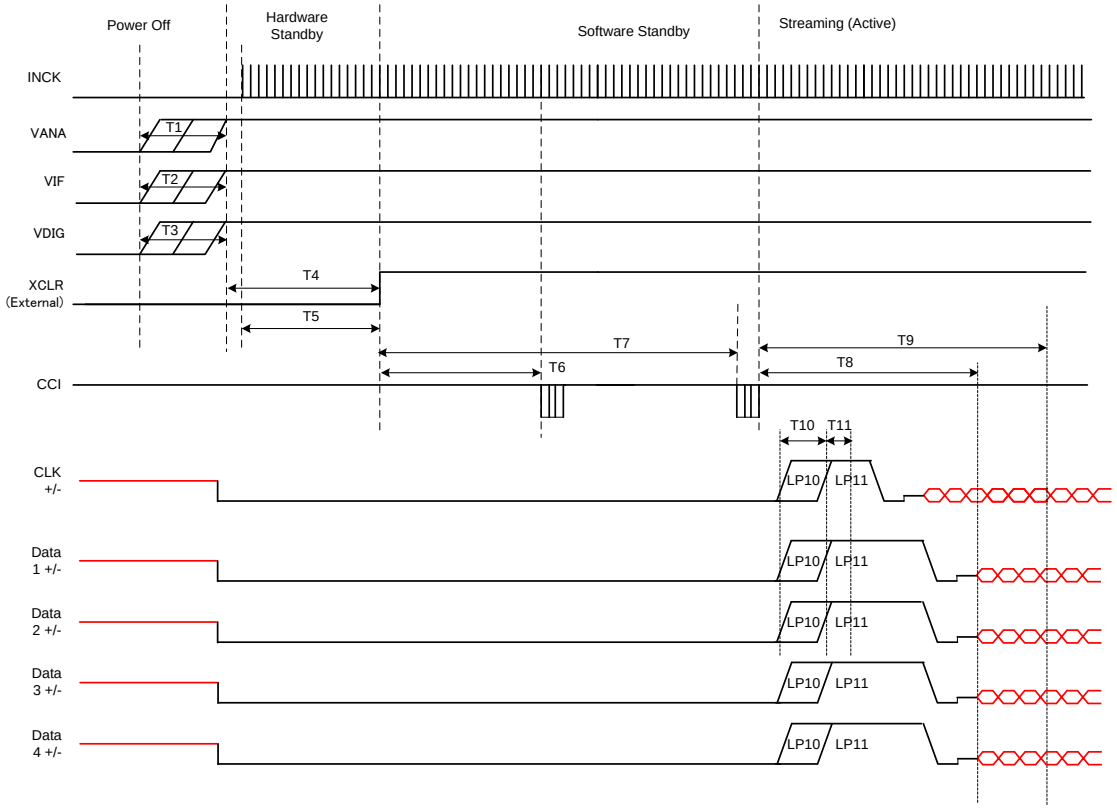


Figure 18 Startup sequence with 2-wire serial communication (external reset)

* Presence of INCK during Power Off is acceptable despite of above chart.

Table 9 Startup sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA ON	T1	VANA and VDIG and VIF may rise in any order.		µs	Slew rate of VANA, VDIG and VIF (0%-100%): Max100 mv/us
VDIG rising – VDIG ON	T2			µs	
VIF rising – VIF ON	T3			µs	
VANA and VDIG and VIF rising– XCLR rising	T4	0		µs	Later of T1, T2, T3
INCK start – XCLR rising	T5	0		ms	
XCLR rising till CCI Read Version ID register wait time	T6	1		ms	
XCLR rising till Send Streaming Command wait time (To complete reading all parameters from NVM)	T7	10.7		ms	28ms(ES1)
Start of first frame after power-on sequence.	T8		5 ms + The delay of the coarse integration time		
Start of first streaming with valid frame after power-on sequence.	T9		T8 + 1Frame	Frames	
DPHY power up	T10	1	1,1	ms	
DPHY init	T11	100	110	µs	

Note) XCLK needs to be Low until all power supplies complete power-on

7-2-3 Startup sequence with 2-wire serial communication (power on reset)

Follow the power supply start up sequence below.

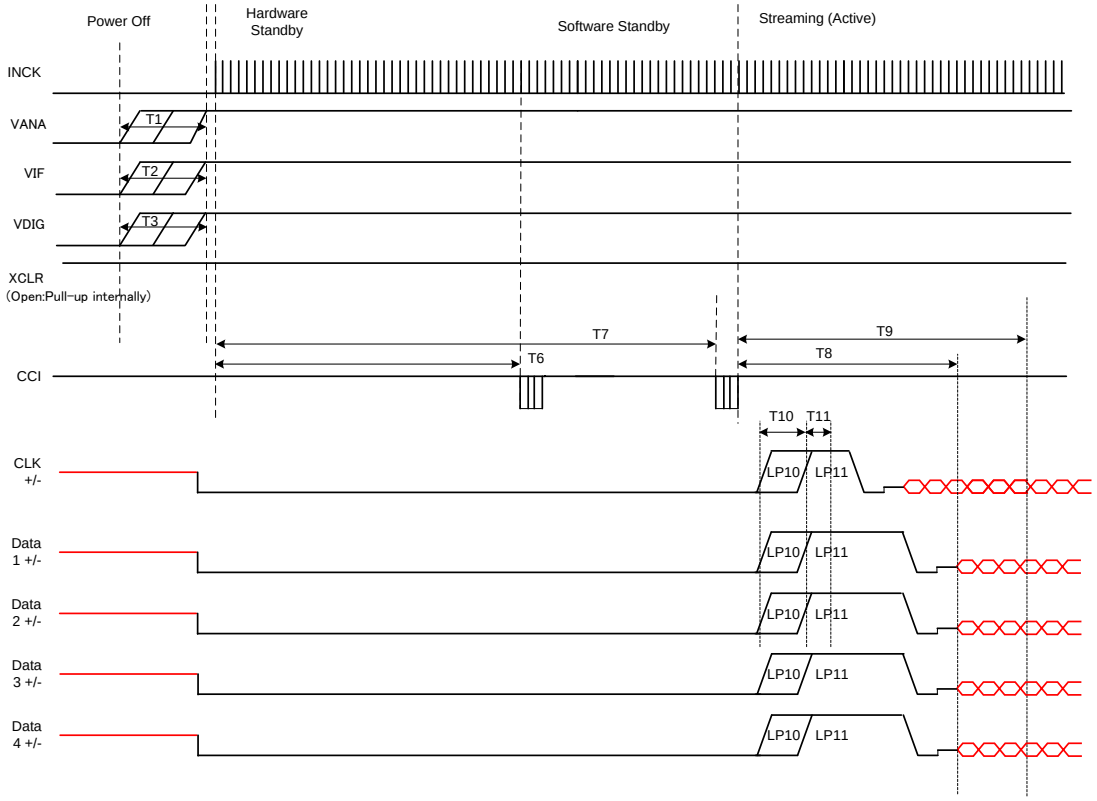


Figure 19 Start up sequence with 2-wire serial communication (power on reset)

Table 10 Startup sequence timing constraints (2-wire serial communication mode with power on reset)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA ON	T1	VANA and VDIG and VIF may rise in any order.		µs	Slew rate of VANA, VDIG and VIF (0%-100%): Max100 mv/us
VDIG rising – VDIG ON	T2			µs	
VIF rising – VIF ON	T3			µs	
VANA and VDIG and VIF rising and INCK start till CCI Read Version ID register wait time	T6	1		ms	
XCLR rising till Send Streaming Command wait time (To complete reading all parameters from NVM)	T7	10.7		ms	28ms(ES1)
Start of first frame after power-on sequence.	T8		5 ms + The delay of the coarse integration time		
Start of first streaming with valid frame after power-on sequence.	T9		T8 + 1Frame	Frames	
DPHY power up	T10	1	1,1	ms	
DPHY init	T11	100	110	µs	

Constrains of XCLR

XCLR must remain low when VIF (IOVDD) is off.

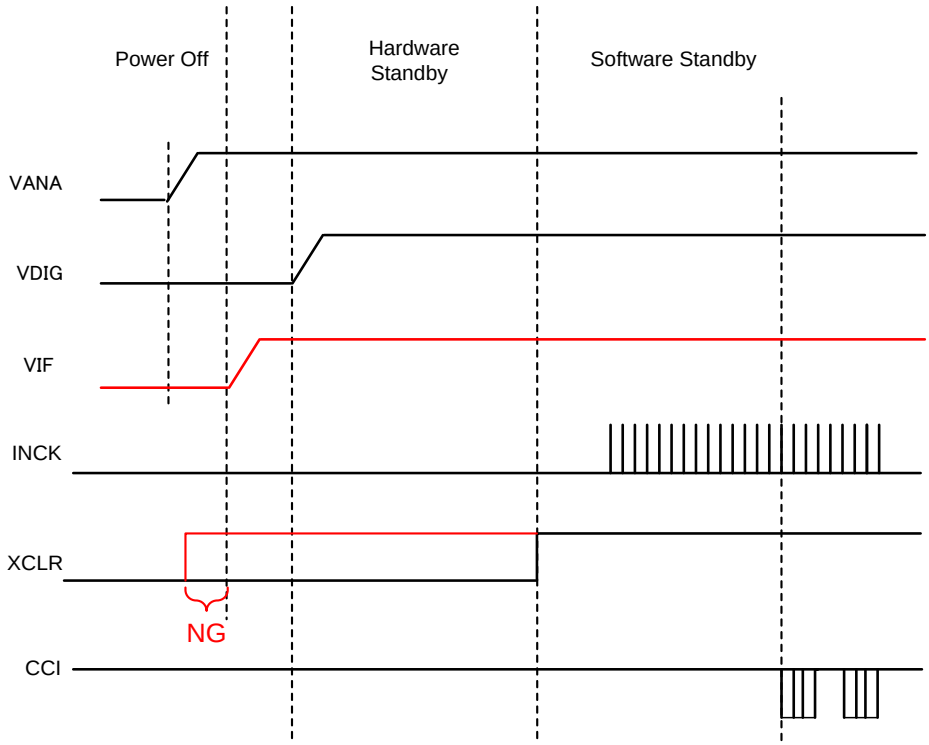


Figure 20 Constrains of XCLR in Start up sequence

※Ignore this constraint if XCLR is not controlled externally (XCLR is open).

7-3 Power down sequence

7-3-1 Power down sequence with 2-wire serial communication (external reset)

Follow the power down sequence below.

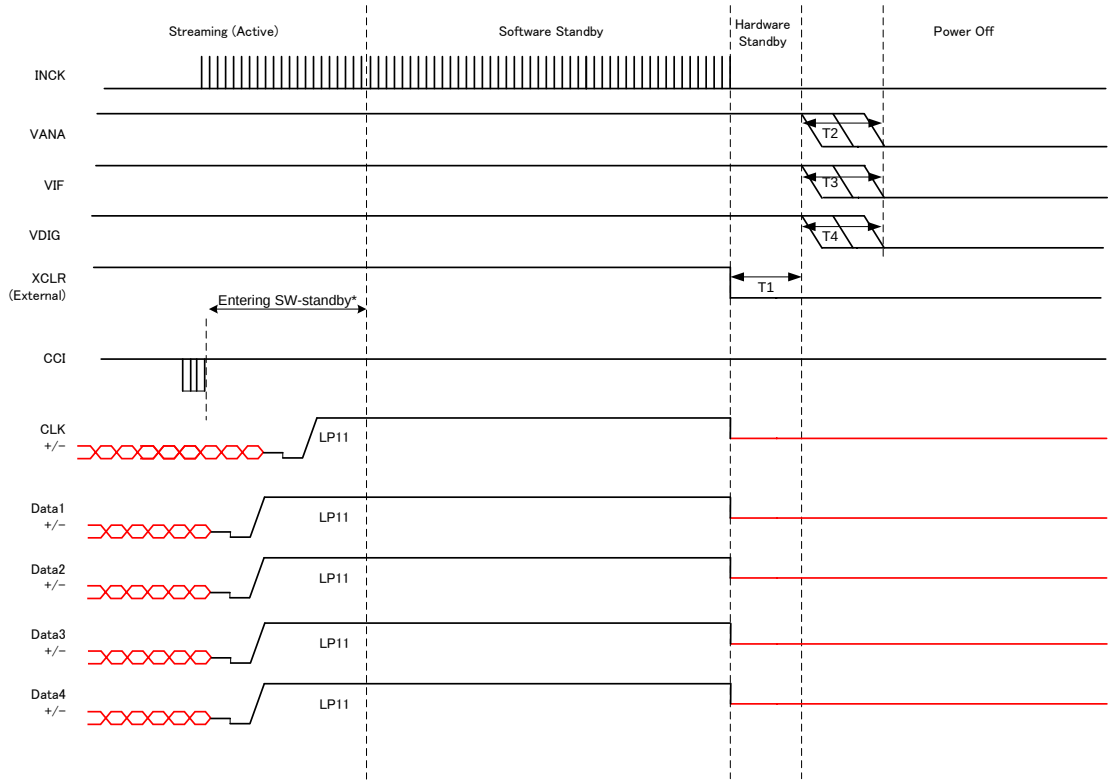


Figure 21 Power down sequence with 2-wire serial communication (external reset)

Table 11 Power down sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
Internal POR negedge - VANA (VDIG or VIF) fall	T1	15		µs	
Sequence free of VANA falling and VDIG falling and VIF falling	T2,T3,T4,T5	VANA and VDIG and VIF may fall in any order.		ns	

7-3-2 Power down sequence with 2-wire serial communication (power on reset)

Follow the power down sequence below.

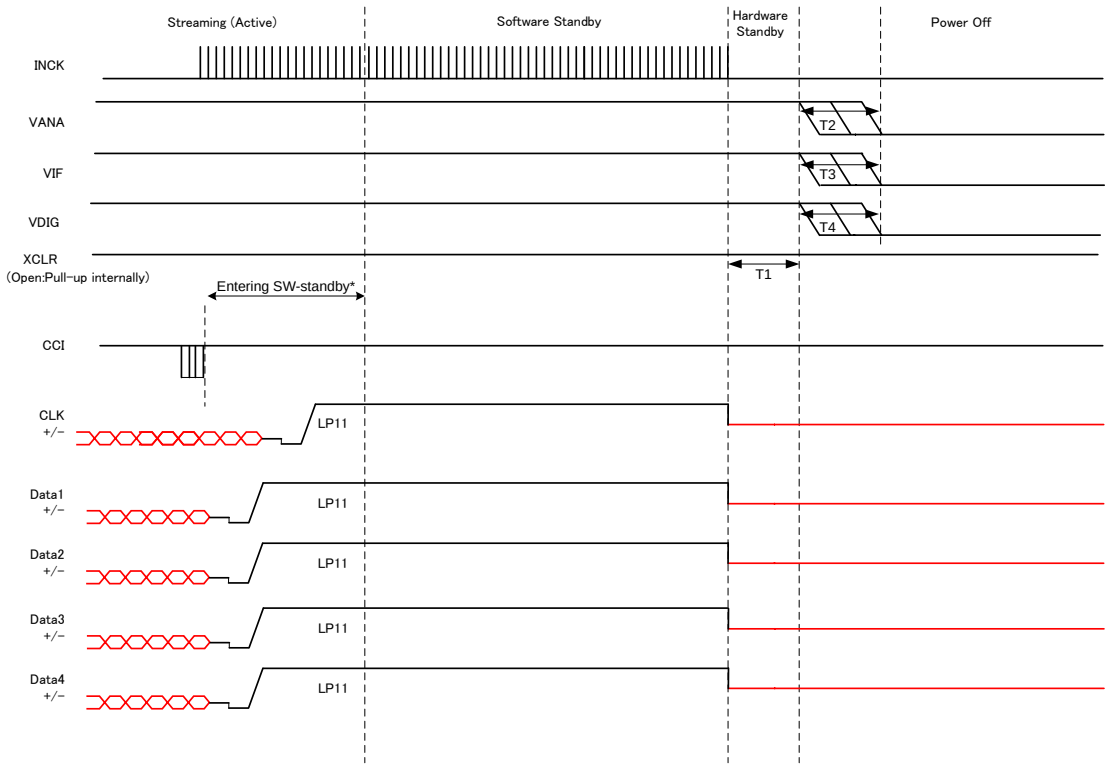


Figure 22 Power down sequence with 2-wire serial communication (power on reset)

Table 12 Power down sequence timing constraints (2-wire serial communication mode with power on reset)

Item	Label	Min.	Max.	Unit	Comment
Internal POR negedge - VANA (VDIG or VIF) fall	T1	15		µs	
Sequence free of VANA falling and VDIG falling and VIF falling	T2,T3,T4,T5	VANA and VDIG and VIF may fall in any order.		ns	

Constrains of XCLR

XCLR must remain low when VIF (IOVDD) is low.

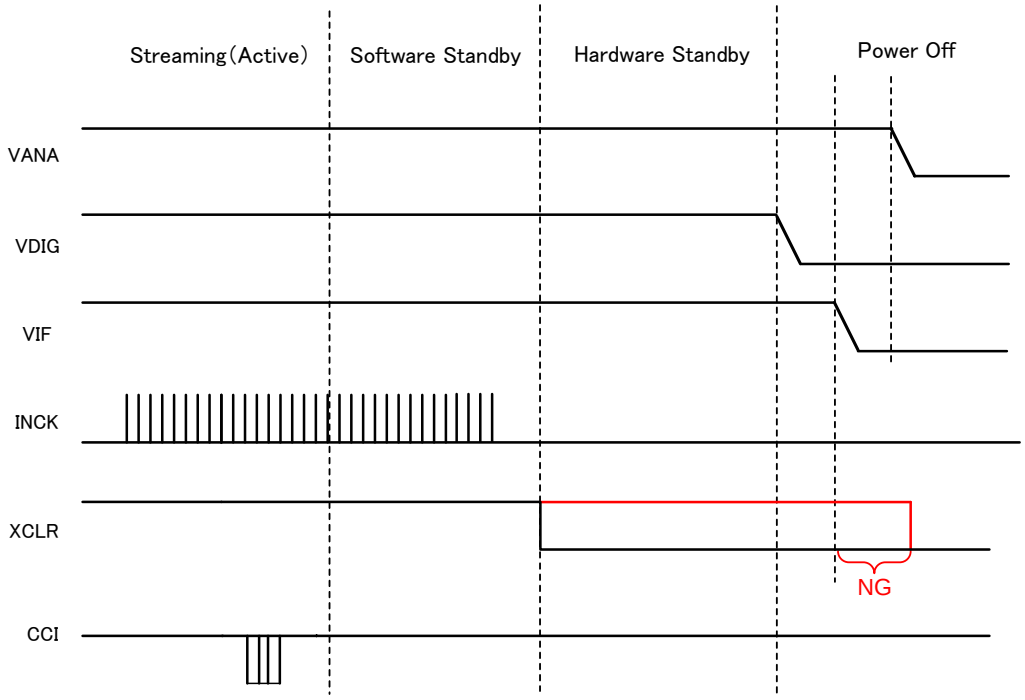


Figure 23　Constrains of XCKR in Power down sequence

※Ignore this constraint if XCLR is not controlled externally (XCLR is open).

7-4　Register Map

See Register Map.

8. Electrical Characteristics

The Electrical Characteristics of the IMX230 is shown below

8-1 DC characteristics

Table 13 DC Characteristics

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VDDSUB VDDHCM1,2 VDDHSN1,2,3,4,5,6 VDDHAN VDDHCP VDDHFIL VDDHCD VDDHVB VDDHVC1A - C VDDHVC2	VANA		2.4	2.5	2.6	V
	VDDLCN1,2 VDDLSC1 - 17 VDDLIO1,2 VDDLPL1,2 VDDLVS1,2	VDIG		1.0	1.1	1.2	V
	VDDMIO1,2,3,4,5,6,7	VIF		1.7	1.8	1.9	V
Digital input voltage	SDA SCL	VIH		0.7VIF		2.9	V
		VIL		-0.3		0.3VIF	V
Digital input voltage	XCLR INCK	VIH		0.65VIF		VIF + 0.3	V
		VIL		-0.3		0.35VIF	V
Digital output voltage	SDA SDO	VOH		VIF-0.4			V
		VOL				0.4	V

8-2 AC Characteristics

8-2-1 Master Clock Waveform Diagram

8-2-1-1 INCK Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK.

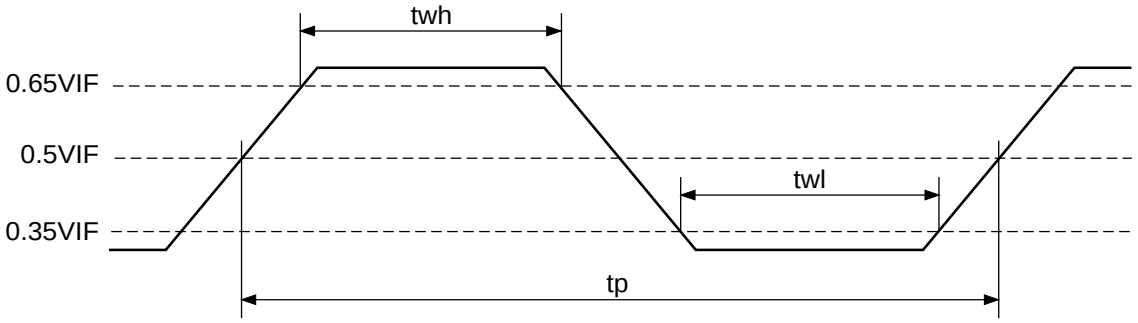


Figure 24 Master Clock Square Waveform Input Diagram

Table 14 Master Clock Square Waveform Input Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{SCK}	6		27	MHz
INCK clock period	t_p	37.0		166.7	ns
INCK low level width	t_{wl}	0.4tp		0.6tp	ns
INCK high level width	t_{wh}	0.4tp		0.6tp	ns
INCK jitter	Tjitter			600	ps

8-2-1-2 INCK Sine Waveform Input Specifications

IMX230 does not support the “AC coupled connection”.
Therefore, there is no description of AC characteristics

8-2-2 PLL block characteristics

Electrical characteristics of PLL block is shown below.

Table 15 PLL block characteristics (VTsystem)

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	6.0		12.0	MHz	
VCO frequency range	400		1200.0	MHz	
Output frequency range	400		1200.0	MHz	
Settling time			1000	μs	

Table 16 PLL block characteristics (OP system)

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	1.0		27.0	MHz	
VCO frequency range	800		3000.0	MHz	
Output frequency range	400		1500.0	MHz	
Settling time			1000	μs	

Conditions) V_{ANA} = 2.5 V, V_{DIG} = 1.1 V, Tj = 25 ˚C, Output frequency = 1200 MHz.

8-2-3 Definition of settling time of PLL block

After start operation, the oscillation frequency of PLL output transits from 0 Hz to target frequency then gradually become stable. The duration for oscillation frequency becomes within 5 % of the target frequency is defined as “settling time”.

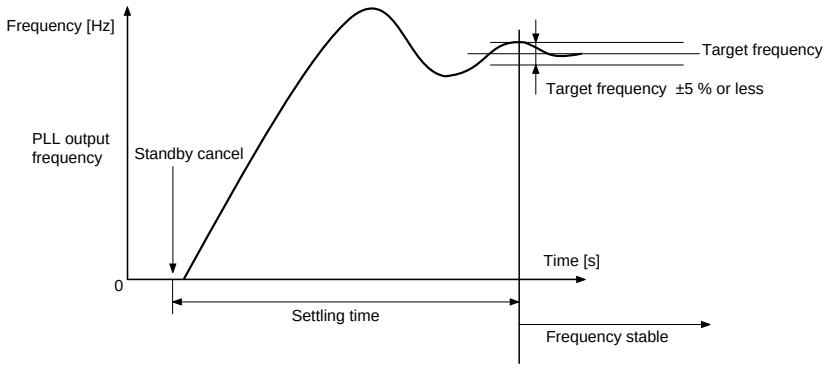


Figure 25 Definition of settling time

8-2-4 2-wire serial communication block characteristics

2-wire serial communication characteristics are shown below.

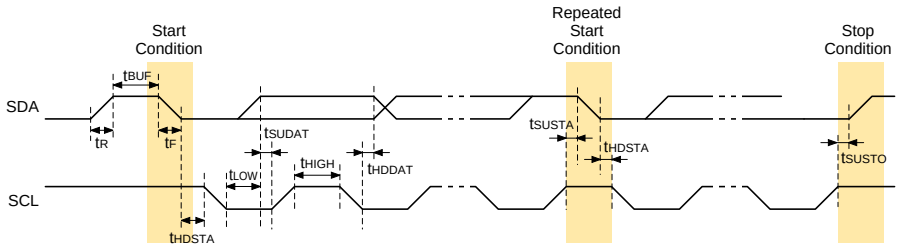


Figure 26 2-wire serial communication block specification

Table 17 2-wire serial communication block specification

Parameter	Symbol	Conditions	Min.	Max.	Unit
Low level input voltage	V_{IL}		-0.3	$0.3V_{IF}$	V
High level input voltage	V_{IH}		$0.7V_{IF}$	2.9	V
Low level output voltage	V_{OL1}	VIF > 2 V, Sink 3 mA	0	0.4	V
	V_{OL2}	VIF < 2 V, Sink 3 mA	0	$0.2V_{IF}$	V
High level output voltage	V_{OH}		V_{IF} - 0.4		V
Output fall time	t_{of}	Load 10 pF – 400 pF, 0.7 VIF→0.3 VIF		250	Ns
Input current	I_I	0.1 VIF→0.9 VIF	-10	10	μA
SDA I/O capacitance	$C_{I/O}$			8	pF
SCL Input capacitance	C_I			6	pF

Table 18 2-wire serial communication block AC specification

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Rise time (SDA and SCL)	t_R	—	300	ns
Fall time (SDA and SCL)	t_F	—	300	ns
Hold time (start condition)	t_{HDSTA}	0.6	—	μs
Setup time (rep.-start condition)	t_{SUSTA}	0.6	—	μs
Setup time (stop condition)	t_{SUSTO}	0.6	—	μs
Data setup time	t_{SUDAT}	100	—	ns
Data hold time	t_{HDDAT}	0	0.9	μs
Bus free time between Stop and Start condition	t_{BUF}	1.3		μs
Low period of the SCL clock	t_{LOW}	1.3		μs
High period of the SCL clock	t_{HIGH}	0.6		μs

8-2-5 Current consumption and standby current

Table 19 Current consumption and standby current

(24 frame/s, V_{ANA} = 2.5 V, V_{DIG} = 1.1 V, V_{IF} = 1.8 V, Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (analog)	I_{ANA}		54.39	54.59	mA	
Current consumption (digital)	I_{DIG}		210.87	230.09	mA	HDR, ARNR, CNR function off
Standby current (analog)	I_{STBANA}			0.06	mA	XCLR : Low fixed INCK :stop
Standby current (digital)	I_{STBDIG}			14.50	mA	XCLR : Low fixed INCK :stop
Standby current (IF)	I_{STBIF}			0.12	mA	XCLR : Low fixed INCK :stop

9. Spectral Sensitivity Characteristic

(Includes neither lens characteristics nor light source characteristics.)

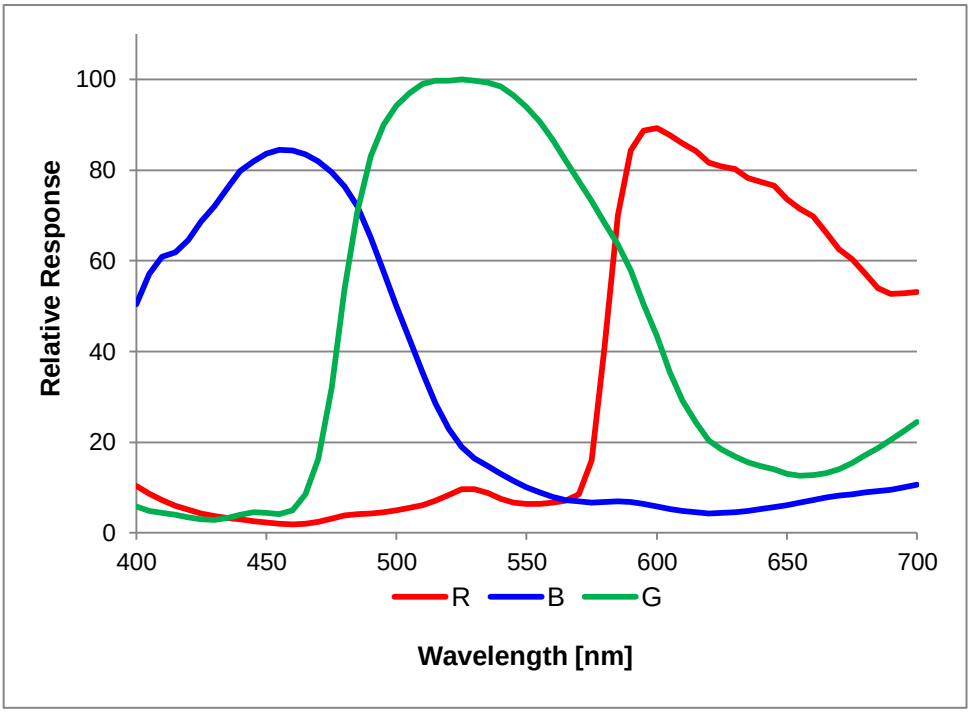


Figure 27 Spectral sensitivity characteristics

10. Image Sensor Characteristics

10-1 Image Sensor Characteristics

Table 20 Image Sensor Characteristics (T.B.D)

(30 frame/s(T.B.D), V_{ANA} = 2.5 V, V_{DIG} = 1.0 V, V_{IF} = 1.8 V,Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Range	Measurement method	Remarks
Sensitivity	S				LSB	Center	1(*)	1/120 s storage
Sensitivity ratio	RG					Center	2(*)	
	BG							
Saturation signal	Vsat				LSB	Zone1	3(*)	
Video signal shading	SH				%	Zone2D	4(*)	Design assurance
Dark signal	Vdt				LSB	Zone2D	5(*)	When operation at 15 frame/s

(*)These refer to the descriptions of the Measurement Methods on Page 43.

LSB is the abbreviation of Least Significant Bit. 10 bits = 1023 digital is the maximum output code for the output unit. The gain setting (base gain setting) in which the saturation signal output matches with 1023 LSB requires 0[dB] when the OB level is 64 LSB (standard recommended value). The data described at this image sensor characteristics are the measurement standard without base gain setting, and indicates the results evaluated with OB as a reference.

10-2 Zone Definition used for specifying image sensor characteristics

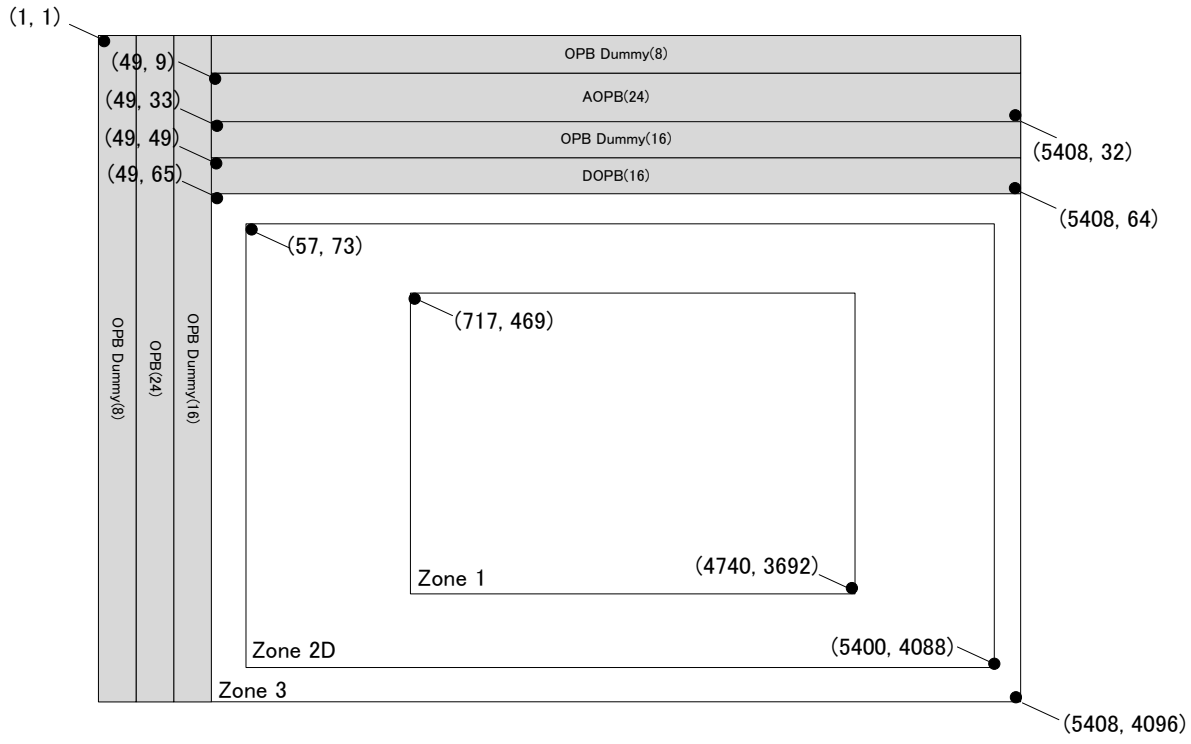


Figure 28 Zone Definition Diagram

11. Measurement Method for Image Sensor Characteristics

11-1 Measurement conditions

The device operation conditions are at the typical values of the bias and clock voltage.

Table 21 Measurement Conditions

Supply voltage	Analog 2.5 V, digital 1.1 V, IF 1.8 V
Clock	INCK 18 MHz

In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr, Gb, R and B digital signal outputs of the measurement system.
As an example of 1 LSB, the typical value is 1 LSB ≈ 0.355 mV(T.B.D) in all-pixel output 10-bit operation mode. The minimum value is 0.327 mV and the maximum value is 0.376 mV.

11-2 Color Coding of This Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.
All pixel signals are output successively in a 1/15 s(T.B.D) period.

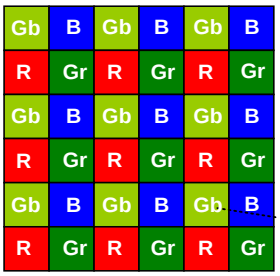


Figure 29 Color coding alignment

11-3 Definition of Standard Imaging Conditions

11-3-1 Standard imaging condition I

Use a pattern box (luminance: 706 cd/m2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

11-3-2 Standard imaging condition II

A testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or storage time control by the electronic shutter.

11-3-3 Standard imaging condition III

A recommended testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output or storage time control by the electronic shutter.

11-4 Measurement method

11-4-1 Sensitivity

Set the measurement condition to the standard imaging condition I. After the electronic shutter mode with a shutter speed of 1/300 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of imaging area, and substitute the values into the following formula.

S = {((VGr + VGb) /2) × (300/120)} [LSB]

11-4-2 Sensitivity ratio

Set the measurement condition to the standard imaging condition II. After adjusting so that the average value of the Gr and Gb signal output is 300 LSB, measure the R signal output (VR [LSB]), the Gr and Gb signal outputs (VGr, VGb [LSB]) and the B signal output (VB [LSB]) at the imaging area Center in frame readout mode, and substitute the values into the following formulas.

VG = (VGr + VGb) /2

RG = VR/VG

RB = VB/VG

11-4-3 Saturation signal

Set the measurement condition to the standard imaging condition II. After adjusting the luminous Intensity to 20 times the intensity with the average value of the Gr, Gb signal outputs, 300 [LSB], measure the average value of the Gr, Gb, R and B signal outputs.

11-4-4 Video signal shading

Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 300 [LSB]. Then measure the maximum value (Gmax [LSB]) and minimum value (Gmin [LSB]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

SH = ((Gmax – Gmin) /Gmax) × 100 [%]

11-4-5 Dark signal

Measure the output difference between 1/15 [s] signal output (Va) and 1/15000 or less [s] signal output (Vb) at the device ambient temperature of 60 ˚C and the device in the light-obstructed state, and calculate the signal output at 1/15 [s] storage by them using the following approximate formula. Then, this is Vdt [LSB].

Vdt = (Va – Vb) × (1/15) / (1/15) – (1/15000) ≈ (Va –Vb) [LSB]

12. Spot Pixel Specification

Table 22 Spot Pixel Specifications

(15 frame/s, VANA = 2.5 V, VDIG = 1.1 V, VIF = 1.8 V, Tj = 60 ˚C)

Type of distortion	Level Note 1)	Maximum distorted pixels in each zone				Measurement method	Remarks
		Zone2D	Zone3	Ineffective OB	Effective OB		
Black or white pixels at high light	30 % ≤ D	65	No evaluation criteria applied			SPS_1	
White pixels in the dark	28 (LSB) ≤ D	975	No evaluation criteria applied			SPS_2	1/30 storage Note 2)

Note) 1. D...Spot pixel level.
2. Continuous same color pixels in the horizontal or vertical direction are NG.
3. Defect pixels are measured with all optional image processing features (DPC, HDR, LNR, CNR) disabled..
4. The maximum quantity pixel counts of 65 for Bright Pixels and 975 for Dark Pixels are total of R + Gr + Gb + B individual pixels from any colour channels.
5. The analog gain for both the Illuminated and Dark defect conditions is 0dB.
6. The above chart (hereinafter referred to as the “White and Black Pixel Specifications”) is the standard only for sorting image sensor products in this specification book (hereinafter referred to as the “PRODUCTS”) before shipment from a manufacturing factory. Sony Corporation and its distributors (collectively hereinafter referred to as the “Seller”) disclaim and will not assume any liability even if actual number of distorted pixels of the PRODUCTS delivered to you exceeds the maximum number set forth in the White and Black Pixel Specifications. You are solely liable for any claim, damage or liability arising from or in connection with such distorted pixels. If the Seller separately has its own product warranty program for the PRODUCTS (the “Program”), the conditions in this specification book shall prevail over the Program and the Seller shall not assume any liability under the Program to the extent there is contradiction.

12-1 Notice on White Pixels Specifications

After shipment inspection of CMOS image sensors, pixels of CMOS image sensors may be distorted and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels.") Cosmic radiation is one of the causes of White Pixels. Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such distorted pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against White Pixels, such as adoption of automatic compensation systems for White Pixels and establishment of quality assurance standards.
White Pixels may be also caused by alpha radiation, which will be emitted in a process of decay of radioactive isotopes which inevitably exist in the air in minute amounts and may exist in materials or parts of CMOS image sensor devices (e.g. packaging materials, seal glass, wiring materials and IC chips). It is recommended that you should use materials or parts which do not include radioactive isotopes, which are sources of alpha radiation, and consider taking measures, such as adoption of vacuum packaging technologies in order to ensure that the PRODUCTS are not exposed to the air. As the density of radioactive isotopes in the air of the underground space may become thicker than that on the ground, it is highly recommended to ensure the PRODUCTS are not exposed to the air in using or storing the PRODUCTS at the underground space.

[For Your Reference] The Annual number of White Pixels Occurrence Caused by Cosmic Radiation
The data in the below chart shows the estimated annual number of White Pixels occurrence caused by cosmic radiation in a single-story building in Tokyo at an altitude of 0 meters. The data shows estimated number of White Pixels based on records of past field tests calculated taking structures and electrical properties of each device into account. However, the data in the chart is for your reference purpose only, and shall not be construed as part of any CMOS image sensor product specifications which the Seller warrants.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 ℃)	Annual number of occurrence
5.6 mV or higher	1.3 pcs
10.0 mV or higher	0.8 pcs
24.0 mV or higher	0.4 pcs
50.0 mV or higher	0.2 pcs
72.0 mV or higher	0.2 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the annual number of White Pixels occurrence.

Note 4) As this data does not take occurrence of White Pixels caused by alpha radiation into account, White Pixels are likely to occur at higher value than the rate set forth in such data.

For Your Reference:
The annual number of White Pixels occurrence caused by cosmic radiation at an altitude of 3,000 meters will be from 5 to 10 times higher than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence caused by cosmic radiation in such areas approximately doubles when compared with that in Tokyo.

12-2 Measurement Method for Spot Pixels

Measure under the standard imaging condition II.

12-3 Spot Pixel Pattern Specifications

12-3-1 SPS_1 Black or white pixels at high light

After adjusting the average value of the Gr/Gb signal output to 367 LSB(T.B.D), measure the local dip point (black pixel at high light, VXB) and peak point (white pixel at high light, VXK) in the Gr/Gb/R/B signal output Vx (x = Gr/Gb/R/B), and substitute the values into the following formula.
The 367LSB does not include the dark level offset of 64. The average value is calculated using the signal level output of Zone 2D.

$$D_K(\text{White Pixel level}) = (V_{XK}/\overline{V_X}) \times 100[\%]$$

$$D_B(\text{Black Pixel level}) = (V_{XB}/\overline{V_X}) \times 100[\%]$$

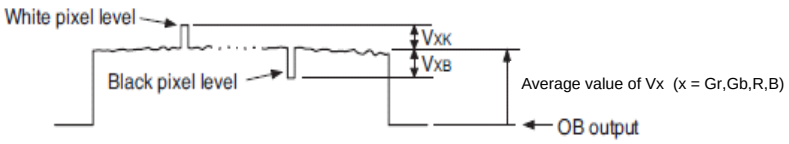


Figure 30 Measurement Method for Spot Pixels

12-3-2 SPS_2 White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

13. CRA Characteristics of Recommended Lens

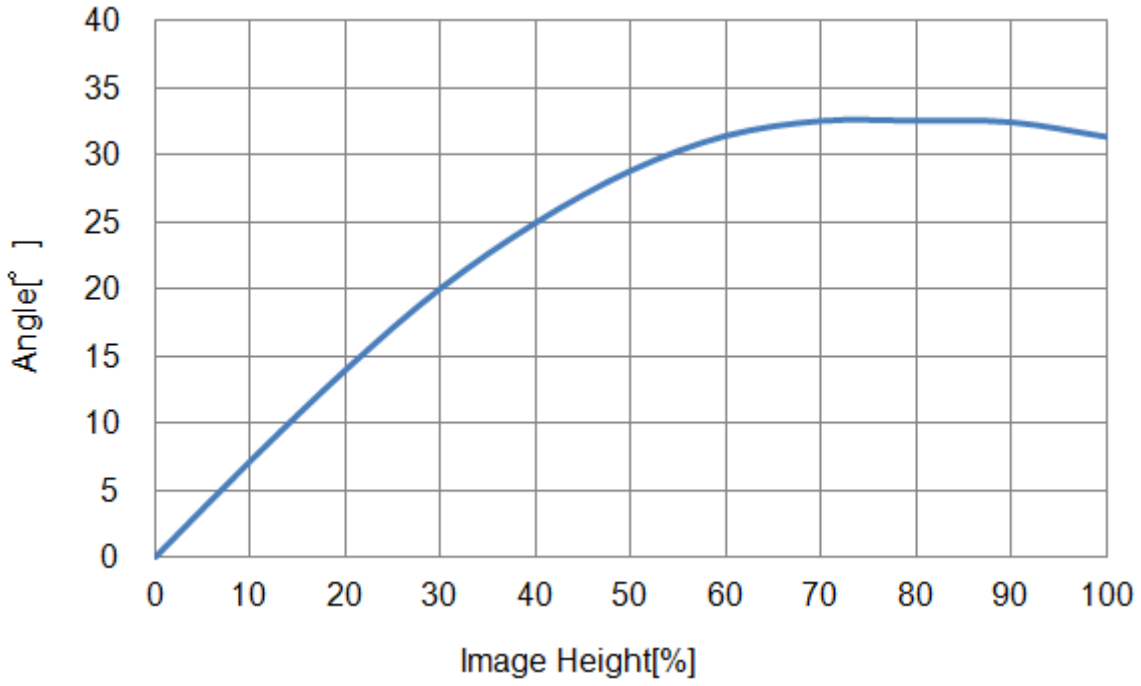


Figure 31 CRA characteristics

14. Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

(1) Perform all work in a clean environment.
(2) Do not touch the chip surface with hand and make any object contact with it.
(3) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

3. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Reliability assurance of this product should be ignored because it is a bare chip.
(5) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(6) Note that X-ray inspection may damage characteristics of the sensor.
(7) Note that the sensor may be damaged when using ultraviolet ray and infrared ray on mounting it.
(8) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

15. Notes on Handling (Additional items concerning bare chip mounting of stacked-type CMOS image sensors)

Collet contact is allowed in areas other than the pixel area, bonding pads, scribe area, and chip edge. Contact with areas other than the contact-allowed area may result in problems such as dust emission or electrostatic breakdown.

Collet contact-prohibited areas

- Pixel area: Abnormal images
- Bonding pad: Circuit electrostatic breakdown
  (Please note that this rule is not applicable for electrostatic breakdown prevention areas.)
- Scribe area: Dust emission due to chipping
- Chip edge: Dust emission due to chip breakage

Note: Ensure sufficient positional accuracy during the pickup work.
Separate the collet contact surfaces and contact-prohibited areas as much as possible.

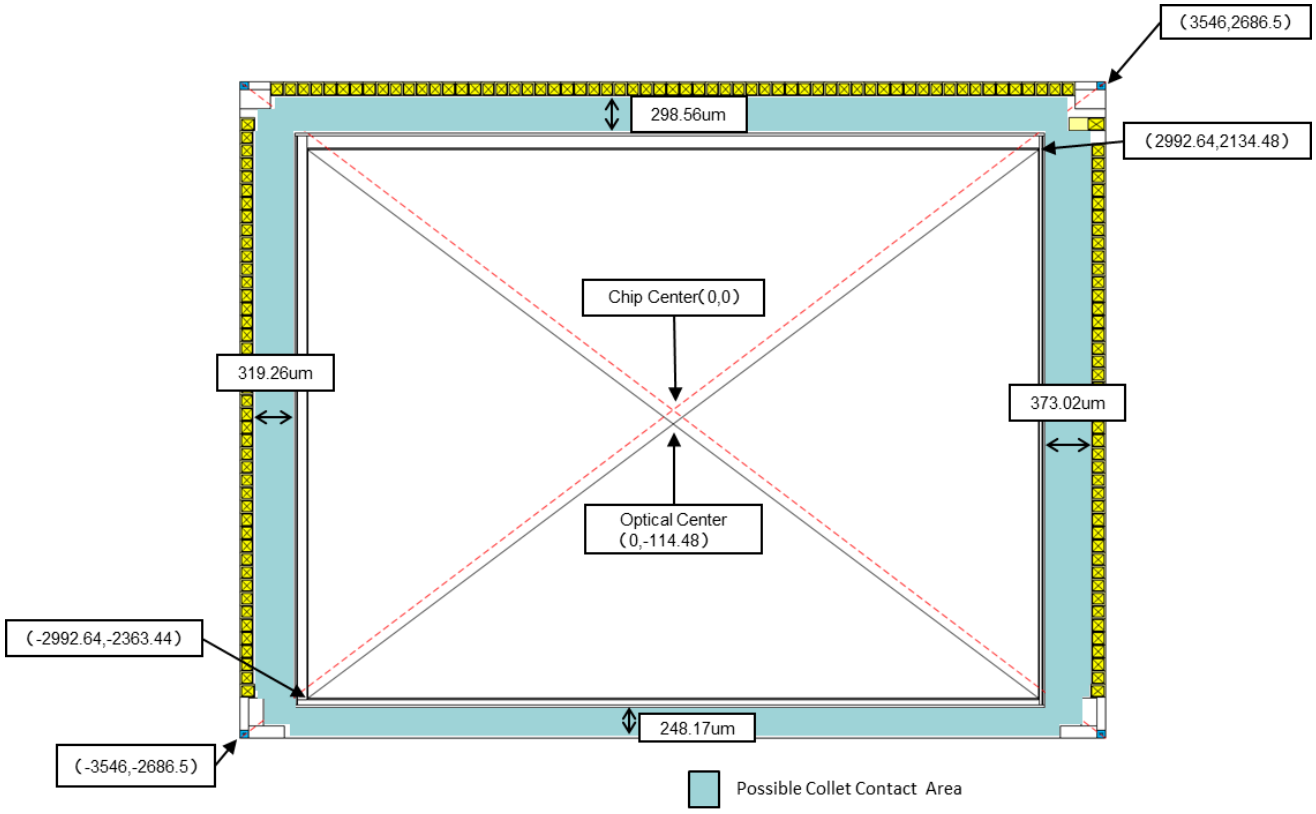


Figure 32 Prohibited Area

Ultrasonic chip clearing is prohibited.
This may result in dust emission from cut surfaces.