

LP5900 Ultra Low-Noise, 150-mA Linear Regulator for RF/Analog Circuits - Requires No Bypass Capacitor

1 Features

- Input Voltage Range, 2.5 V to 5.5 V
- Output Voltage Range, 1.5 V to 4.5 V
- Stable with 0.47- μ F Ceramic Input and Output Capacitors
- No Noise Bypass Capacitor Required
- Logic Controlled Enable
- Thermal-Overload and Short-Circuit Protection
- -40°C to 125°C Junction Temperature Range for Operation
- Output Current, 150 mA
- Low Output Voltage Noise, 6.5 μV_{RMS}
- PSRR, 75 dB at 1 kHz
- Output Voltage Tolerance, $\pm 2\%$
- Virtually Zero I_{Q} (Disabled), $< 1 \mu\text{A}$
- Very Low I_{Q} (Enabled), 25 μA
- Start-up Time, 150 μs
- Low Dropout, 80 mV Typ.

2 Applications

- Cellular Phones
- PDA Handsets
- Wireless LAN Devices

3 Description

The LP5900 is a linear regulator capable of supplying 150-mA output current. Designed to meet the requirements of RF/Analog circuits, the LP5900 device provides low noise, high PSRR, low quiescent current, and low line transient response figures. Using new innovative design techniques the LP5900 offers class-leading device noise performance without a noise bypass capacitor.

The device is designed to work with 0.47- μF input and output ceramic capacitors (no bypass capacitor required).

The device is available in a DSBGA (YZR) package and a WSON package; also available in an extremely thin DSBGA (YPF) package. For all other package options, contact your local Texas Instruments sales office.

This device is available with 1.5-V, 1.575-V, 1.8-V, 1.9-V, 2-V, 2.1-V, 2.2-V, 2.3-V, 2.5-V, 2.6-V, 2.65-V, 2.7-V, 2.75-V, 2.8-V, 2.85-V, 3-V, 3.3-V and 4.5-V outputs. Please contact your local sales office for any other voltage options.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE |
|-------------|-----------|---------------------------|
| LP5900 | DSBGA (4) | 1.108 mm x 1.083 mm (MAX) |
| | WSON (6) | 2.50 mm x 2.20 mm (NOM) |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

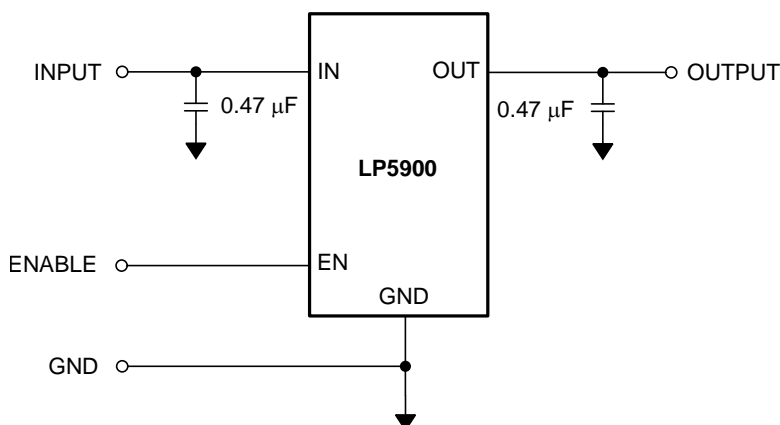


Table of Contents

| | | | |
|--|-----------|--|-----------|
| 1 Features | 1 | 7.4 Device Functional Modes..... | 11 |
| 2 Applications | 1 | 8 Application and Implementation | 12 |
| 3 Description | 1 | 8.1 Application Information..... | 12 |
| 4 Revision History | 2 | 8.2 Typical Application | 12 |
| 5 Pin Configuration and Functions | 3 | 9 Power Supply Recommendations | 14 |
| 6 Specifications | 4 | 10 Layout | 15 |
| 6.1 Absolute Maximum Ratings | 4 | 10.1 Layout Guidelines | 15 |
| 6.2 ESD Ratings..... | 4 | 10.2 Layout Examples..... | 15 |
| 6.3 Recommended Operating Conditions..... | 4 | 10.3 DSBGA Mounting..... | 15 |
| 6.4 Thermal Information | 4 | 10.4 DSBGA Light Sensitivity | 16 |
| 6.5 Electrical Characteristics..... | 5 | 10.5 WSON Mounting | 16 |
| 6.6 Output and Input Capacitor, Recommended Specifications | 6 | 11 Device and Documentation Support | 17 |
| 6.7 Typical Characteristics | 7 | 11.1 Documentation Support | 17 |
| 7 Detailed Description | 10 | 11.2 Trademarks | 17 |
| 7.1 Overview | 10 | 11.3 Electrostatic Discharge Caution..... | 17 |
| 7.2 Functional Block Diagram | 10 | 11.4 Glossary | 17 |
| 7.3 Feature Description..... | 10 | 12 Mechanical, Packaging, and Orderable Information | 17 |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

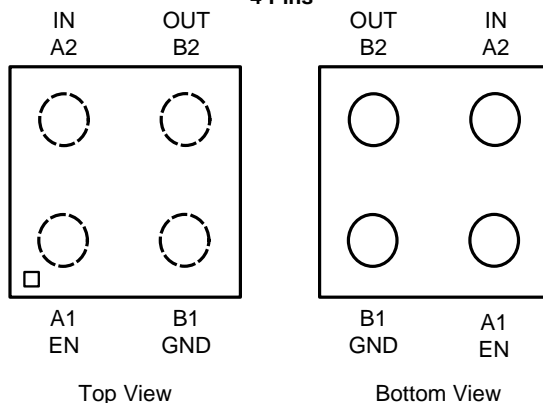
| Changes from Revision P (December 2014) to Revision Q | Page |
|--|-----------|
| • Added NC and Thermal Pad descriptions in <i>Pin Functions</i> | 3 |
| • Changed <i>Handling Ratings</i> to <i>ESD Ratings</i> table format; move storage temp spec to Ab Max; delete soldering info (in POA) | 4 |
| • Changed Unit for Line and Load regulation | 5 |
| • Changed I_I to I_{out} | 7 |
| • Changed I_I to I_{out} | 8 |
| • Changed I_I to I_{out} | 9 |
| • Added <i>WSON Mounting</i> subsection | 16 |
| • Added another related doc link | 17 |

| Changes from Revision O (April 2013) to Revision P | Page |
|--|----------|
| • Added <i>Pin Configuration and Functions</i> section, <i>Handling Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section; updated pin names and thermal information | 1 |

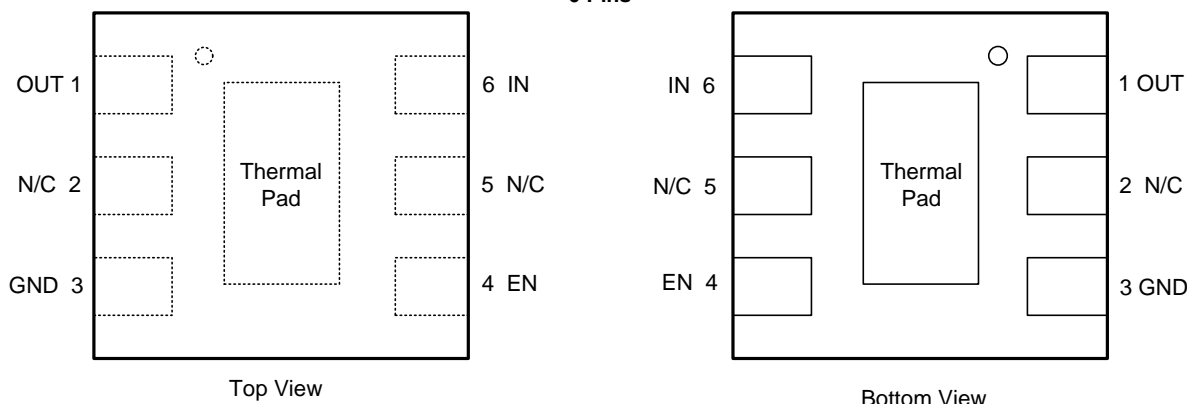
| Changes from Revision N (April 2013) to Revision O | Page |
|--|-----------|
| • Changed layout of National Data Sheet to TI format | 16 |

5 Pin Configuration and Functions

DSBGA (YZR and YPF) Packages
4 Pins



WSON Package with Exposed Thermal Pad (NGF)
6 Pins



Pin Functions

| PIN | | NAME | TYPE | DESCRIPTION |
|-------|-------------|-------------|------|---|
| DSBGA | WSON | | | |
| A1 | 4 | EN | I | Enable input; disables the regulator when ≤ 0.4 V. Enables the regulator when ≥ 1.2 V. An internal 1-M Ω pull-down resistor connects this input to ground. |
| A2 | 6 | IN | I | Input voltage supply. A 0.47- μ F capacitor should be connected at this input. |
| B1 | 3 | GND | — | Common ground |
| B2 | 1 | OUT | O | Output voltage. A 0.47- μ F Low ESR capacitor should be connected to this Pin. Connect this output to the load circuit. |
| — | 2 | NC | — | No internal connection. |
| — | Thermal Pad | Thermal Pad | — | The exposed thermal pad on the bottom of the package should be connected to a copper area on the PCB under the package. The use of thermal vias to remove heat from the package into the PCB is recommended. Connect the thermal pad to ground potential or leave floating. Do not connect the thermal pad to any potential other than the same ground potential seen at device pin 3. For additional information on using TI's Non Pull Back WSON package, see Application Note AN-1187 (SNOA401). |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

| | MIN | MAX | UNIT |
|---|--------------------|-----------------------|------|
| V _{IN} : Input voltage | –0.3 | 6 | V |
| V _{OUT} : Output voltage | –0.3 | V _{IN} + 0.3 | |
| V _{EN} : Enable input voltage | –0.3 | V _{IN} + 0.3 | |
| Continuous power dissipation ⁽⁴⁾ | Internally Limited | | |
| T _{JMAX} : junction temperature | | 150 | °C |
| T _{stg} : Storage temperature | –65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

| | VALUE | UNIT |
|--|-------|------|
| V _(ESD) Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|--|-----|-----------------------|------|
| V _{IN} : Input voltage | 2.5 | 5.5 | V |
| V _{EN} : Enable voltage | 0 | V _{IN} + 0.3 | V |
| I _{OUT} : Output current ⁽²⁾ | 0 | 150 | mA |
| Junction temperature(T _J) | –40 | 125 | °C |
| Ambient temperature (T _A) ⁽²⁾ | –40 | 85 | °C |

- (1) All voltages are with respect to the potential at the GND pin.
- (2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} – (R_{θJA} × P_{D-MAX}). See [Application and Implementation](#).

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LP5900 | | UNIT |
|-------------------------------|--|--------|---------|------|
| | | NGF | YZR/YPF | |
| | | 6 PINS | 4 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 79.8 | 177.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 84.4 | 0.7 | |
| R _{θJB} | Junction-to-board thermal resistance | 20.4 | 35.6 | |
| ψ _{JT} | Junction-to-top characterization parameter | 2.6 | 5.8 | |
| ψ _{JB} | Junction-to-board characterization parameter | 20.3 | 35.3 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 11.2 | — | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Unless otherwise noted, specifications apply in [Figure 16](#) with: $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $V_{EN} = 1.2\text{ V}$, $C_{IN} = C_{OUT} = 0.47\text{ }\mu\text{F}$, $I_{OUT} = 1\text{ mA}$.⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------------|---|---|---------------------------|-----|-------|-----|-------------------|
| V _{IN} | Input voltage | | | 2.5 | | 5.5 | V |
| ΔV _{OUT} | Output voltage tolerance | V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA to 150 mA, −40°C ≤ T _J ≤ 125°C | | −2% | | 2% | |
| | Line regulation | V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA | | | 0.05 | | %V |
| | Load regulation | I _{OUT} = 1 mA to 150 mA | | | 0.001 | | %mA |
| I _{LOAD} | Load current | See ⁽³⁾ | | | | | mA |
| | Maximum output current | −40°C ≤ T _J ≤ 125°C | | | | 150 | |
| I _Q | Quiescent current ⁽⁴⁾ | V _{EN} = 1.2 V, I _{OUT} = 0 mA | | | 25 | | μA |
| | | V _{EN} = 1.2 V, I _{OUT} = 0 mA, −40°C ≤ T _J ≤ 125°C | | | | 50 | |
| | | V _{EN} = 1.2 V, I _{OUT} = 150 mA | | | 160 | | |
| | | V _{EN} = 1.2 V, I _{OUT} = 150 mA, −40°C ≤ T _J ≤ 125°C | | | | 230 | |
| | | V _{EN} = 0.3 V (disabled) | | | 0.003 | | |
| | | V _{EN} = 0.3 V (disabled, −40°C ≤ T _J ≤ 125°C | | | | 1 | |
| I _G | Ground current ⁽⁵⁾ | I _{OUT} = 0 mA (V _{OUT} = 2.5 V) | | | 30 | | μA |
| V _{DO} | Dropout voltage ⁽⁶⁾ | I _{OUT} = 150 mA | | | 80 | | mV |
| | | I _{OUT} = 150 mA, −40°C ≤ T _J ≤ 125°C | | | | 150 | |
| I _{SC} | Short-circuit current limit ⁽⁷⁾ | | | | 300 | | mA |
| PSRR | Power supply rejection ratio ⁽⁸⁾ | f = 100 Hz, I _{OUT} = 150 mA | | | 85 | | dB |
| | | f = 1 kHz, I _{OUT} = 150 mA | | | 75 | | |
| | | f = 10 kHz, I _{OUT} = 150 mA | | | 65 | | |
| | | f = 50 kHz, I _{OUT} = 150 mA | | | 52 | | |
| | | f = 100 kHz, I _{OUT} = 150 mA | | | 40 | | |
| e _n | Output noise voltage ⁽⁸⁾ | BW = 10 Hz to 100 kHz, V _{IN} = 4.2 V | I _{OUT} = 0 mA | | 7 | | μV _{RMS} |
| | | | I _{OUT} = 1 mA | | 10 | | |
| | | | I _{OUT} = 150 mA | | 6.5 | | |
| T _{SHUTDOWN} | Thermal shutdown | Temperature | | | 160 | | °C |
| | | Hysteresis | | | 20 | | |
| LOGIN INPUT THRESHOLDS | | | | | | | |
| V _{IL} | Low input threshold (V _{EN}) | V _{IN} = 2.5 V to 5.5 V, −40°C ≤ T _J ≤ 125°C | | | | 0.4 | V |
| V _{IH} | High input threshold (V _{EN}) | V _{IN} = 2.5 V to 5.5 V, −40°C ≤ T _J ≤ 125°C | | 1.2 | | | V |
| I _{EN} | Input current at EN pin ⁽⁹⁾ | V _{EN} = 5.5 V and V _{IN} = 5.5 V | | | 5.5 | | μA |
| | | V _{EN} = 0 V and V _{IN} = 5.5 V | | | 0.001 | | |

(1) All voltages are with respect to the potential at the GND pin.

(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.

(3) The device maintains a stable, regulated output voltage without a load current.

(4) Quiescent current is defined here as the difference in current between the input voltage source and the load at the OUT pin.

(5) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.

(6) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value. This parameter only applies to output voltages above 2.5 V.

(7) Short Circuit Current is measured with OUT pulled to 0 V and IN worst case = 6 V.

(8) This specification is specified by design.

(9) There is a 1-M Ω resistor between EN pin and ground on the device.

Electrical Characteristics (continued)

Unless otherwise noted, specifications apply in [Figure 16](#) with: $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $V_{EN} = 1.2\text{ V}$, $C_{IN} = C_{OUT} = 0.47\text{ }\mu\text{F}$, $I_{OUT} = 1\text{ mA}$.⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|--------------------------------------|--|------|-----|-----|---------------|
| TRANSIENT CHARACTERISTICS | | | | | | |
| ΔV_{OUT} | Line transient ⁽⁸⁾ | $V_{IN} = (V_{OUT(NOM)} + 1\text{ V})$ to $(V_{OUT(NOM)} + 1.6\text{ V})$ in $30\text{ }\mu\text{s}$, $I_{OUT} = 1\text{ mA}$, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ | -2 | | | mV |
| | | $V_{IN} = (V_{OUT(NOM)} + 1.6\text{ V})$ to $(V_{OUT(NOM)} + 1\text{ V})$ in $30\text{ }\mu\text{s}$, $I_{OUT} = 1\text{ mA}$, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ | | 2 | | |
| | Load transient ⁽⁸⁾ | $I_{OUT} = 1\text{ mA}$ to 150 mA in $10\text{ }\mu\text{s}$, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ | -110 | | | mV |
| | | $I_{OUT} = 150\text{ mA}$ to 1 mA in $10\text{ }\mu\text{s}$, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ | | 50 | | |
| | Overshoot on start-up ⁽⁸⁾ | $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ | | 20 | | mV |
| Turnon time | | To 95% of $V_{OUT(NOM)}$ | | 150 | 300 | μs |

6.6 Output and Input Capacitor, Recommended Specifications⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|------------------|--------------------------|---|------|-----|-----|------|
| C _{IN} | Input capacitance | Capacitance for stability | 0.47 | | | μF |
| | | Capacitance for stability, −40°C ≤ T _J ≤ 125°C | 0.33 | | | |
| C _{OUT} | Output capacitance | Capacitance for stability | 0.47 | | 10 | |
| | | Capacitance for stability, −40°C ≤ T _J ≤ 125°C | 0.33 | | | |
| ESR | Output/Input capacitance | | 5 | | 500 | mΩ |

- (1) The minimum capacitance should be greater than $0.33\text{ }\mu\text{F}$ over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.

6.7 Typical Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 0.47 \mu F$, $V_{IN} = V_{OUT(NOM)} + 1 V$, $V_{EN} = 1.2 V$, $I_{OUT} = 1 mA$, $T_A = 25^\circ C$.

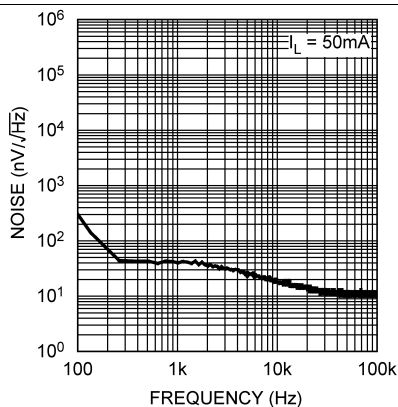


Figure 1. Output Noise Density

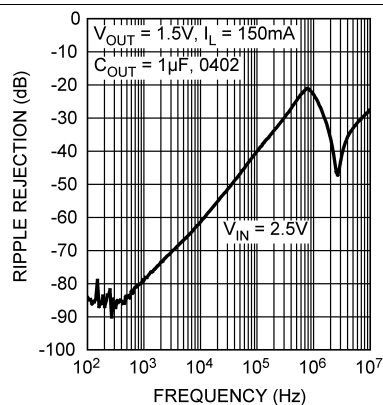


Figure 2. Power Supply Rejection Ratio

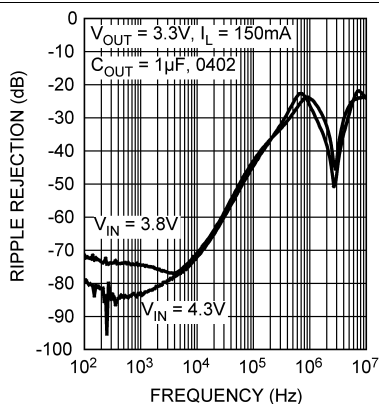


Figure 3. Power Supply Rejection Ratio

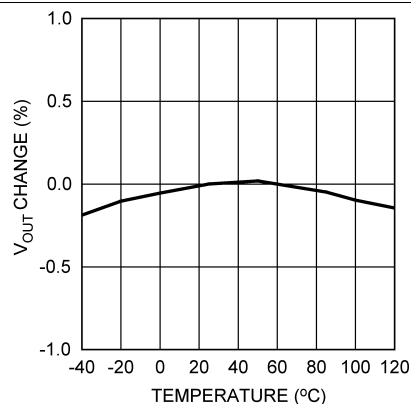


Figure 4. Output Voltage Change vs Temperature

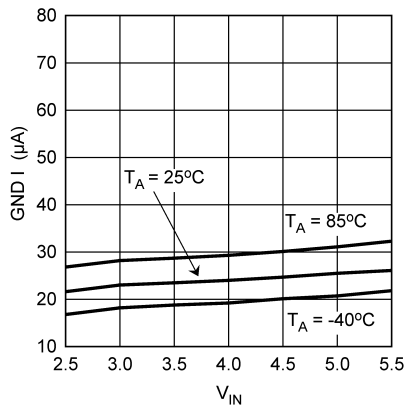


Figure 5. Ground Current vs V_{IN} , $I_{LOAD} = 0 mA$

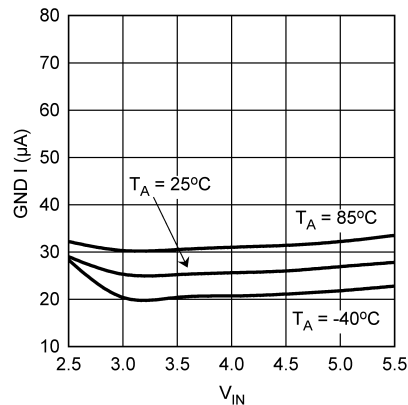


Figure 6. Ground Current vs V_{IN} , $I_{LOAD} = 1 mA$

Typical Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 0.47 \mu F$, $V_{IN} = V_{OUT(NOM)} + 1 V$, $V_{EN} = 1.2 V$, $I_{OUT} = 1 mA$, $T_A = 25^\circ C$.

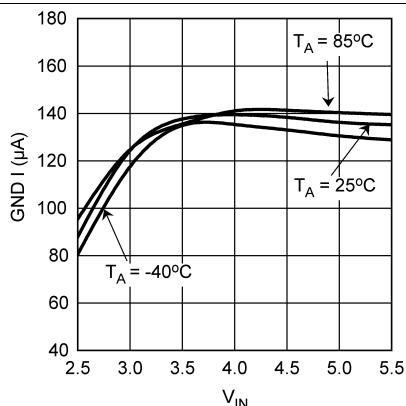


Figure 7. Ground Current vs V_{IN} , $I_{LOAD} = 100 mA$

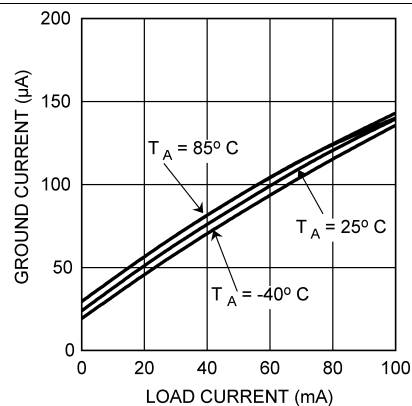


Figure 8. Ground Current vs Load Current

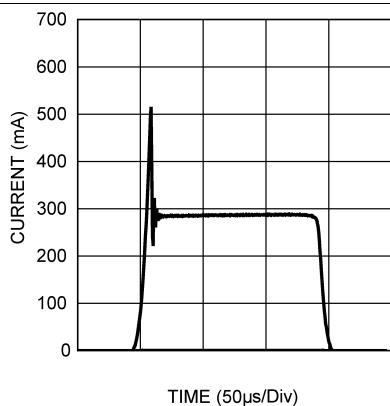


Figure 9. Short-Circuit Current

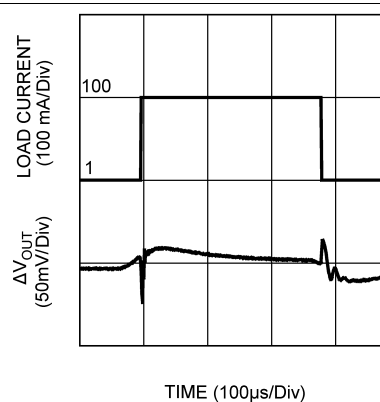


Figure 10. Load Transient

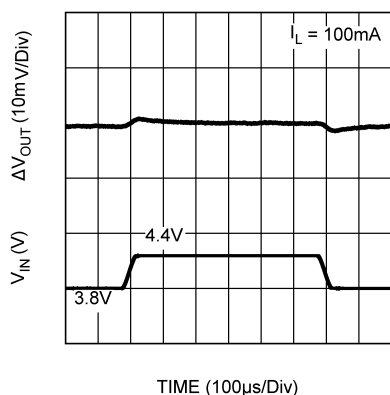


Figure 11. Line Transient

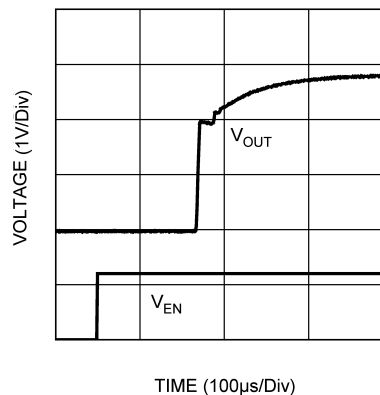


Figure 12. Enable Start-up Time, ($I_{OUT} = 1 mA$, $V_{OUT} = 2.8 V$)

Typical Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 0.47 \mu F$, $V_{IN} = V_{OUT(NOM)} + 1 V$, $V_{EN} = 1.2 V$, $I_{OUT} = 1 mA$, $T_A = 25^\circ C$.

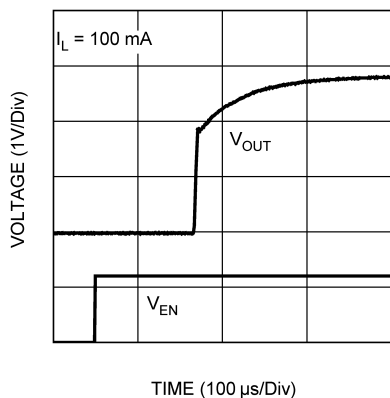


Figure 13. Enable Start-up Time, ($I_{OUT} = 100 mA$, $V_{OUT} = 2.8 V$)

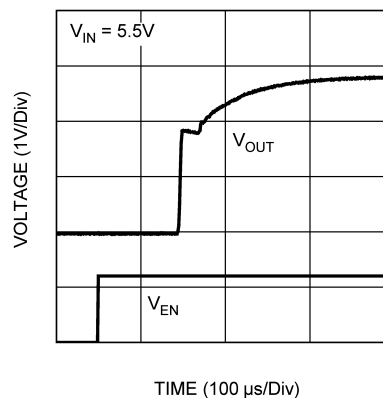


Figure 14. Enable Start-up Time, ($I_{OUT} = 1 mA$, $V_{OUT} = 2.8 V$)

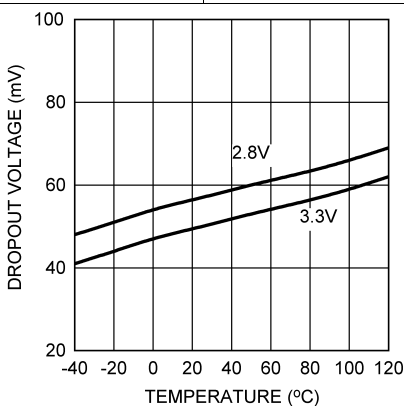


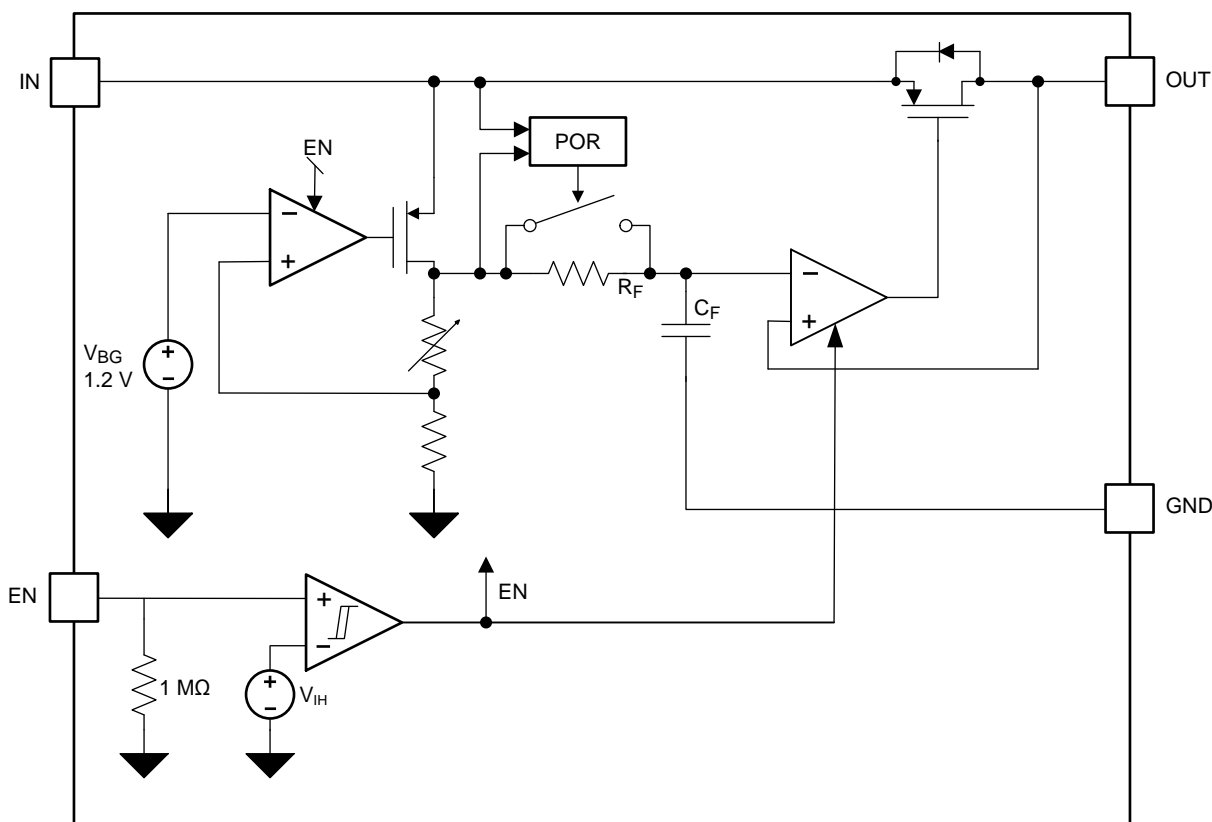
Figure 15. Dropout Over Temperature (100 mA)

7 Detailed Description

7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the LP5900 provides low noise, high PSRR, low quiescent current, as well as low line and load transient response figures. Using new innovative design techniques, the LP5900 offers class-leading noise performance without the need for a separate noise filter capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 No-Load Stability

The LP5900 will remain stable and in regulation with no external load.

7.3.2 Enable Control

The LP5900 Enable (EN) pin is internally held low by a 1-MΩ resistor to GND. The EN must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to ensure that the device is fully disabled.

7.3.3 Low Noise Output

Any internal noise at the LP5900 reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. This eliminates the need for the external bypass capacitor for noise suppression.

Feature Description (continued)

7.3.4 Thermal-Overload Protection

Thermal-overload protection disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 140°C, the output is enabled. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

7.4 Device Functional Modes

7.4.1 Operation with Enable Control

The LP5900 may be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3 nA. However, if the application does not require the shutdown feature, the EN pin can be tied to IN pin to keep the regulator output permanently on. In this case the supply voltage must be fully established 500 μ s or less to ensure correct operation of the start-up circuit. Failure to comply with this condition may cause a delayed start-up time of several seconds.

A 1 M Ω pull-down resistor ties the EN input to ground, and this ensures that the device will remain off when the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the [Electrical Characteristics](#) section under V_{IL} and V_{IH} .

7.4.2 Operation with Minimum Operating Input Voltage (V_{IN})

The LP5900 does not include any dedicated UVLO circuitry. The LP5900 internal circuitry is not fully functional until V_{IN} is at least 2.5 V. The output voltage is not regulated until $V_{IN} \geq (V_{OUT} + V_{DO})$.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5900 is a linear regulator capable of supplying 150 mA output current. Designed to meet the requirements of RF/Analog circuits, the device provides low noise, high PSRR, low quiescent current, and low line transient response figures. Using new innovative design techniques the LP5900 offers class-leading device noise performance and is designed to work with 0.47- μ F input and output ceramic capacitors (no bypass capacitor is required).

8.2 Typical Application

Figure 16 shows the typical application circuit for the LP5900. Input and output capacitances may need to be increased above the 0.47 μ F minimum for some applications.

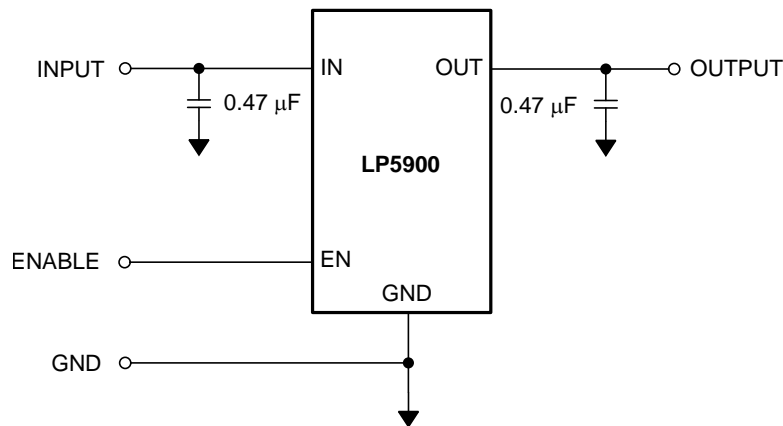


Figure 16. LP5900 Typical Application

8.2.1 Design Requirements

| DESIGN PARAMETER | MIN | MAX | UNITS |
|----------------------------------|------|-----|------------|
| Input voltage range | 2.5 | 5.5 | V |
| Output voltage | | 2.8 | V |
| Output current | | 150 | mA |
| Output capacitor range | 0.47 | 10 | μ F |
| Input/Output capacitor ESR range | 5 | 500 | m Ω |

8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air. As stated in [Recommended Operating Conditions](#), the allowable power dissipation for the device in a given package can be calculated using [Equation 1](#):

$$P_D = \frac{(T_{JMAX} - T_A)}{R_{\theta JA}} \quad (1)$$

The actual power dissipation across the device can be represented by [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

8.2.2.2 External Capacitors

Like any low-dropout regulator, the LP5900 requires external capacitors for regulator stability. The LP5900 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.2.1 Input Capacitor

An input capacitor is required for stability. The input capacitor should be at least equal to or greater than the output capacitor. It is recommended that a 0.47-μF capacitor be connected between the LP5900 IN pin and ground.

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5900, then it is recommended to increase the input capacitor to at least 2.2 μF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain 0.47 μF ±30% over the entire operating temperature range.

8.2.2.2.2 Output Capacitor

The LP5900 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X5R or X7R) in the 0.47 μF to 10 μF range, and with ESR between 5 mΩ to 500 mΩ, is suitable in the LP5900 application circuit. For this device the output capacitor should be connected between the OUT pin and a good ground connection and should be mounted within 1 cm of the device.

It may also be possible to use tantalum or film capacitors at the device output, OUT, but these are not as attractive for reasons of size and cost (see the [Capacitor Characteristics](#) section below).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

8.2.2.2.3 Capacitor Characteristics

The LP5900 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 μF to 4.7 μF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 0.47 μF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5900.

The temperature performance of ceramic capacitors varies by type and manufacturer. Most large value ceramic capacitors (≥ 2.2 μF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 μF to 4.7 μF range.

LP5900

SNVS358Q – JULY 2005 – REVISED FEBRUARY 2015

www.ti.com

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

8.2.3 Application Curve

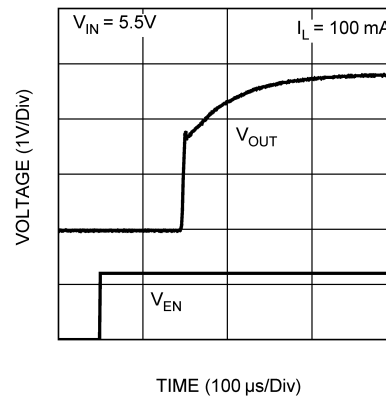


Figure 17. Enable Start-up Time, $I_{OUT} = 100$ mA, $V_{OUT} = 2.8$ V

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply must be well regulated. To ensure that the LP5900 output voltage is well regulated, the input supply should be at least $V_{OUT} + 1$ V.

10 Layout

10.1 Layout Guidelines

The device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply must be well regulated. To ensure that the LP5900 output voltage is well regulated, the input supply should be at least $V_{OUT} + 1$ V.

10.2 Layout Examples

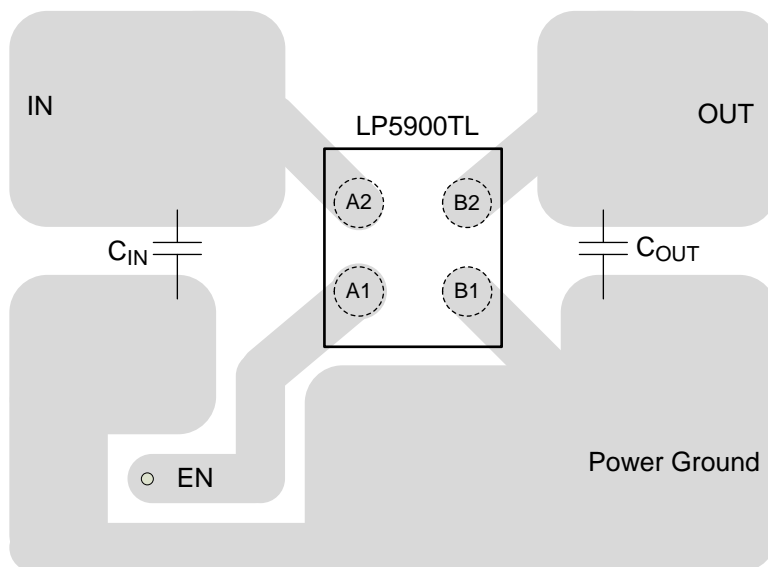


Figure 18. DSBGA Layout

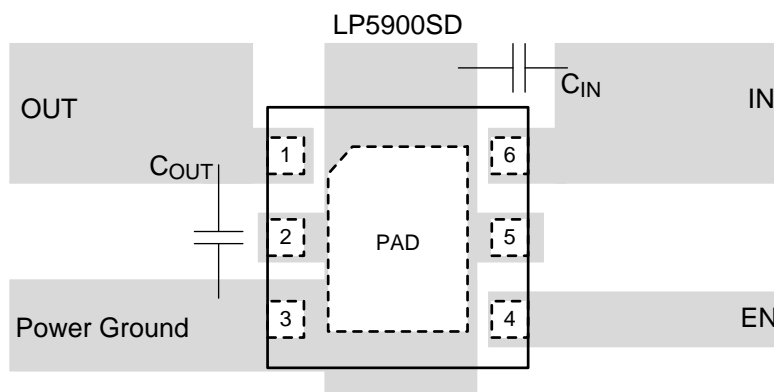


Figure 19. WSON Layout

10.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in Texas Instruments Application Note AN-1112, *DSBGA Wafer Level Chip Scale Package* (SNVA009). For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device.

Light with wavelengths in the red and infra-red part of the spectrum has the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

10.5 WSON Mounting

The 6-lead WSON package requires specific mounting techniques which are detailed in the TI AN-1187 *Leadless Leadframe Package (LLP)* ([SNOA401](#)). Referring to the section PCB Design Recommendations, it should be noted that the pad style which should be used with the WSON package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The exposed thermal pad on the bottom of the WSON package should be connected to a copper area on the PCB under the package. The use of thermal vias to remove heat from the package into the PCB is recommended. Connect the thermal pad to ground potential or leave floating. Do not connect the thermal pad to any potential other than the same ground potential seen at device pin 3.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

AN-1112 *DSBGA Wafer Level Chip Scale Package*, [SNVA009](#).

TI AN-1187 *Leadless Leadframe Package (LLP)*, [SNOA401](#).

IC Package Thermal Metrics application report, [SPRA953](#).

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP5900SD-1.5 | NRND | WSO | NGF | 6 | 1000 | TBD | Call TI | Call TI | -40 to 125 | L15 | |
| LP5900SD-1.5/NOPB | ACTIVE | WSO | NGF | 6 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L15 | Samples |
| LP5900SD-1.8/NOPB | ACTIVE | WSO | NGF | 6 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L17 | Samples |
| LP5900SD-2.0/NOPB | ACTIVE | WSO | NGF | 6 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L18 | Samples |
| LP5900SD-2.2/NOPB | ACTIVE | WSO | NGF | 6 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L19 | Samples |
| LP5900SD-2.5 | NRND | WSO | NGF | 6 | 1000 | TBD | Call TI | Call TI | -40 to 125 | L13 | |
| LP5900SD-2.5/NOPB | ACTIVE | WSO | NGF | 6 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L13 | Samples |
| LP5900SD-2.7/NOPB | ACTIVE | WSO | NGF | 6 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L14 | Samples |
| LP5900SD-2.8/NOPB | ACTIVE | WSO | NGF | 6 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L12 | Samples |
| LP5900SD-3.0/NOPB | ACTIVE | WSO | NGF | 6 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L20 | Samples |
| LP5900SD-3.3/NOPB | ACTIVE | WSO | NGF | 6 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L16 | Samples |
| LP5900SDX-1.5/NOPB | ACTIVE | WSO | NGF | 6 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L15 | Samples |
| LP5900SDX-1.8/NOPB | ACTIVE | WSO | NGF | 6 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L17 | Samples |
| LP5900SDX-2.0/NOPB | ACTIVE | WSO | NGF | 6 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L18 | Samples |
| LP5900SDX-2.2/NOPB | ACTIVE | WSO | NGF | 6 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L19 | Samples |
| LP5900SDX-2.5/NOPB | ACTIVE | WSO | NGF | 6 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L13 | Samples |
| LP5900SDX-2.7/NOPB | ACTIVE | WSO | NGF | 6 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L14 | Samples |
| LP5900SDX-2.8/NOPB | ACTIVE | WSO | NGF | 6 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L12 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP5900SDX-3.0/NOPB | ACTIVE | WSO | NGF | 6 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L20 | Samples |
| LP5900SDX-3.3/NOPB | ACTIVE | WSO | NGF | 6 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | L16 | Samples |
| LP5900TL-1.5/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-1.575/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-1.8/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-1.9/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-2.0/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-2.2/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-2.3/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-2.5/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-2.6/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-2.65/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-2.7/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-2.75/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-2.8/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-2.85/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-3.0/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TL-3.3/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP5900TL-4.5/NOPB | ACTIVE | DSBGA | YZR | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-1.5/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-1.8/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-1.9/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.0/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.1/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.2/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.3/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.5/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.6/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.65/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.7/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.75/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.8/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-2.85/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-3.0/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-3.3/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900TLX-4.5/NOPB | ACTIVE | DSBGA | YZR | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP5900XR-1.8/NOPB | ACTIVE | DSBGA | YPF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900XR-2.8/NOPB | ACTIVE | DSBGA | YPF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900XRX-1.8/NOPB | ACTIVE | DSBGA | YPF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| LP5900XRX-2.8/NOPB | ACTIVE | DSBGA | YPF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP5900SD-1.5 | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SD-1.5/NOPB | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SD-1.8/NOPB | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SD-2.0/NOPB | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SD-2.2/NOPB | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SD-2.5 | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SD-2.5/NOPB | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SD-2.7/NOPB | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SD-2.8/NOPB | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SD-3.0/NOPB | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SD-3.3/NOPB | WSO | NGF | 6 | 1000 | 178.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SDX-1.5/NOPB | WSO | NGF | 6 | 4500 | 330.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SDX-1.8/NOPB | WSO | NGF | 6 | 4500 | 330.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SDX-2.0/NOPB | WSO | NGF | 6 | 4500 | 330.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SDX-2.2/NOPB | WSO | NGF | 6 | 4500 | 330.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SDX-2.5/NOPB | WSO | NGF | 6 | 4500 | 330.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SDX-2.7/NOPB | WSO | NGF | 6 | 4500 | 330.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SDX-2.8/NOPB | WSO | NGF | 6 | 4500 | 330.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP5900SDX-3.0/NOPB | WSO | NGF | 6 | 4500 | 330.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900SDX-3.3/NOPB | WSO | NGF | 6 | 4500 | 330.0 | 12.4 | 2.8 | 2.5 | 1.0 | 8.0 | 12.0 | Q1 |
| LP5900TL-1.5/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-1.575/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-1.8/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-1.9/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-2.0/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-2.2/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-2.3/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-2.5/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-2.6/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-2.65/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-2.7/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-2.75/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-2.8/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-2.85/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-3.0/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-3.3/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TL-4.5/NOPB | DSBGA | YZR | 4 | 250 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-1.5/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-1.8/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-1.9/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.0/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.1/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.2/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.3/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.5/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.6/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.65/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.7/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.75/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.8/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-2.85/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-3.0/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-3.3/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900TLX-4.5/NOPB | DSBGA | YZR | 4 | 3000 | 178.0 | 8.4 | 1.15 | 1.16 | 0.79 | 4.0 | 8.0 | Q1 |
| LP5900XR-1.8/NOPB | DSBGA | YPF | 4 | 250 | 178.0 | 8.4 | 1.16 | 1.2 | 0.4 | 4.0 | 8.0 | Q1 |
| LP5900XR-2.8/NOPB | DSBGA | YPF | 4 | 250 | 178.0 | 8.4 | 1.16 | 1.2 | 0.4 | 4.0 | 8.0 | Q1 |
| LP5900XR-1.8/NOPB | DSBGA | YPF | 4 | 3000 | 178.0 | 8.4 | 1.16 | 1.2 | 0.4 | 4.0 | 8.0 | Q1 |
| LP5900XR-2.8/NOPB | DSBGA | YPF | 4 | 3000 | 178.0 | 8.4 | 1.16 | 1.2 | 0.4 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

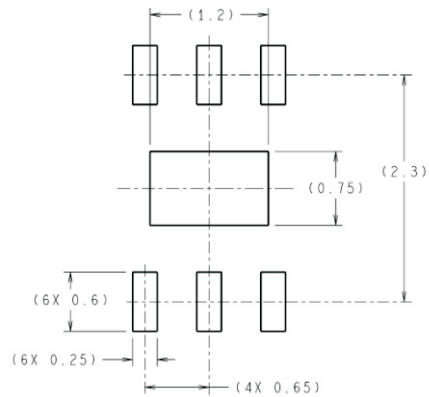


*All dimensions are nominal

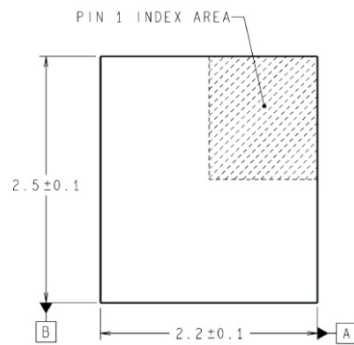
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP5900SD-1.5 | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SD-1.5/NOPB | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SD-1.8/NOPB | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SD-2.0/NOPB | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SD-2.2/NOPB | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SD-2.5 | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SD-2.5/NOPB | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SD-2.7/NOPB | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SD-2.8/NOPB | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SD-3.0/NOPB | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SD-3.3/NOPB | WSN | NGF | 6 | 1000 | 210.0 | 185.0 | 35.0 |
| LP5900SDX-1.5/NOPB | WSN | NGF | 6 | 4500 | 367.0 | 367.0 | 35.0 |
| LP5900SDX-1.8/NOPB | WSN | NGF | 6 | 4500 | 367.0 | 367.0 | 35.0 |
| LP5900SDX-2.0/NOPB | WSN | NGF | 6 | 4500 | 367.0 | 367.0 | 35.0 |
| LP5900SDX-2.2/NOPB | WSN | NGF | 6 | 4500 | 367.0 | 367.0 | 35.0 |
| LP5900SDX-2.5/NOPB | WSN | NGF | 6 | 4500 | 367.0 | 367.0 | 35.0 |
| LP5900SDX-2.7/NOPB | WSN | NGF | 6 | 4500 | 367.0 | 367.0 | 35.0 |
| LP5900SDX-2.8/NOPB | WSN | NGF | 6 | 4500 | 367.0 | 367.0 | 35.0 |
| LP5900SDX-3.0/NOPB | WSN | NGF | 6 | 4500 | 367.0 | 367.0 | 35.0 |
| LP5900SDX-3.3/NOPB | WSN | NGF | 6 | 4500 | 367.0 | 367.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP5900TL-1.5/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-1.575/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-1.8/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-1.9/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-2.0/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-2.2/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-2.3/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-2.5/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-2.6/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-2.65/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-2.7/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-2.75/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-2.8/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-2.85/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-3.0/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-3.3/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TL-4.5/NOPB | DSBGA | YZR | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-1.5/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-1.8/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-1.9/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.0/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.1/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.2/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.3/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.5/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.6/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.65/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.7/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.75/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.8/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-2.85/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-3.0/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-3.3/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900TLX-4.5/NOPB | DSBGA | YZR | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900XR-1.8/NOPB | DSBGA | YPF | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900XR-2.8/NOPB | DSBGA | YPF | 4 | 250 | 210.0 | 185.0 | 35.0 |
| LP5900XR-1.8/NOPB | DSBGA | YPF | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| LP5900XR-2.8/NOPB | DSBGA | YPF | 4 | 3000 | 210.0 | 185.0 | 35.0 |

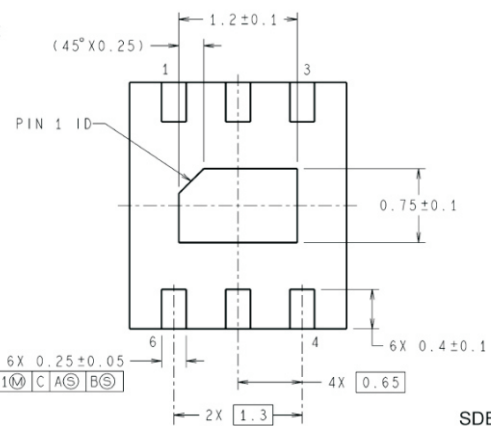
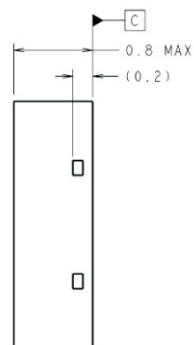
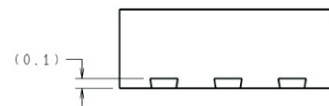
NGF0006A



RECOMMENDED LAND PATTERN

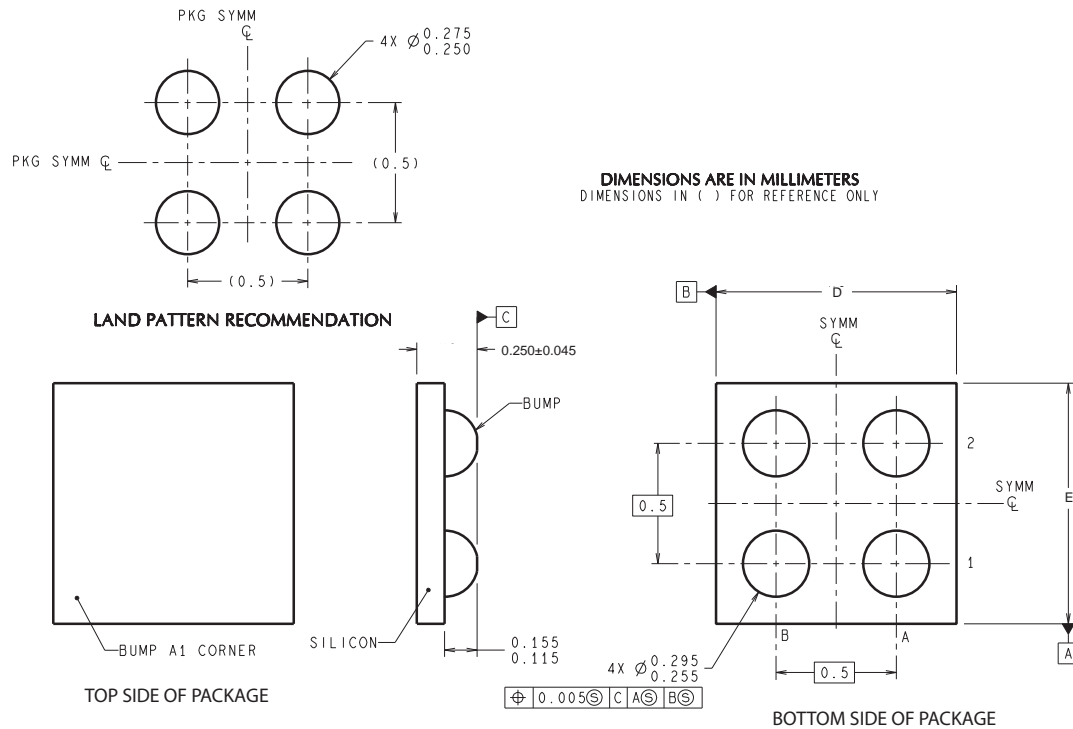


DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



SDB06A (Rev A)

YPF0004



XRA04XXX (Rev C)

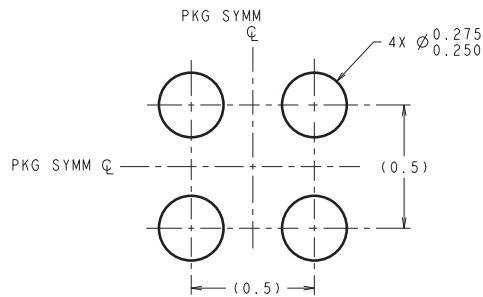
D: Max = 1.108 mm, Min = 1.047 mm

E: Max = 1.083 mm, Min = 1.022 mm

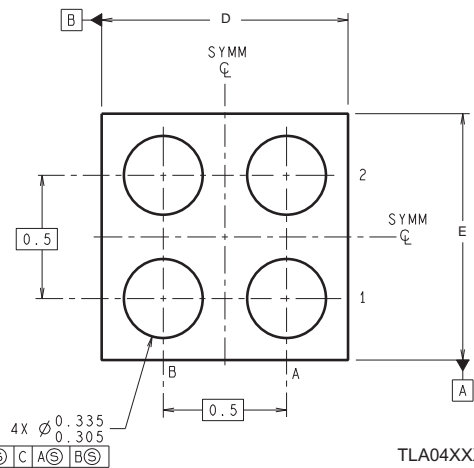
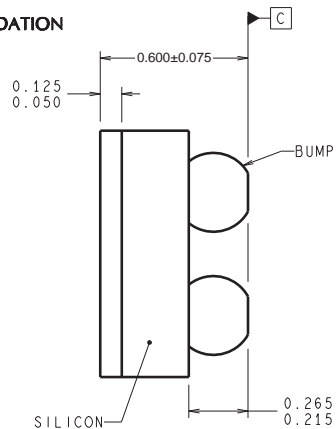
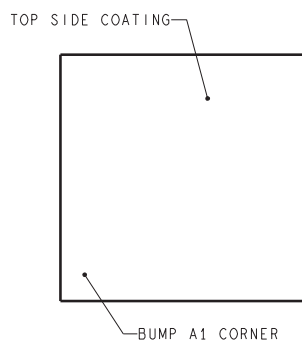
4215204/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

YZR0004



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION

TLA04XXX (Rev D)

D: Max = 1.108 mm, Min = 1.047 mm

E: Max = 1.083 mm, Min = 1.022 mm

4215042/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

| | |
|------------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Applications Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| | |
|-------------------------------|--|
| Automotive and Transportation | www.ti.com/automotive |
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Video and Imaging | www.ti.com/video |

TI E2E Community

e2e.ti.com