Protection Device

TVS (Transient Voltage Suppressor)

ESD101-B1-02 Series

Bi-directional, 5.5 V, 0.1 pF, 0201, 0402, RoHS and Halogen Free compliant

ESD101-B1-02ELS
ESD101-B1-02EL

Data Sheet

Revision 1.3, 2015-07-13
Final

Power Management & Multimarket

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1 Product Overview

1.1 Features

- ESD / transient protection of high speed data lines according to:
  - **IEC61000-4-2 (ESD): ±14 kV (air), ±12 kV(contact)**
  - **IEC61000-4-4 (EFT): ±1.5 kV / ±30 A (5/50 ns)**
  - **IEC61000-4-5 (surge): ±2 A (8/20 µs)**
- Bi-directional working voltage up to: V_{RWM} **= ±5.5 V**
- Extremely low capacitance C_L **= 0.1 pF (typical) at** f **= 1 GHz**
- Very low clamping voltage: V_{CL} **= 30 V (typical) at** I_{TLP} **= 16 A**
- Very low reverse current: I_R **< 0.1 nA**
- Very low dynamic resistance: R_{DYN} **= 1.5 Ω (typical)**
- Pb-free package (RoHS compliant)

1.2 Application Examples [3]

- Tailored for ESD Protection of capacitance-susceptible application like
  - Super high speed interface
  - RF antenna

1.3 Product Description

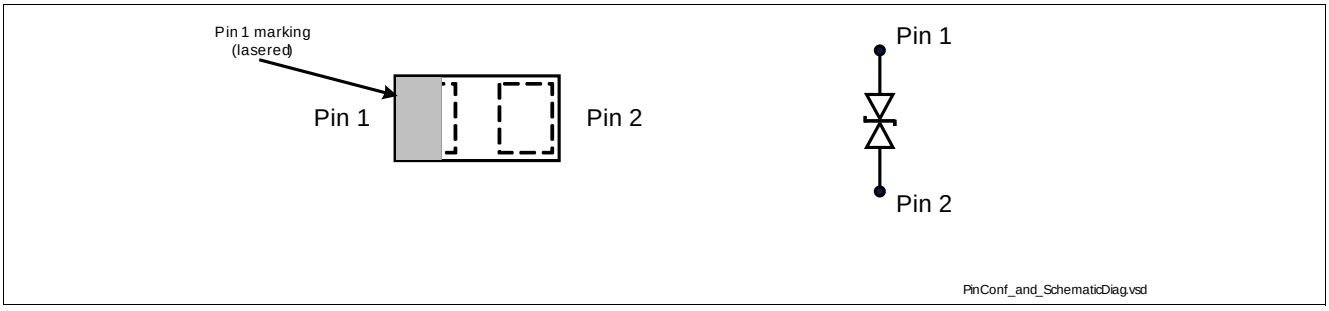

Figure 1 Pin configuration and Schematic diagram

Table 1 Part Information

Type	Package	Configuration	Marking code
ESD101-B1-02ELS	TSSLP-2-4	1 line, bi-directional	R
ESD101-B1-02EL	TSLP-2-20	1 line, bi-directional	R

2 Maximum Ratings

Table 2 Maximum Rating *at T_A = 25 °C, unless otherwise specified*[1)]

Parameter	Symbol	Values	Unit
ESD air discharge[2)] ESD contact discharge[2)]	V_{ESD}	±14 ±12	kV
Peak pulse power	P_{PK}	30	W
Peak pulse current[3)]	I_{PP}	±2	A
Operating temperature	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

1) Device is electrically symmetrical

2) V_{ESD} according to IEC61000-4-2

3) Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

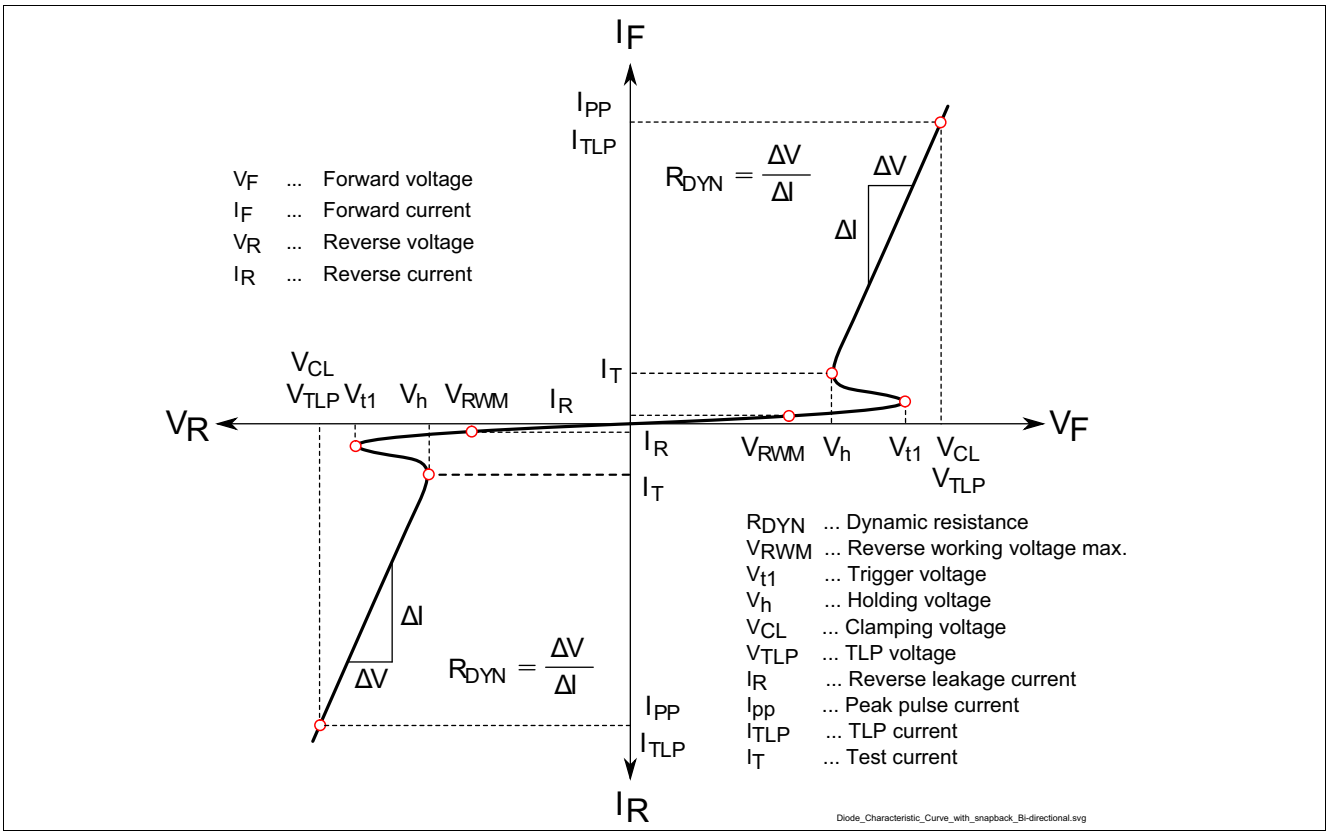

Figure 2 Definitions of electrical characteristics

Table 3 DC Characteristics at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-5.5	–	5.5	V	
Trigger voltage	V_{t1}	6.1	–	–		
Holding voltage	V_h	6.1	7.0	7.9		I_T = 10 mA
Reverse leakage current	I_R	–	<0.1	20	nA	V_R = 5.5 V

1) Device is electrically symmetrical

Table 4 AC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	–	0.2	pF	V_R = 0 V, f = 1 MHz
		–	0.1	–		V_R = 0V, f = 1 GHz
Serie inductance	L_S	– –	0.2 0.4	– –	nH	ESD101-B1-02ELS ESD101-B1-02EL

Table 5 ESD and Surge Characteristics at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[2)]	V_{CL}	–	18	–	V	I_{TLP} = 8 A, t_p = 100 ns
		–	30	–		I_{TLP} = 16 A, t_p = 100 ns
Clamping voltage[3)]		–	9	–		I_{PP} = 1 A, t_p = 8/20 µs
		–	13	–		I_{PP} = 2 A, t_p = 8/20 µs
Dynamic resistance[2)]	R_{DYN}	–	1.5	–	Ω	t_p = 100 ns

1) Device is electrically symmetrical

2) Please refer to Application Note AN210[1]. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 300ps.

3) Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5

4 Typical Characteristics Diagrams

Typical characteristics diagrams at T_A = 25°C, unless otherwise specified

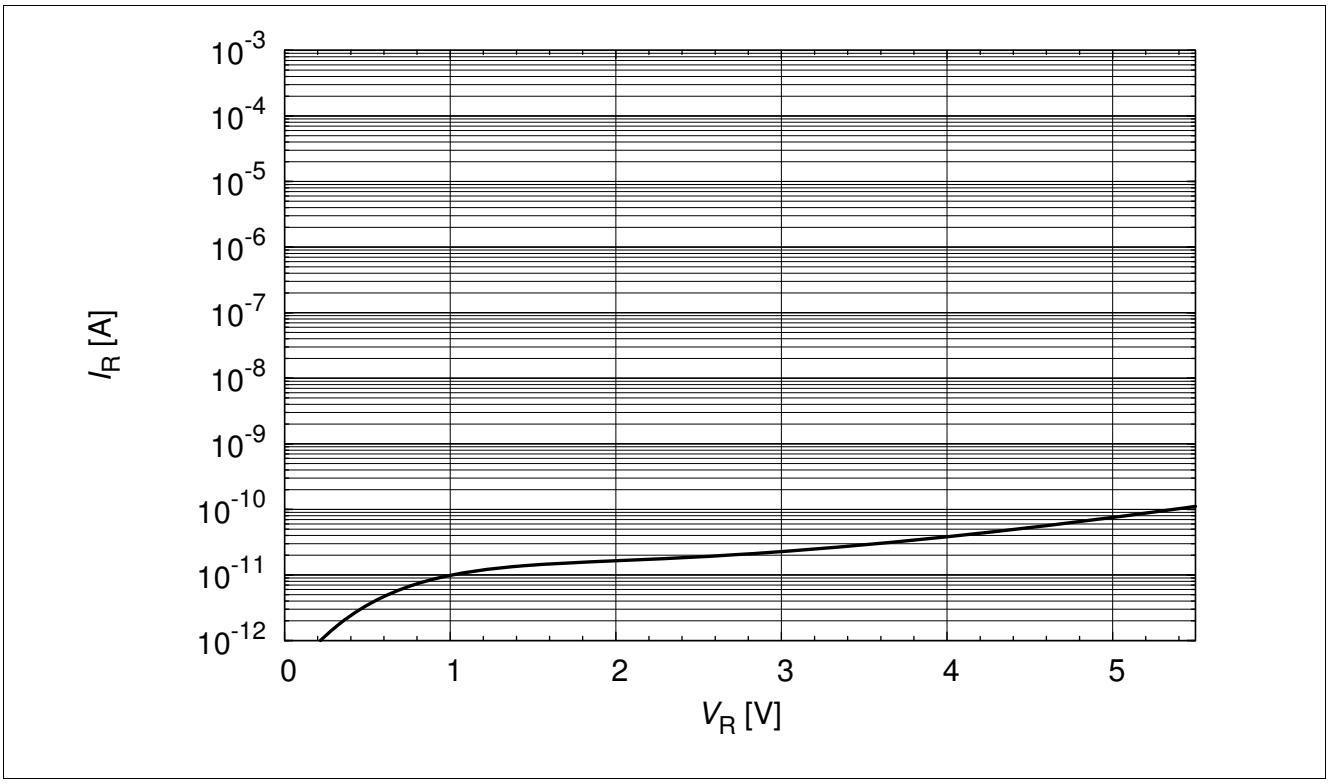

Figure 3 Reverse leakage current: $I_R = f(V_R)$

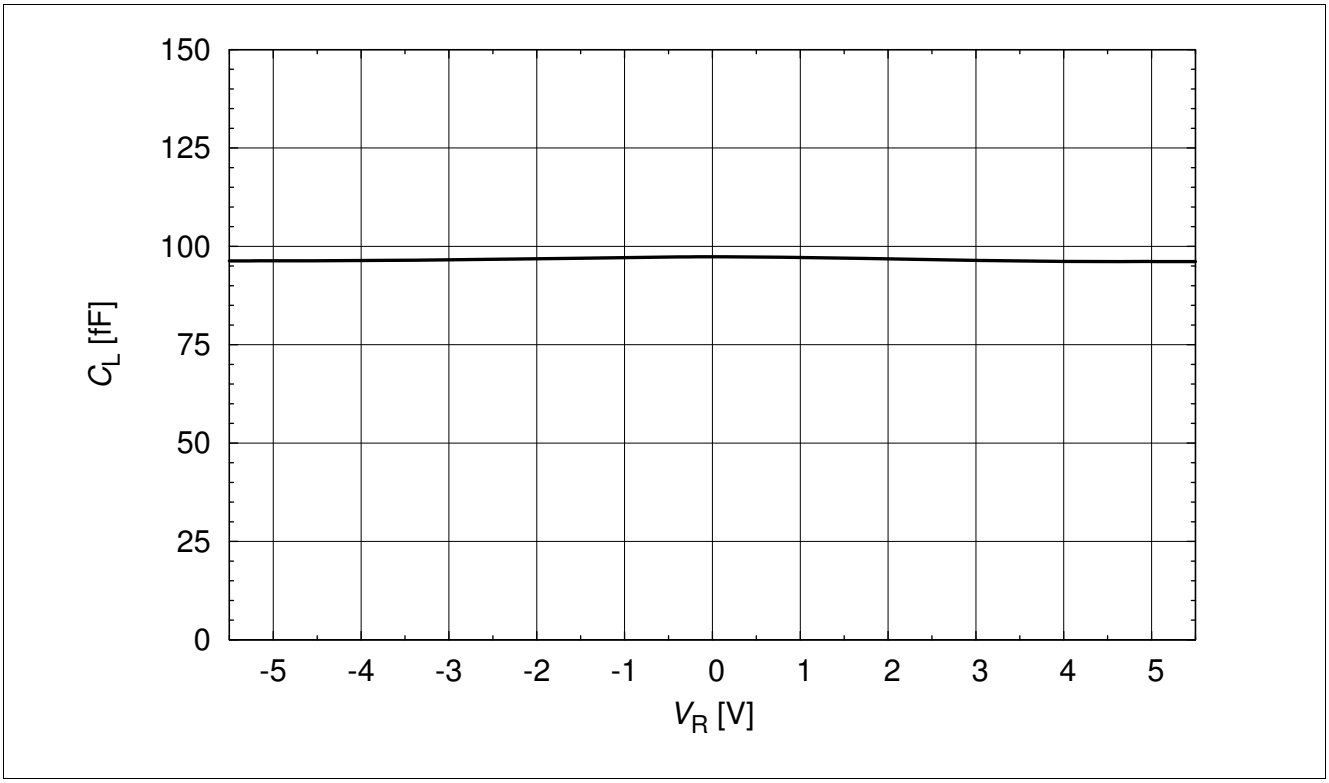

Figure 4 Line capacitance $C_L = f(V_R)$, f = 1 GHz

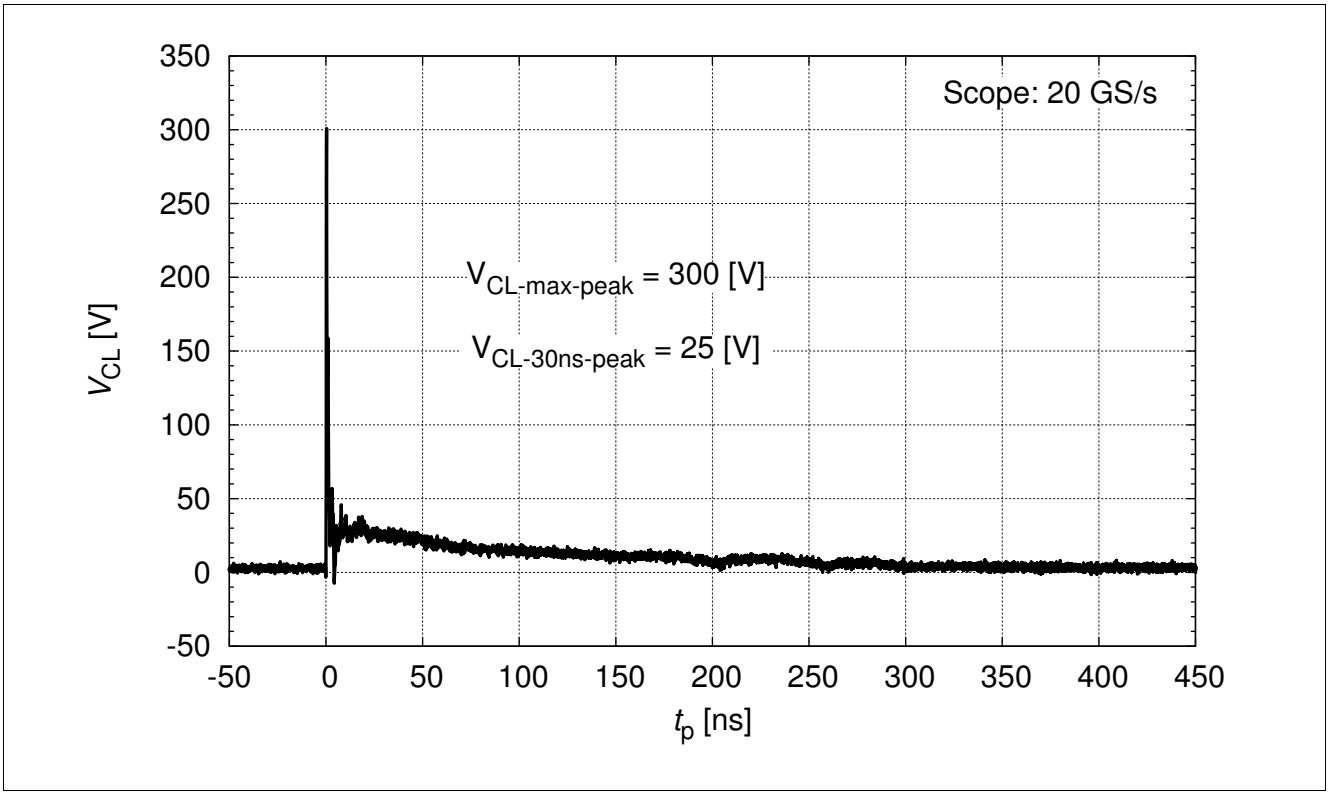

Figure 5 Clamping voltage (ESD): V_{CL} = $f(t)$, 8 kV positive pulse from pin 1 to pin 2

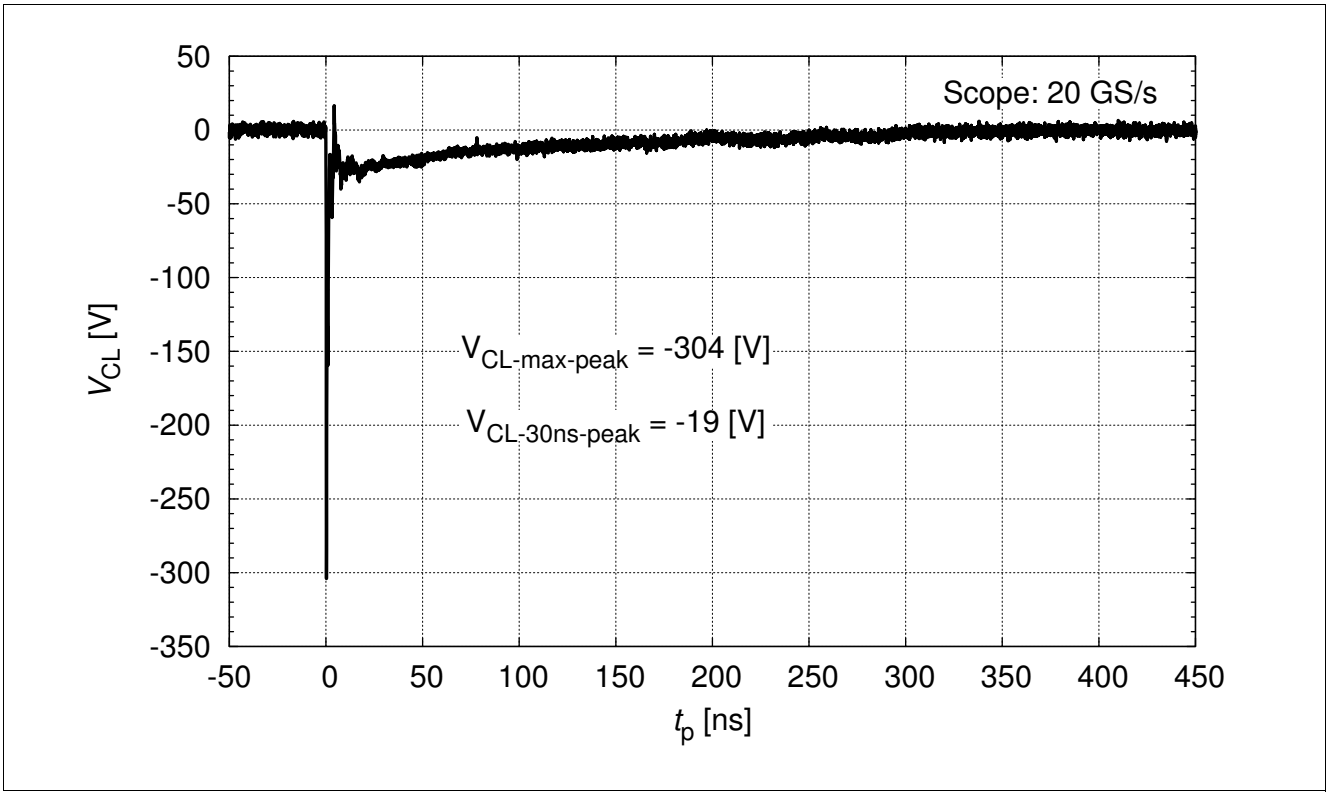

Figure 6 Clamping voltage (ESD): V_{CL} = $f(t)$, 8 kV negative pulse from pin 1 to pin 2

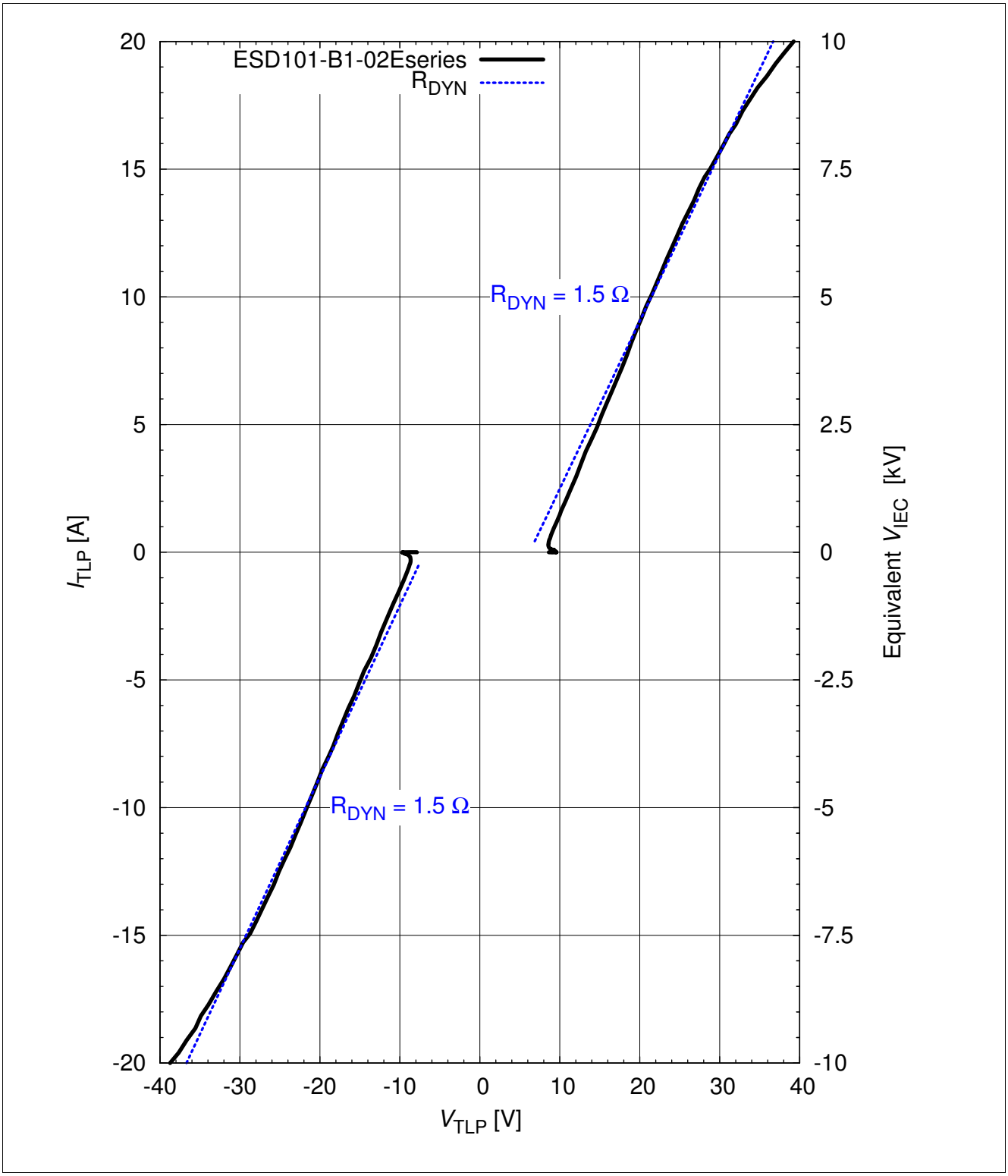

Figure 7 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1], pin 1 to pin 2

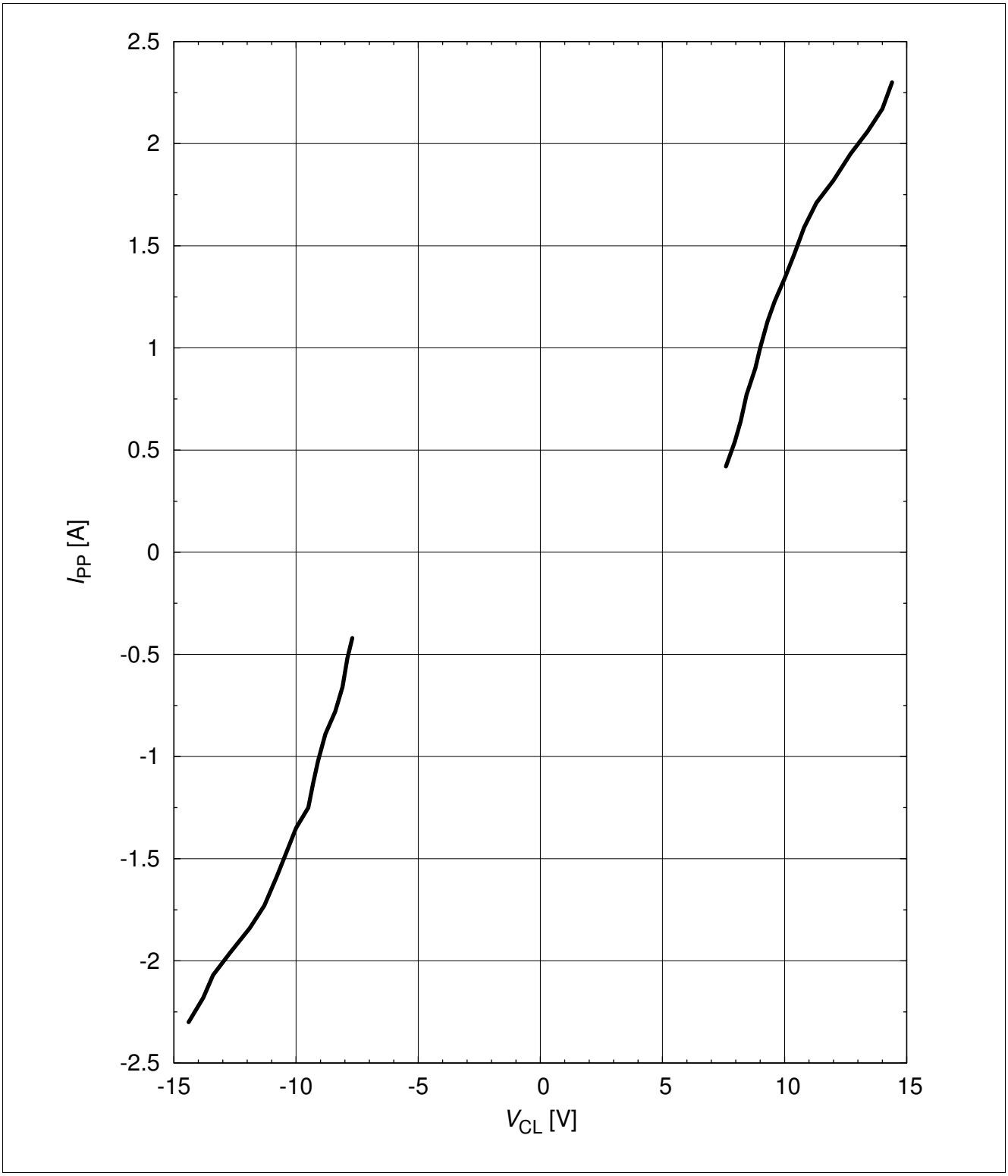

Figure 8 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ [1], pin 1 to pin 2

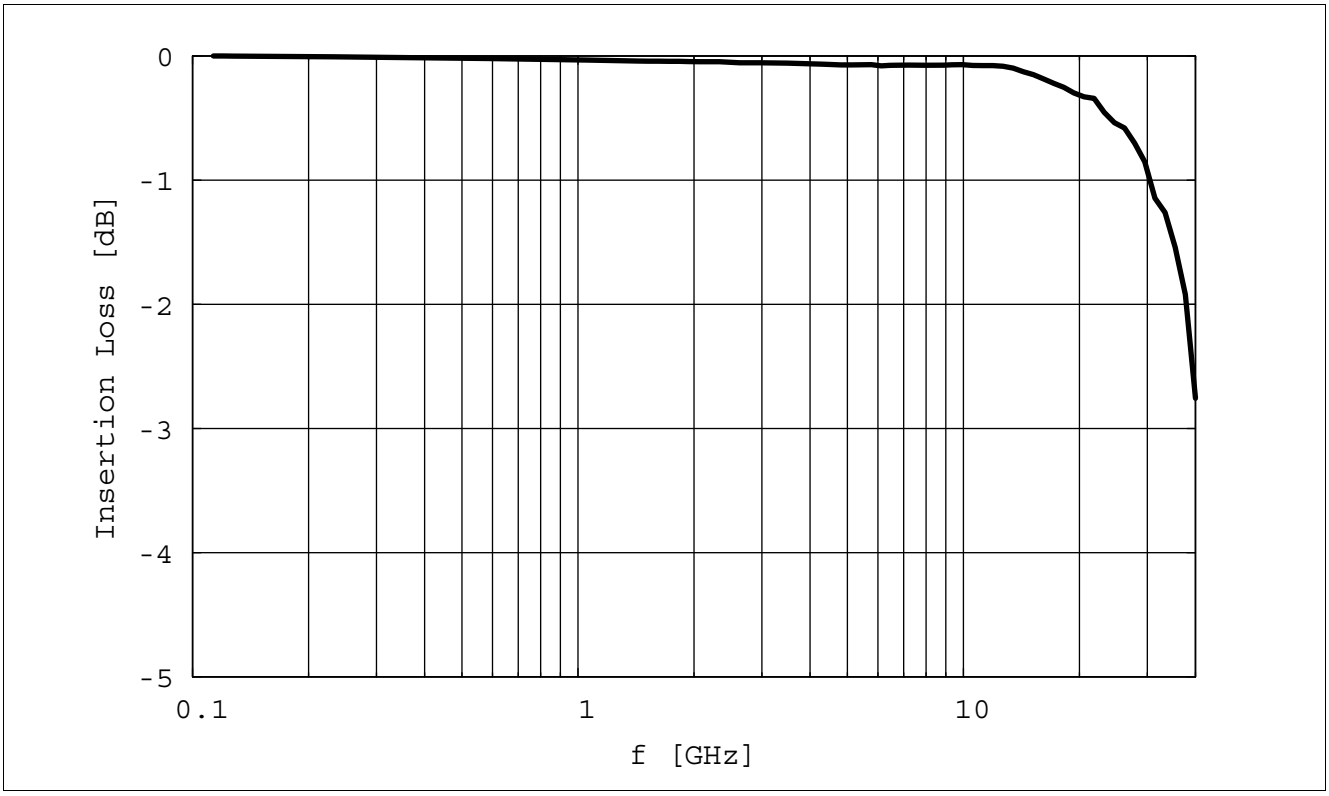

Figure 9 Insertion loss vs. frequency in a 50 Ω system (ESD101-B1-02ELS)

5 Package Information

5.1 TSSLP-2-4

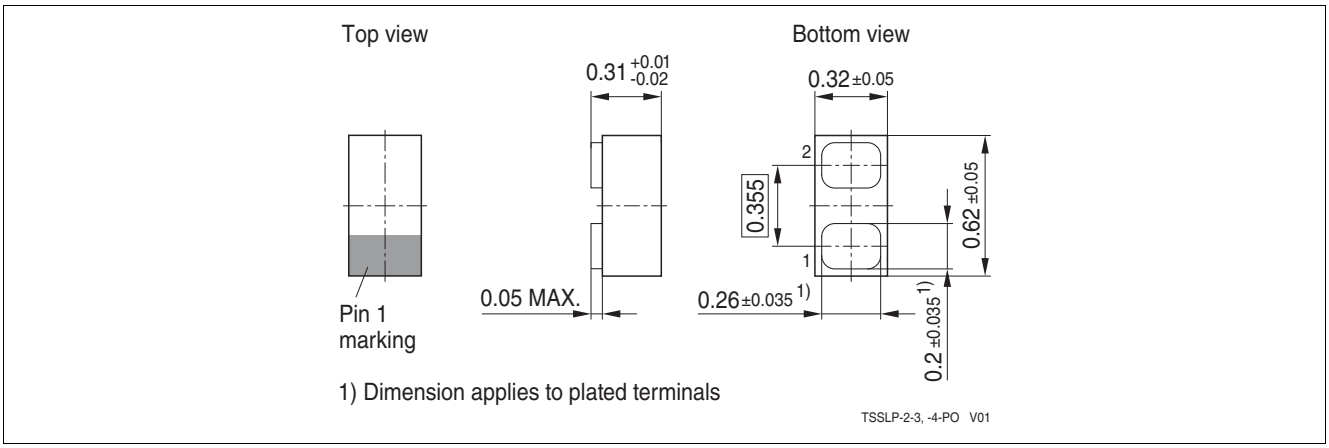

Figure 10 TSSLP-2-4 Package outline (dimension in mm)

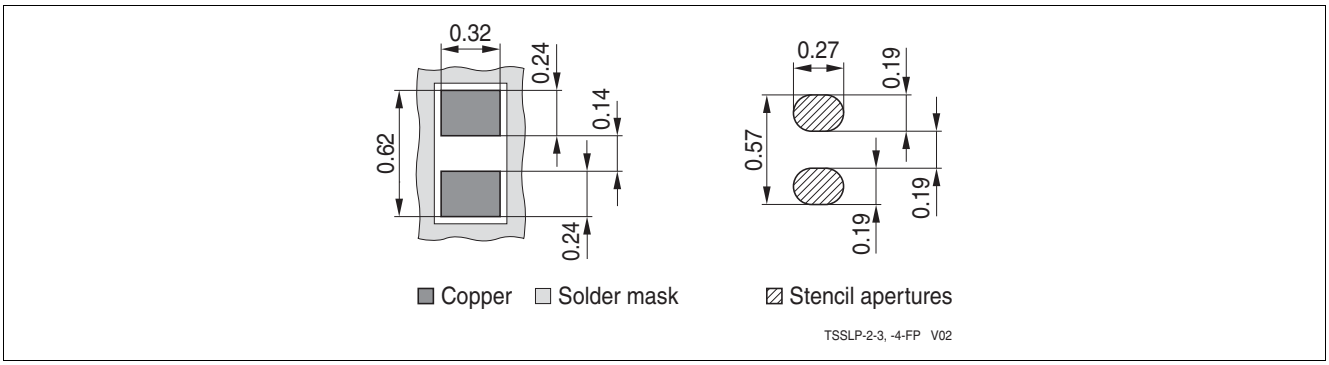

Figure 11 TSSLP-2-4 Footprint (dimension in mm)

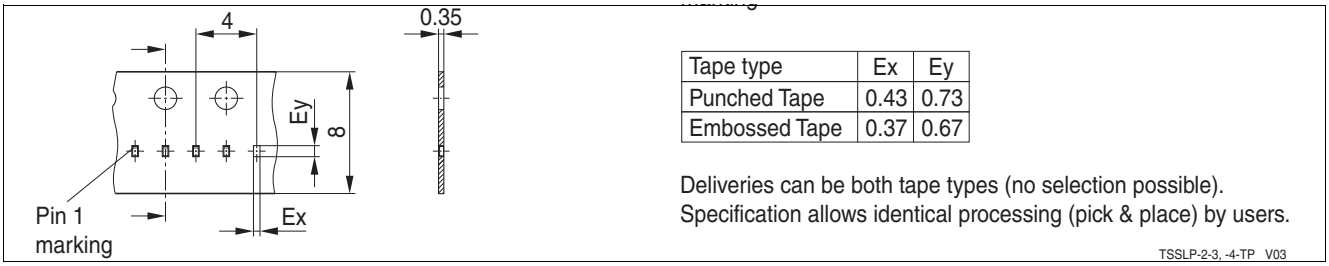

Figure 12 TSSLP-2-4 Packing (dimension in mm)

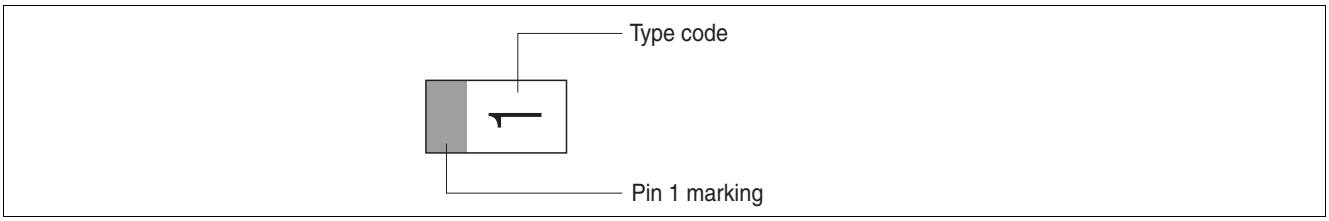

Figure 13 TSSLP-2-4 Marking example Table 1 “Part Information” on Page 3

5.2 TSLP-2-20

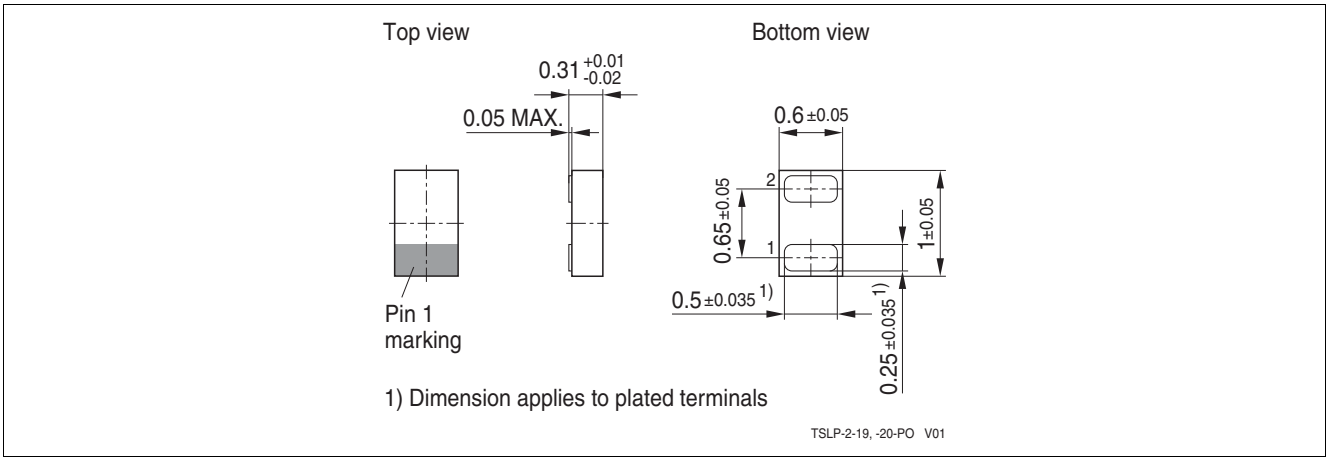

Figure 14 TSLP-2-20 Package outline (dimension in mm)

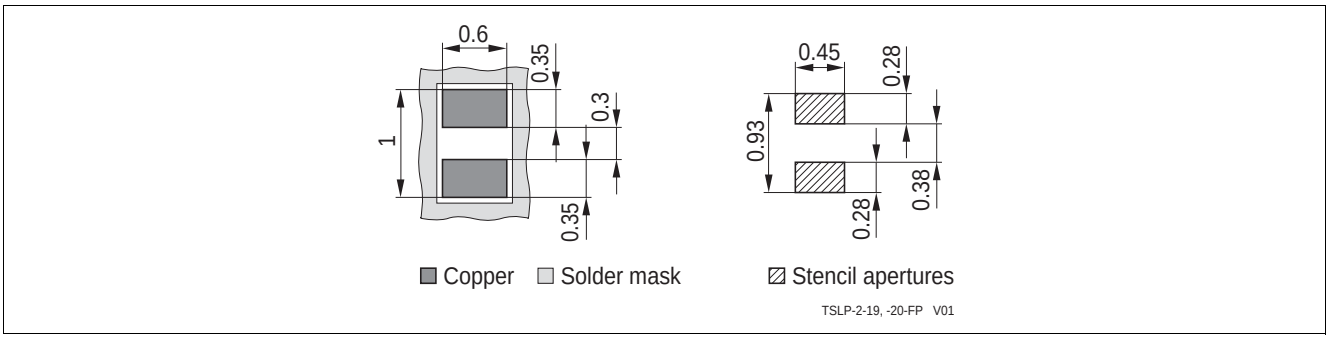

Figure 15 TSLP-2-20 Footprint (dimension in mm)

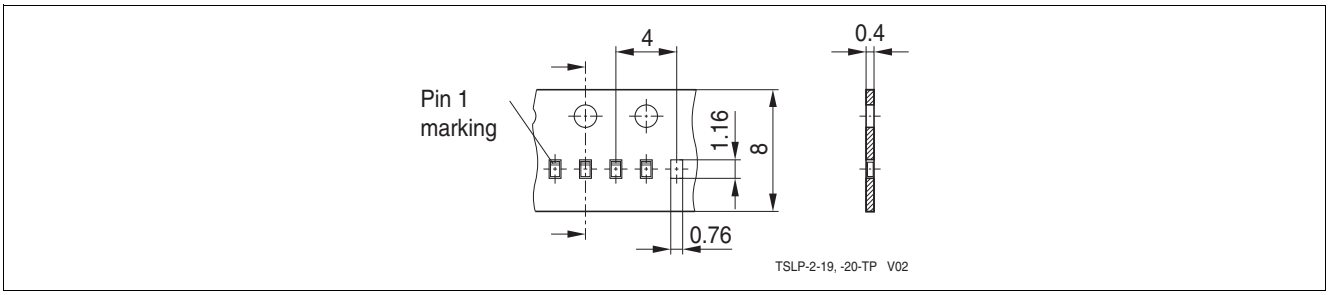

Figure 16 TSLP-2-20 Packing (dimension in mm)

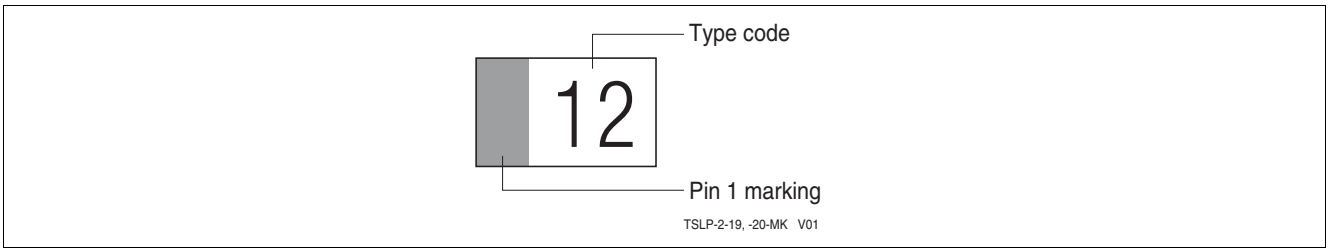

Figure 17 TSLP-2-20 Marking example **Table 1 "Part Information" on Page 3**

References

[1] Infineon Technologies AG, “Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology”, **Application Note AN210**, RF and Protection Devices, April 22, 2010, Rev.1.0

[2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

[3] Infineon AC - **Application Note AN327**: ESD101-B1 / ESD103-B1, Bi-directional Ultra Low Capacitance Transient Voltage Suppression Diodes for High Power RF Applications.

Revision History: Rev. .1.2, 2013-07-23	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.3, 2015-07-13	
All	Layout changes
5	Table 3-1) updated

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